Realization of all-optical multi-logic functions and a digital adder with input beam power management for multi-input injection locking in a single-mode Fabry-Pérot laser diode

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Abstract: We propose a novel idea for the suppression of the dominant mode of the single-mode Fabry-Pérot laser diode (SMFP-LD) to realize all-optical multi-logic functions and a digital adder. The basic principle of the proposed scheme is the power management of input beams to suppress the dominant mode of the SMFP-LD for multi-input injection locking. The proposed principle is explained and implemented to realize all-optical multi-logic functions and a digital adder at an input data rate of 10 Gbps. A clear eye opening with an extinction ratio of about 12 dB and a rising-falling time of less than 40 ps are observed at the outputs. The bit error rate (BER) performance is measured for all logic gates and half adder operation. We found there is no BER floor up to BER of 10^{-12} and the maximum power penalty of about 1.2 dB at a BER of 10^{-9}.

OCIS codes: (200.4660) Optical logic; (140.3520) lasers, injection-locked.

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1. Introduction

All-optical signal processing is one of the most promising solutions to meet the demands of future high-speed and large capacity optical communication networks [1,2]. All-optical logic gates are the basic functional blocks of all-optical signal processing such as encryption and data encoding, pattern matching, binary addition, counting, addressing, de-multiplexing, regeneration, switching, and other computing techniques [3]. One of the applications of the logic functions is to realize a combinational circuit such as a digital adder. A digital adder is a combinational circuit that generates the sum of two binary digits. Various schemes to realize optical logic gates and digital adders have been proposed and demonstrated using non-linear fiber such as an Er-doped optical amplifier [4] and periodical poled $LiNbO_3$ (PPLN) [5]. Also used have been semiconductor materials, such as a semiconductor optical amplifier (SOA) [6–8], and FP-LDs [9–11]. The Er-doped optical amplifier is operated at a low speed of 1 Gbps. PPLN-based gates are costly (they require several light sources). The most widely used and attractive SOA-based logic functions and SOA-based digital combinational circuits also require an interferrometric structure [3] that requires two or more devices with identical characteristics, accurate control, and stabilization. Using noninterferrometric SOA-based logic gates, two additional beams and other associated components are needed to obtain the logic functions. Logic gates and signal processing using multimode Fabry-Pérot laser diodes (MMFP-LDs) need an additional external probe beam and associated components, and are based on the power of a single injected beam to modulate the gain of the probe beam [9,10], [12,13]. Thus far, only NOR and NOT gates have been demonstrated using MMFP-LDs [9,10]. Absorption modulation is an optical signal processing technique using FP-LDs. During absorption modulation, a polarization-sensitive polarization beam splitter is necessary to separate the TE- and TM-polarized light, which is expensive [10]. Hence, signal processing using MMFP-LDs and absorption modulation scheme are expensive and complex.

In this paper, a novel idea for suppressing the dominant mode of a single-mode Fabry-Pérot laser diode (SMFP-LD) based on the power management of the input beams for multi-input injection locking is proposed and experimentally demonstrated. We used SMFP-LDs for the proposed scheme. SMFP-LDs do not require any external probe beam and associated components because they operate in a self-locked dominant mode [11,14]. Additionally, our idea does not require an expensive polarization beam splitter, as is needed in absorption modulation using FP-LDs. Hence, the proposed idea has a simple configuration, resulting in a cost- and power-effective solution. With this principle, all-optical multi-logic functions (NAND, XNOR, AND, and XOR) with a digital adder (half adder) function are realized. The proposed scheme is verified with output waveforms, clear eye openings, low rising-falling times, and bit error rate (BER) performance at a data rate of 10 Gbps.

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2. Principle of operation

In the proposed scheme, we used SMFP-LDs, which were specially designed and developed in our laboratory [15]. The SMFP-LD used here has a dominant self-locked single longitudinal mode with a high side mode suppression ratio. The SMFP-LD is obtained by eliminating the inclinations of 6° to 8° of the coupling fiber present in conventional FP-LDs, thereby, forming an external cavity between the laser diode and the fiber. The SMFP-LD consists of a FP-LD chip with a multi-quantum well of 300 μm and an external cavity length of 4 mm. By varying the temperature, a mode-matching condition is achieved for both cavities. The refractive index of the active region changes with the change in the temperature. As a result, there is a change in the optical path length in the laser diode, providing the optimal mode-matching condition for single-mode oscillation. This single-mode oscillation can be tuned to another mode by varying the operating temperature, which gives the tunability of SMFP-LD. The self-locking mode of SMFP-LD is tunable over a wide range with a wavelength difference of about 10 nm. The SMFP-LD shows characteristics similar to those of MMFP-LDs including the mechanical stability, wavelength stability, and power stability of laser diode and also shows similar characteristics with the injection of external beams [15]. The only difference between SMFP-LDs and MMFP-LDs is that the former does not require an external probe beam for signal processing.

The key principle of the proposed scheme is the suppression of the dominant mode of the SMFP-LD with proper power management of the input beams for multi-input injection locking as illustrated in Fig. 1. A basic block diagram of the proposed scheme with the optical logic functions and the digital adder (half adder) is shown in Fig. 1 (a). SMFP-LD1 has a dominant mode at λ_{01}, which is suppressed only when both inputs are in the logic high mode ('1'). This results in the logic NAND gate, which is attained by proper power management of the input beam power and the corresponding wavelength detuning. The SMFP-LD2 has a dominant mode at λ_{02} which works on the supporting beam principle to suppress the dominant mode. It has multiple inputs (3 inputs), among which one is a major beam with the other two the supporting beams. It should be noted that the presence of supporting beams alone without the major beam cannot suppress the dominant mode of the SMFP-LD. One of the inputs for the SMFP-LD2 is the output from the SMFP-LD1, which acts as the major beam, and the other input is a combination of two input beams, A and B, which individually act as supporting beam. The dominant mode of SMFP-LD2 is suppressed when the major beam along with either of the input beams A and B is '1'. For all other conditions, the combined power of the beams input to SMFP-LD2 is not sufficient to suppress the dominant mode of SMFP-LD2. This phenomenon is utilized to realize logic XNOR gate. SMFP-LD3 and SMFP-LD4 work on the basic principle of the injection locking of semiconductor lasers in which the power of a single input is enough to suppress the dominant mode of the SMFP-LDs [16], which are used to realize the logic NOT gate. We used a logic NOT gate at the output of NAND and a XNOR gate to obtain the logic AND and logic XOR gate, respectively. The output of the logic AND gate acts as a CARRY, and the output of the logic XOR gate acts as a SUM for the proposed digital half adder. Figure 1 (b)-(i), Fig. 1 (b)-(ii), and Fig. 1 (b)-(iii) show a spectrum schematic of the injection locking, multi-input injection locking and supporting beam principles, respectively, that suppress the dominant mode of SMFP-LDs. λ_0 indicates the dominant mode of SMFP-LD, λ_{i1} and λ_{i2} indicate two input beams, λ_m represents the major beam, and λ_{S1} and λ_{S2} represent the supporting beams. In Fig. 1(c), the power management of the beams for suppressing the dominant mode of the SMFP-LD is shown. P_S is the power required to suppress the dominant mode with constant wavelength detuning (the wavelength difference between the corresponding mode and the injected beam) of the input beams. P_S can be attained in different ways. Three methods to attain P_S with constant wavelength detuning are illustrated in Fig. 1(c). Figure 1(c)-(i) shows the first method of attaining P_S by injecting a beam with the equivalent power of P_S. Figure 1(c)-(ii) shows the

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second method with a combination of two inputs such that $(P_1 + P_2) \geq P_S$, but the individual power, P_1 and P_2 should be less than P_S and greater than the supporting beams P_{S1} and P_{S2}. Figure 1(c)-(iii) shows the third method with a combination of major beam (P_m) and any one of the supporting beams (P_{S1} or P_{S2}) such that either $(P_m + P_{S1}) \geq P_S$ or $(P_m + P_{S2}) \geq P_S$, but P_{S1} and P_{S2} should be less than P_m and $(P_{S1} + P_{S2}) < P_S$.

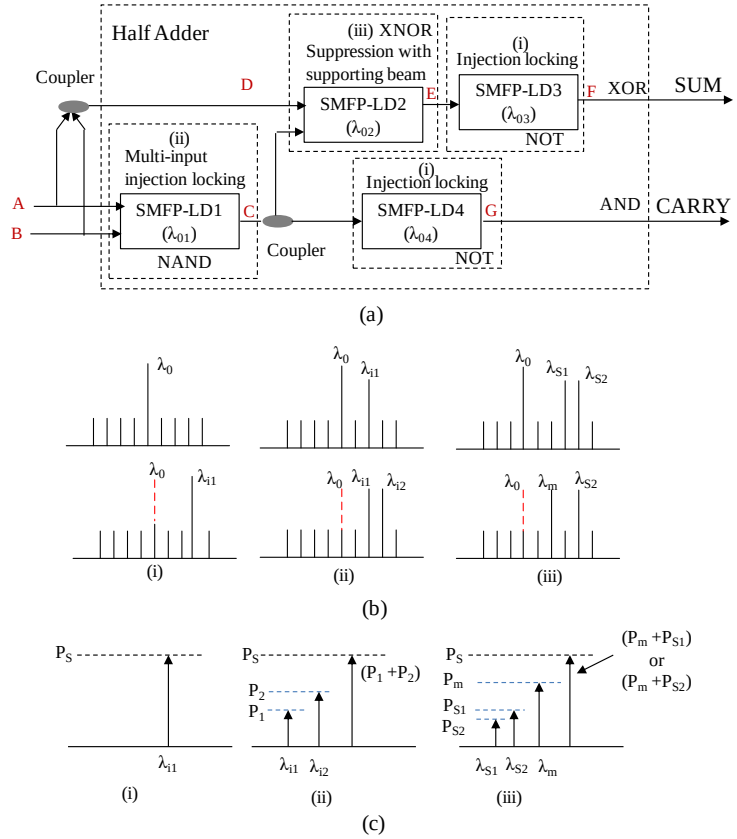

Fig. 1. (a) Block diagram of all-optical multi-logic functions. (b) Schematic of the spectrum for (i) Injection locking (ii) Multi-input injection locking (iii) Supporting beam for suppressing the dominant mode (c) Power level management for the proposed scheme.

Table 1. Truth table of the proposed logic gate and half adder.

Input 1 (A)	Input 2 (B)	NAND O/P (C)	AND O/P, CARRY (G)	XNOR O/P (G)	XOR O/P, SUM (G)
0	0	1	0	1	0
0	1	1	0	0	1
1	0	1	0	0	1
1	1	0	1	1	0

The required power, P_S, can be varied according to the wavelength detuning of the injected beams to the FP-LD [14], as the locking strength is dependent on wavelength detuning. Lower detuning requires less injected power for injection locking and higher detuning needs more input power. The SMFP-LD has a free spectral range (FSR) of about 1.16 nm. This provides flexibility regarding the choice of wavelength detuning of about 1.16

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nm. As a result, a large range in the choice of the input beams' wavelength and input beams' power levels can be achieved.

Table 1 shows a truth table of the proposed all-optical logic gates and half adder. A and B are the inputs of the logic functions; and C, G, E, and F are the outputs of the NAND, AND, XNOR, and XOR logic functions, respectively. The output of the AND logic function (G) works as a CARRY, and the output of XOR (F) works as a SUM for the proposed digital half adder. The '0' and '1' symbols indicate the logic low and logic high, respectively.

3. Experimental setup and results

Figure 2 illustrates the experimental setup for the proposed multi-logic functions and digital half adder. SMFP-LD1, SMFP-LD2, SMFP-LD3, and SMFP-LD4 are biased with a driving current of 12mA, 14mA, 12.6mA, and 10mA and are operated at a temperature of 20.1°C, 10.6°C, 22.9°C, and 14.9°C, respectively. Under these operating conditions, the SMFP-LDs are self-locked at λ_{01} (1542.78nm), λ_{02} (1541.6 nm), λ_{03} (1536.92 nm), and λ_{04} (1538.38 nm), respectively, for the logic gate operation. Input beams can be injection locked to any of the side modes of the SMFP-LD. The side modes of SMFP-LDs are observed in the range of 1535nm to 1555 nm. Hence the inputs beams can be injection locked to any of the modes within the range of 1535nm to 1555nm. In our experiment, two input beams (TL1 and TL2) are injected at wavelengths of 1550.8 nm (λ_{i1}) and 1553.1 nm (λ_{i2}) with wavelength detuning values of 0.08 nm and 0.16 nm, respectively. The polarization controllers, PC1 and PC2, are used to minimize the loss in the polarization-dependent Mach-Zehnder modulator. The input light beams are modulated with 10 Gbps Non-return-to-Zero pseudorandom bit sequences of 2^{31}-1 that are generated from an Anritsu MP1763B pulse pattern generator. PC3, PC4, and PC5 are used to allow only TE polarized beams, as only the TE mode of the light source is used to injection-lock the FP-LDs. Band pass filters (BPFs) are used to filter the dominant wavelength of the corresponding SMFP-LDs.

The power of each input beam for SMFP-LD1 is managed in such a way that the SMFP-LD1 works on the principle of multi-input injection locking. The dominant mode of SMFP-LD1 (λ_{01}) is sufficiently suppressed to be considered as logic "0" only when both input beams (A and B) are logic high ('1'); otherwise, λ_{01} will not be suppressed enough. This gives the NAND output. During our experiment, we found that the required minimum individual power for injection locking that did not suppress the dominant mode of the SMFP-LD is −12.15 dBm; the same state is maintained up to −7.61 dBm without a sufficient amount of suppression. Upon further increases in the power above −7.61 dBm, the dominant mode of the SMFP-LD starts to be suppressed. When the power of the beam reaches −5.81 dBm, the dominant mode of the SMFP-LD is suppressed at a suppression ratio of about 25 dB. On the other hand, when the power of the beam is lower than −12.15 dBm, the gain obtained by the individual beam on the respective mode is not sufficient to be considered as a logic '1'. We recorded a combined power of −4.56 dBm before optical circulator (OC1), which is sufficient to suppress the dominant mode of SMFP-LD1. The two inputs for SMFP-LD2 are from the output of SMFP-LD1 and the combination of the input beams (A and B) through a coupler (CO1) and PC5. The dominant mode of SMFP-LD2 (λ_{02}) will be suppressed only when the output from NAND (C, λ_{01}), the major beam, and either of the input beams are logic '1'. The input beams serve as a supporting beam for the major beam to suppress λ_{02}. The power of the major beam after CO2 was recorded as −6.02 dBm. Hence, a combination of any of the input beams and the major beam is sufficient to suppress the dominant mode of SMFP-LD2 (λ_{02}). This gives the XNOR logic function.

SMFP-LD3 and SMFP-LD4 work on the injection locking of FP-LD based on a single input. In our experiment, when the input beam attains a sufficient amount of power (greater than −5.81 dBm), the dominant mode of the SMFP-LD is suppressed enough to be considered as a logic '0'. This function gives the logic NOT gate. We used the NOT function at the

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outputs of the NAND and XNOR gate to obtain the logic AND and XOR gate, which are considered, respectively, as a CARRY and a SUM of the proposed digital half adder combinational block.

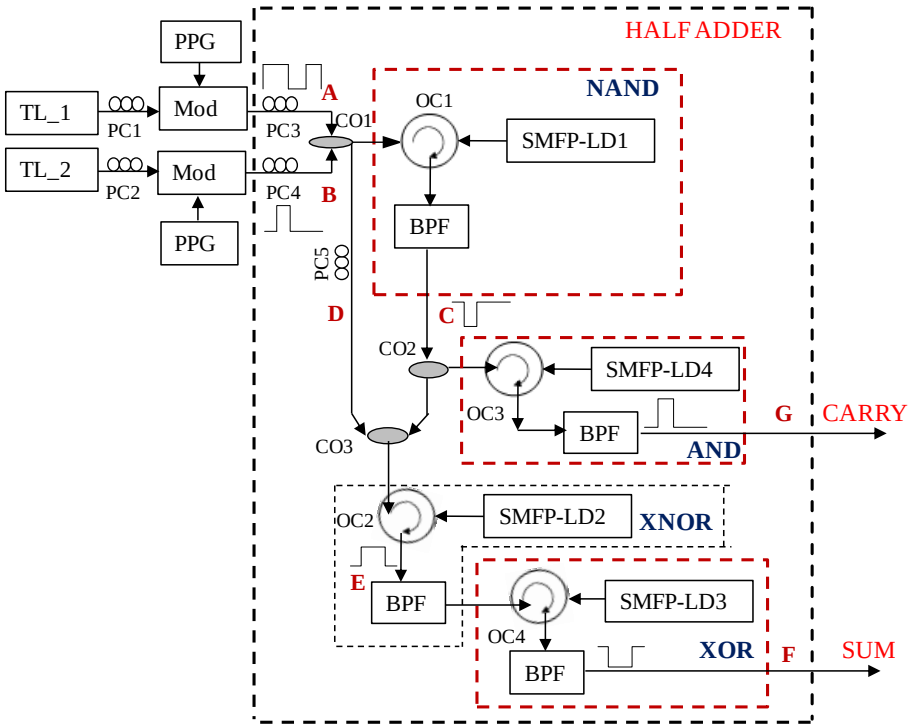

Fig. 2. Experimental set up for the multi-logic functions and digital half adder operation. TL: Tunable laser; PC: Polarization controller; PPG: Pulse pattern generator; Mod: Modulator; CO: Coupler; OC: Optical circulator; BPF: Band pass filter.

To verify the power requirement for the suppression of the dominant mode of the SMFP-LD as a function of the wavelength detuning, we changed the wavelength detuning of the input beams from 0.08 nm and 0.16 nm to 0.12 and 0.2 nm, respectively. We found that the required minimum individual power for injection locking without suppressing the dominant mode of the SMFP-LD is increased from −12.15 dBm to −11.05 dBm. When the power is less than −11.05 dBm, we found that the gain obtained by the individual beams on the respective mode is not sufficient to be considered as logic "1". In addition, the same state is maintained up to −6.21 dBm without a sufficient amount of suppression. The dominant mode of the SMFP-LD started to be suppressed above −6.21 dBm. When the power of the beam reaches −4.92 dBm, the dominant mode of SMFP-LD is suppressed with a suppression ratio of about 25 dB. It should be noted that the required power for the injection locking phenomenon of SMFP-LD with wavelength detuning of 0.12 and 0.2 nm is higher than that with wavelength detuning of 0.08 nm and 0.16 nm. This shows the amount of required power increases with an increase in wavelength detuning and the tradeoff between the wavelength and the power of the injected beams.

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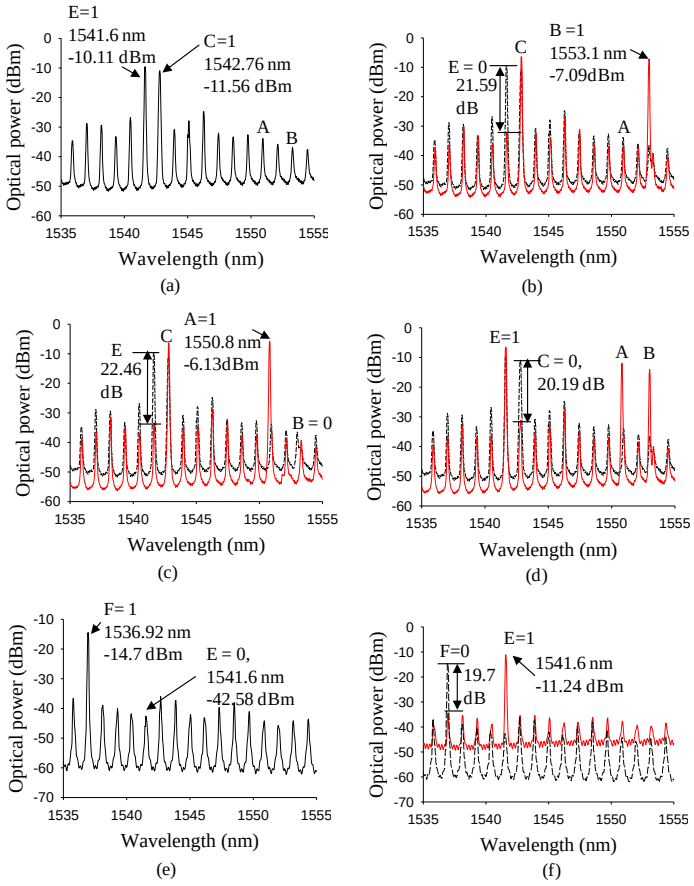

Fig. 3. Optical power spectrum traces for all-optical NAND, XNOR and inverter function using SMFP-LDs, where A and B are inputs and C is the NAND output, E is the XNOR output and F is the inverter of input E. (a) {A: B: C: E } = { 0: 0: 1: 1 }, (b) {A: B: C: E } = { 0: 1: 1: 0 }, (c) {A: B: C: E } = { 1: 0: 1: 0}, (d) {A: B: C: E } = { 1: 1: 0: 1}, (e) {E:F} = {0: 1} and (f) {E:F} = {1: 0}.

Figure 3 shows the verification of the proposed scheme in the spectrum domain taken at the output of SMFP-LD2 and SMFP-LD3 without BPFs. Figure 3(a) shows the spectrum diagram taken at point E after the circulator, OC2. In Fig. 3(a), the input beams are logic '0'. Hence, the dominant mode of SMFP-LD1 (λ_{01}) is logic '1', and this power alone is not sufficient to suppress the dominant mode of SMFP-LD2 (λ_{02}). As a result, λ_{02} is also logic '1'. In Fig. 3(b) and Fig. 3(c), the dominant mode of SMFP-LD1 is logic '1' as λ_{01} is set to be suppressed only when both the inputs are logic '1'. In this case, the dominant mode of SMFP-LD2 is logic '0' because the major beam (λ_{01}) and one of the input beams (either A or B) are logic '1'. Figure 3(d) shows the spectrum diagram taken when both inputs are logic '1'. In this case, λ_{01} is logic '0' and λ_{02} is logic '1' (because the combined power of the two input beams is not sufficient to suppress (λ_{02})). Figure 3(e) and Fig. 3(f) show the NOT function, which gives the output for the XOR gate and acts as a SUM for the half adder scheme. Similarly, implementing the NOT function of the NAND gate using SMFP-LD4, we obtain the logic AND gate, which acts as a CARRY for the half adder scheme. The suppression ratio measured in the spectrum domain for the NAND, XNOR, and XOR gates are 20.19 dB, 22.46 dB, and 19.7 dB, respectively. The little different in the suppression ratio for the different logic gates output is due to the different SMFP-LDs (SMFP-LD1, SMFP-LD2, and SMFP-LD3), and difference in the power of the input injected beams. This little difference in

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suppression ratio does not have noticeable effect on the logic level and the output of the logic gates and half adder.

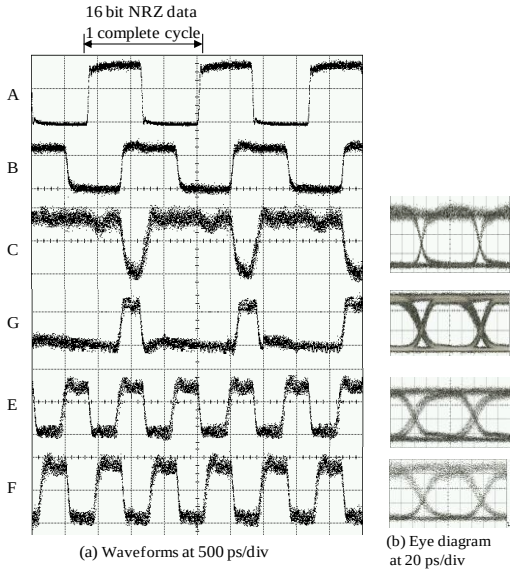

Fig. 4. Oscilloscope traces of (a) inputs (A and B) and outputs (C, G, E and F) waveform for all-optical logic gates (b) Corresponding eye diagrams.

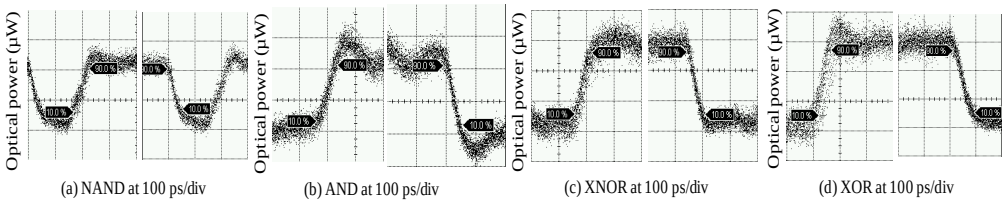

Fig. 5. Rising-falling edge of (a) the NAND gate (b) the AND gate (c) the XNOR gate and (d) the XOR gate.

The oscilloscope traces of input beams (A and B), output of NAND (C), AND (G), XNOR (E), and XOR (F) are shown in Fig. 4(a) with their respective eye diagrams in Fig. 4(b). The input A is a 16-bit 10 Gbps NRZ pulse train with a bit pattern of 1111111100000000, and input B is the delayed pattern of input A. The outputs are taken at the output of each SMFP-LD after their respective wavelength-selective BPF; thus, all other unwanted signal wavelengths are filtered out. Eye diagrams are measured with 10 Gbps PRBS 2^{31}-1 signals. We recorded the extinction ratio of individual instances of logic gate output as 12.6 dB for NAND, 14.6 dB for AND, 12.33 dB for XNOR, and 11.6 dB for XOR. The output from the logic XOR gives the SUM and the output from the logic AND gives the CARRY of the digital half adder combinational block. The waveforms and clear eye diagrams with a good extinction ratio prove the success of the proposed multi-logic functions and a digital half adder. Figure 5 shows the rising-falling edge of the demonstrated logic outputs. We measured the rising-falling time of 53 ps and 43.2 ps for NAND (Fig. 5(a)), 44.8 ps and 46 ps for AND (Fig. 5(b)), 29.6 ps and 32.3 ps for XNOR (Fig. 5(c)), and 30.8 ps and 36 ps for the XOR (Fig. 5(d)) logic gates.

Figure 6 shows the BER measurements of proposed all-optical logic functions and half adder. No any noise floor is seen up to BER of 10^{-12} which shows good performance of the

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demonstrated all-optical logic gates and half adder. We measured the maximum power penalty of 1.2 dB for XNOR gate at the BER of 10^{-9}.

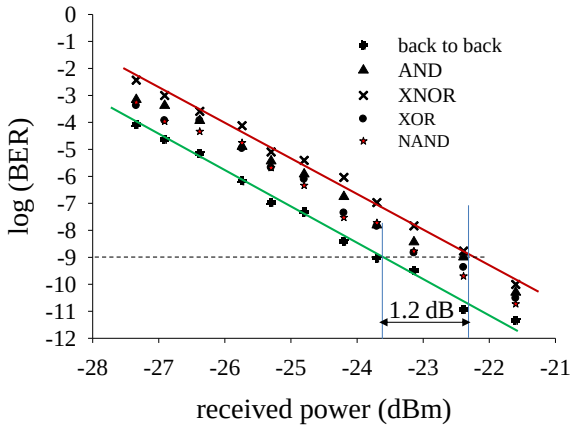

Fig. 6. BER measurements for proposed all-optical logic gates

4. Discussion and conclusion

The key issue in the implementation of these logic functions and the digital adder is the proper power management of input beams to suppress the dominant mode of the SMFP-LDs. The required amount of power to suppress the dominant mode of the SMFP-LD for a multi-input injection is obtained with the proper management of the beams' power at different stages. This power can be changed by adjusting the corresponding wavelength detuning, as the wavelength detuning and the amount of power required for suppression are proportional to each other. Based on these techniques, we set the SMFP-LD in such a way that the dominant mode is suppressed via the combination of input beams.

In this paper, we demonstrated all-optical logic functions (NAND, AND, XNOR, and XOR) and a digital half adder. The digital half adder is obtained through the output of XOR (SUM) and AND (CARRY). The output waveforms, clear eye diagrams, low rising-falling time, and BER performance demonstrate the successful operation of the proposed scheme. This work is conducted at a data rate of 10 Gbps; however, the speed can be increased to higher data rates as the speed of the SMFP-LD depends on the relaxation oscillation of solitary lasers. The theoretical and experimental relaxation oscillation frequency of Fabry-Pérot laser has been reported as 100 GHz and 72 GHz, respectively in [17]. Further, the relaxation oscillation can be increased by engineering the cavity length, the injected power and the injected current as reported in [17,18]. As we use SMFP-LDs, the proposed scheme does not require the external probe beam required in other schemes, making this module simpler and more attractive. The combined input power of −5.81 dBm, which is sufficient for logic operation, and the driving current of about 15 mA both confirm that it is efficient in terms of power. This simple configuration, low power consumption, and the low-cost approach can be implemented in future all-optical communication and optical networks for computation, decision making, header matching, and label swapping [19]. The implementation of the proposed scheme on an optical network subsystem remains as future work, while the most challenging factor connected to commercialization is the fabrication, which we will consider in our future research.

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