AIP | Applied Physics Letters

Nonvolatile memory based on sol-gel ZnO thin-film transistors with Ag nanoparticles embedded in the ZnO/gate insulator interface

Dipti Gupta, Manish Anand, Seong-Wan Ryu, Yang-Kyu Choi, and Seunghyup Yoo

Citation: Appl. Phys. Lett. **93**, 224106 (2008); doi: 10.1063/1.3041777
View online: http://dx.doi.org/10.1063/1.3041777
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v93/i22
Published by the American Institute of Physics.

Nonvolatile memory based on sol-gel ZnO thin-film transistors with Ag nanoparticles embedded in the ZnO/gate insulator interface

Dipti Gupta,[1] Manish Anand,[2] Seong-Wan Ryu,[1] Yang-Kyu Choi,[1,a)] and Seunghyup Yoo[1,b)]
[1]*Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Republic of Korea*
[2]*Department of Material Science and Engineering, Gwangju Institute of Science and Technology (GIST), Gwangju 500-712, Republic of Korea*

(Received 26 July 2008; accepted 14 November 2008; published online 5 December 2008)

A nonvolatile memory is demonstrated using a solution-processed sol-gel ZnO thin-film transistor (TFT) in which Ag nanoparticles are embedded as charge storage nodes at the insulator-ZnO interface. Its TFT transfer characteristics exhibit a large clockwise hysteresis that is proportional to the gate bias sweep range. Measurement of the threshold voltage shift versus the pulse width of gate bias reveals that the device can be programed or erased at a time scale of as short as 10^{-4} s. Retention of the initial memory window is measured to be 27% after 10^5 s and projected to last until 10^7 s. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3041777]

Reprogramable nonvolatile memory is an indispensable element in most of the modern electronic devices. While Si-based technologies are still holding the largest share of nonvolatile memory devices, a demand for an alternative memory technology is rapidly growing especially in emerging applications such as radio frequency identification tags,[1] where the conventional wafer technologies are too expensive or incompatible with the form-factor requirements such as bendability or flexibility. In these respects, memories based on organic thin-film transistors (TFTs) have been investigated as potential low-cost alternatives with a variety of fabrication routes and flexibility in choice of substrates.[1,2] However, challenges still remain in developing inexpensive encapsulation layers to protect organic devices from oxygen and moisture.[3] Another technology that is attracting a growing attention with the same motivations as organic technology is the TFTs based on oxide semiconductors such as ZnO and related compounds.[4,5] Current development of ZnO-TFTs is mainly driven by the need for reliable and scalable TFT technologies with a performance compatible with active-matrix displays,[6] but their applications are getting rapidly extended to a variety of areas because they can provide high performance as well as low cost, high environmental stability, and even optical transparency.[4,5,7]

A memory device is also an example of the areas that can benefit from the aforementioned advantages of ZnO-TFTs. The first memory device based on ZnO-TFTs was recently reported by Noh *et al.*[8] in top-gate geometry based on rf-sputtered ZnO channel and gate insulators consisting of polymeric/ferroelectric bilayers. While their work is based on the ferroelectric technology, another technology typically used in metal-oxide-semiconductor field-effect transistor (MOSFET) memory devices is based on isolated nanoscale objects such as metal/semiconductor nanoparticles (NPs)[9–11] or nanotubes[12] that are embedded into gate insulators. Such nano-objects function as the charge storage nodes that trap or detrap charges depending on the applied gate bias and thus effectively shift the threshold voltage, which in turn results in hysteresis in the transfer characteristics. This kind of scheme is popular because it can be used with well-established gate insulators and because some of the memory properties are controllable by NP density or multistacked NP layer configuration, etc.[13] From the perspectives of low-cost processing, it would also be highly beneficial if major processes can be done using a solution process so that electronic devices can eventually be made by printing. Here we demonstrate reprogramable nonvolatile memory devices by solution processing of sol-gel ZnO as semiconducting layers and Ag-NPs as charge storage nodes in TFT geometry, where Ag-NPs are embedded into the interface between ZnO channels and gate insulators.

Figure 1(a) shows the schematic structure of the ZnO/Ag-NP memory TFT under study. The memory TFT was fabricated on the heavily doped *n*-type (100) Si wafers having a 100 nm thick thermally grown SiO_2 gate dielectric. Here the Si acts also as the back-gate electrode. A stable dispersion of Ag-NPs was prepared by mixing $AgNO_3$ (0.03M) and polyvinyl pyrollidine (PVP) (0.003M) in dimethylformamide (DMF). Here PVP and DMF act as a stabilizing agent and reducing agent for the silver salt, respectively.[14] A solution of ZnO precursor was prepared

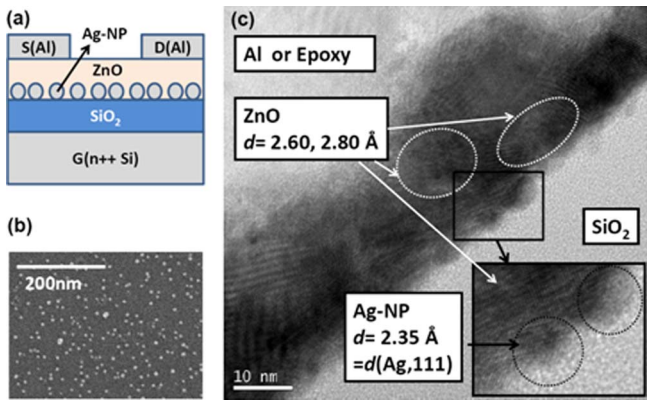

FIG. 1. (Color online) (a) Schematic of the ZnO/Ag-NP memory TFT and (b) SEM image of the Ag NPs on SiO_2 surface after removing the organics by heating. (c) Cross-sectional HRTEM image of the fabricated device featuring Ag-NPs embedded at the SiO_2–ZnO interface.

a)Electronic mail: ykchoi@ee.kaist.ac.kr.
b)Electronic mail: syoo@ee.kaist.ac.kr.

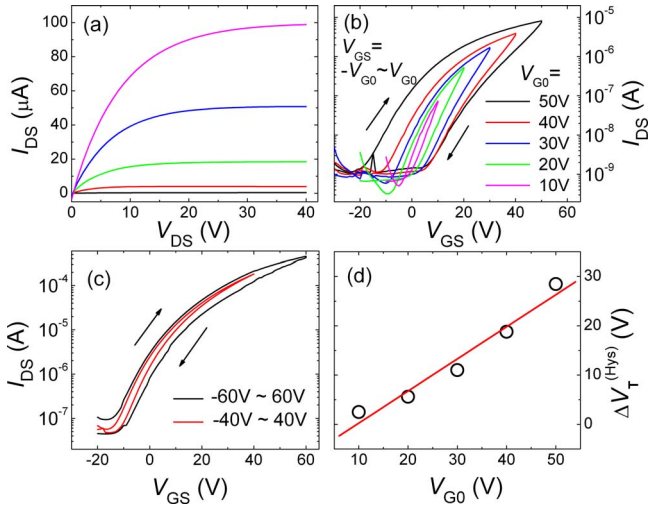

FIG. 2. (Color online) (a) Output characteristics of ZnO/Ag-NP memory TFT with V_{GS} of 0, 10, …, 40 V and (b) transfer characteristics of the same device demonstrating the clockwise hysteresis for the range of gate bias V_{GS} from $-V_{G0}$ to V_{G0} (vice versa) with V_{G0} of 10, 20, …, 50 V and V_{DS} of 3 V. (c) Transfer and hysteresis characteristics of the ZnO-TFTs without Ag-NPs at V_{DS} of 30 V. (d) The hysteresis window ($\Delta V_T^{(hys)}$) vs V_{G0} (circles) and the linear fit (line) result.

based on a sol-gel method by making a 0.5M solution of zinc acetate in the solvent mixture of DMF and methoxyethanol (volume ratio=3:2) as described by Farley *et al.*[15] The prepared dispersion of Ag-NPs was spin coated on the SiO_2 dielectric followed by a thermal annealing at 500 °C for 1 h in a furnace to remove the organic compounds and reorganize the Ag-NPs on the SiO_2 surface. The ZnO precursor solution was then spin coated on the substrate twice followed by thermal annealing at 500 °C for 1 h in a furnace. The typical thickness of ZnO film was approximately 30 nm after the annealing process. Following the deposition of the active ZnO layer, the 100 nm thick aluminum was then thermally evaporated through a shadow mask to form source and drain electrodes with the nominal width W of 1.0 mm and the channel length of 50 μm. The completed devices then went through electrical characterization in ambient air. Memory characteristics were cautiously measured following the standard method used in the established MOSFET memory technologies[9,12] in terms of the threshold voltage shift ΔV_T because ΔV_T is the parameter that directly reflects the change in stored charges.

The scanning electron microscopic (SEM) image shown in Fig. 1(b) indicates that the spin coating of Ag-NP dispersion and the subsequent annealing process described above result in a distribution of isolated Ag-NPs with the areal density of $1.4\times10^{11}/\mathrm{cm}^2$ and the particle size in the range of 3–11 nm. The cross-sectional high-resolution transmission electron microscopy (HRTEM) image of a fabricated device shown in Fig. 1(c) indicates that Ag-NPs, which can be identified as circular domains with the crystalline d spacing typical of Ag,[16] are in fact embedded between SiO_2 and ZnO layers without being disturbed by the annealing process for ZnO layer.

The transistor output characteristics are shown in Fig. 2(a), featuring an n-type enhancement-mode operation typical of ZnO TFTs.[17] By applying the standard MOSFET equations to its transfer characteristics, the saturation mobility (μ_{sat}) is extracted to be 0.75 $\mathrm{cm}^2/\mathrm{V\,s}$. The on/off current ratio is in the range of 10^3–10^4. To verify the feasibility as memory devices of ZnO-Ag NP TFTs, the transfer characteristics were measured for the various sweep ranges of gate voltage V_{GS} in both forward ($-V_{G0}$ to $+V_{G0}$) and reverse ($+V_{G0}$ to $-V_{G0}$) directions, at a drain voltage (V_{DS}) of 3 V, as shown in Fig. 2(b). A clear clockwise hysteresis characterized by the positive hysteresis window $\Delta V_T^{(hys)}$ ($\equiv V_{T,reverse} - V_{T,forward}$) is found for all the sweep ranges tried, which is attributed to the electron/hole trapping in the Ag-NPs during the positive/negative voltage sweep.[8–10] Comparing with the reference device with no Ag-NPs that exhibits a low $\Delta V_T^{(hys)}$ of only 1.5 V [see Fig. 2(c)], the device with Ag-NPs shows the relatively large $\Delta V_T^{(hys)}$ up to 28.5 V at V_{G0} of 50 V, confirming that the presented memory TFT operates through the electrostatic charging and discharging of the Ag-NPs rather than the interface between ZnO and SiO_2 layers itself.[18] Figure 2(d) shows that a linear relationship between $\Delta V_T^{(hys)}$ and V_{G0} can be established, which is in fact equivalent to the relationship between the number of charges stored in the Ag-NPs per unit area ($\equiv N_Q$) and ΔV_T given by[19]

$$qN_Q = C_{SiO_2}\Delta V_T^{(hys)}, \tag{1}$$

where C_{SiO_2} ($=3.5\times10^{-8}$ $\mathrm{F/cm}^2$) is the capacitance per unit area of the SiO_2 layer and q is the electronic charge. For instance, $\Delta V_T^{(hys)}$ of 28.5 V at V_{GS} sweep with V_{G0} of 50 V corresponds to the situation where approximately $6.3\times10^{12}/\mathrm{cm}^2$ charges are captured on the Ag-NPs in total. Using $1.4\times10^{11}/\mathrm{cm}^2$ as the areal density of the Ag-NPs, one can estimate that the average number of charges per Ag-NP is approximately 46. This threshold voltage change and the corresponding number of stored charges per NP are relatively large when compared to conventional MOSFET memory with NPs embedded into gate insulators[9,10] but are comparable to those of the memory devices reported by Novembre *et al.*[11] that are based on pentacene and Au-NPs in a device geometry similar to the devices presented here. The major difference from the conventional devices appears to come from the lack of well-defined tunnel-oxide layer in the present work and Ref. 11.

In order to evaluate the programing (P) capability of this ZnO/Ag-NP memory TFT, the shift in threshold voltage ΔV_T measured with respect to the initial unprogramed value V_{Ti} was measured as a function of a hold time (τ_P) of pulsed programing gate voltages with the amplitudes $V_{GS}^{(P)}$ of +40, +50, and +60 V, respectively. Subsequently, erasing (E) characteristics were measured by monitoring ΔV_T as a function of a hold time τ_E for erasing pulse with the amplitudes $V_{GS}^{(E)}$ of −40, −50, and −60 V, respectively. Note that ΔV_T right before programing and erasing operations are 0 V [$\equiv\Delta V_T(t_i^{(P)})$] and 17.8 V [$\equiv\Delta V_T(t_i^{(E)})$], respectively. It is expected that the programing pulse of the positive gate bias will let a portion of the induced electrons be captured at Ag-NPs. Then, those captured electrons will function like interface fixed charges that eventually results in the V_T shift in the positive V_{GS} direction.[20] Upon application of "erasing" pulse of the negative gate bias, some or all of the precaptured electrons will now be detrapped, resulting in the V_T shift in the negative V_{GS} direction. [See Fig. 3(a) for the illustration comparing the number of the induced carriers between "programed" and "erased case," which is directly related to the V_T shift.] As shown in Fig. 3(b), the magnitude of $[\Delta V_T(\tau^{(P/E)}) - \Delta V_T(t_i^{(P/E)})]$ increases with both the pulse dura-

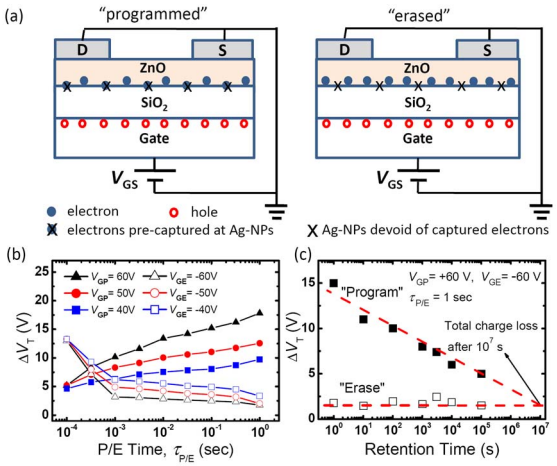

FIG. 3. (Color online) (a) Illustration showing the difference in the number of the induced electrons for the same gate bias V_{GS} between the programed and erased state, which is directly related to the shift in V_T. For example, programed memory TFT requires a larger V_{GS} to induce the same number of electrons in channels compared to erased or unprogramed memory TFTs, resulting in the positive V_T shift. (b) Program/erase (P/E) characteristics of ZnO/Ag-NP memory TFTs, showing the threshold voltage shift ΔV_T on applying pulses with the amplitudes $V_G^{(P/E)}$ of +40/−40 V, +50/−50 V, and +60/−60 V, respectively, and (c) its charge retention characteristics after applying a P/E pulse of +60/−60 V for 1 s.

tion $\tau_{P/E}$ and the magnitude of $V_G^{(P/E)}$. Note that the difference in ΔV_T even at the shortest pulse width $\tau_{P/E}$ of 10^{-4} s is +5.0/−4.6 V in average, which is large enough to be sensed. Hence, it may be considered that ZnO/Ag-NP memory TFTs can potentially be used as fast-operating memories.

As another substantial factor that characterizes the nonvolatile memory devices, the retention characteristics were studied by measuring ΔV_T of the device as a function of time after applying a $V_G^{(P/E)}$ stress of +60/−60 V for 1 s. The charge retention characteristics shown in Fig. 3(b) indicate that the memory window, that is, a difference in ΔV_T between the programing and erasing operations, decreases over time, for example, to 27% of the initial value after a period of 10^5 s. From the extrapolation of the experimental data, it is projected that after programing, the device can retain the initial memory window up to 10^7 s. This rather rapid decrease in the memory window is mainly attributed to the low energy barrier for charge backflow from Ag-NPs to ZnO. While the difference in energy between the work function of Ag and the conduction band edge of ZnO is only of the order of 0.1 eV, the previous reports indicate that the potential barrier height between the Ag and the ZnO is in the range of 0.8–0.9 eV when they are contacted together.[21,22] This barrier height would prevent the backflow and provide some retention as shown in this work, but this may be further improved by applying a tunnel-oxide structure similar to Si-based memory devices[8–10] or by using NPs with a higher work function that can create higher energy barrier for the charge backflow.

In summary, sol-gel ZnO based memory TFTs were fabricated using solution processes with Ag-NPs embedded as charge storage nodes at the insulator-ZnO interface. Pulsed operation indicates that they can be programed or erased to yield measurable threshold voltage shift at a timescale of as short as 0.1 ms. Charge retention characteristics are currently poorer than the established memory technologies, but we believe that a barrier engineering can lead to a further improvement in retention characteristics. With such refinement and development of reliable dielectric technologies that can be prepared by an inexpensive process compatible with various substrates, ZnO-memory TFTs presented here may serve as reliable building blocks for low-cost memory technologies not only in various established applications but also in new emerging systems such as memory-on-panel displays[23] and transparent electronic devices.[4]

This work was supported by the Brain Korea 21 project, School of Information Technology, KAIST, 2008, by the ERC program of the Korea Science and Engineering Foundation (KOSEF) grant funded by the Korea Ministry of Education, Science and Technology (MEST) (Grant Nos. R11–2007–045–01001–0 and R11–2007–045–03004–0), and by the KOSEF grant funded by the same (Grant No. R01–2007–000–11023–0).

[1] J. C. Scott and L. D. Bazano, Adv. Mater. (Weinheim, Ger.) **19**, 1452 (2007).
[2] R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, and D. M. De Leeuw, Nature Mater. **4**, 243 (2005).
[3] J. S. Lewis and M. S. Weaver, IEEE J. Sel. Top. Quantum Electron. **10**, 45 (2004).
[4] J. F. Wager, Science **300**, 1245 (2003).
[5] Y. Sun and J. A. Rogers, Adv. Mater. (Weinheim, Ger.) **19**, 1897 (2007).
[6] J.-S. Park, J. K. Jeong, H.-J. Chung, Y.-G. Mo, and H. D. Kim, Appl. Phys. Lett. **90**, 262106 (2007).
[7] J. Sun, D. A. Mourey, D. Zhao, S. K. Park, S. F. Nelson, D. H. Levy, D. Freeman, P. Cowdery-Corvan, L. Tutt, and T. N. Jackson, IEEE Electron Device Lett. **29**, 721 (2008).
[8] S. H. Noh, W. Choi, M. S. Oh, D. K. Hwang, K. Lee, S. Im, S. Jang, and E. Kim, Appl. Phys. Lett. **90**, 253504 (2007).
[9] H. I. Hanafi, S. Tiwari, and I. Khan, IEEE Trans. Electron Devices **43**, 1553 (1996).
[10] S. Kolliopoulou, P. Dimitrakis, P. Normand, H.-L. Zhang, N. Cant, S. D. Evans, S. Paul, C. Pearson, A. Molloy, M. C. Petty, and D. Tsoukalas, J. Appl. Phys. **94**, 5234 (2003).
[11] C. Novembre, D. Guerin, K. Lmimouni, C. Gamrat, and D. Vuillaume, Appl. Phys. Lett. **92**, 103314 (2008).
[12] S. W. Ryu, X. J. Huang, and Y. K. Choi, Appl. Phys. Lett. **91**, 063110 (2007).
[13] J.-S. Lee, J. Cho, C. Lee, I. Kim, J. Park, Y.-M. Kim, H. Shin, J. Lee, and F. Caruso, Nat. Nanotechnol. **2**, 790 (2007).
[14] I. Pastoriza-Santos and L. M. Liz-Marzán, Pure Appl. Chem. **72**, 83 (2000).
[15] N. R. S. Farley, C. R. Staddon, L. Zhao, K. W. Edmonds, B. L. Gallagher, and D. H. Gregory, J. Mater. Chem. **14**, 1087 (2004).
[16] d=0.235 nm for (111) direction. Joint Committee on Powder Diffraction Standards, File No. 04–0783.
[17] B. S. Ong, C. Li, Y. Li, Y. Wu, and R. Loutfy, J. Am. Chem. Soc. **129**, 2750 (2007).
[18] Another possibility is that migration of Ag atoms into SiO_2 and subsequent creation of deep-level states, which can also function as charge storage nodes. Identification of the exact mechanisms will require further studies such as temperature-dependent measurement. Authors are currently in preparation for such study, and results will be reported elsewhere.
[19] V. Podzorov and M. Gershenson, Phys. Rev. Lett. **95**, 016602 (2005).
[20] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (Wiley, New Jersey, 2006), pp. 319–388.
[21] M. W. Allen, M. M. Alkaisi, and S. M. Durbin, Appl. Phys. Lett. **89**, 103520 (2006).
[22] H. Sheng, S. Muthukumar, N. W. Emanetoglu, and Y. Lu, Appl. Phys. Lett. **80**, 2132 (2002).
[23] H.-T. Chen, S.-I. Hsieh, C.-J. Lin, and Y.-C. King, IEEE Electron Device Lett. **28**, 499 (2007).