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Fabrication and room-temperature characterization of a silicon self-assembled quantum-dot transistor

B. H. Choi and S. W. Hwang[a)]
Department of Electronics Engineering, Korea University, Sungbukku, Anamdong, Seoul 136-701, Korea

I. G. Kim and H. C. Shin
Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Yusonggu, Kusongdong, Taejon 305-701, Korea

Yong Kim and E. K. Kim
Semiconductor Materials Research Center, Korea Institute of Science and Technology, P.O. Box 131, Cheongryang, Seoul 130-650, Korea

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A quantum-dot transistor based on silicon self-assembled quantum dots has been fabricated. The device shows staircases and oscillations in the drain current at room temperature. These data are interpreted as due to single electron tunneling through the dots located in the shortest current path between the source and the drain electrodes. The dot size calculated from the data is ~7 nm, which is consistent with the size of the self-assembled dots incorporated in the transistor. © *1998 American Institute of Physics.* [S0003-6951(98)02147-0]

Single electron tunneling and its application to various electronic devices have been studied extensively for more than a decade.[1] Recently, there have been a lot of breakthroughs for the fabrication of single electron transistors (SETs) operating at room temperature. Most of the room temperature SETs reported so far[2–5] have been based on silicon (Si) technologies, except a few devices fabricated by scanning tunneling microscope nano-oxidation of metals.[6,7] The well-established Si technologies have made it possible to reliably generate ultrasmall quantum dots. On the other hand, a quantum-dot transistor based on silicon will have full integration capability with other conventional Si devices.

Other than the nanolithographic definition, an interesting way of forming ultrasmall quantum dots is resorting to self-assembled growth techniques. Recently, a floating gate memory incorporating such Si self-assembled quantum dots (SAQDs) has been successfully demonstrated.[8] However, a switching device using Si SAQDs has not been reported.

In this letter, the fabrication and the characterization of a quantum-dot transistor utilizing Si SAQDs have been reported. A few number of Si SAQDs with the diameter of 8–10 nm are selected by the deposition of ultrasmall metal pads with the gap $\leqslant$30 nm. The current–voltage characteristics measured from the fabricated quantum-dot transistor exhibit staircases and oscillatory features at room temperature.

The Si SAQDs used in the work have been grown in a conventional low pressure chemical vapor deposition reactor with 20% diluted silane (SiH_4) source. The growth temperature and the time are 620 °C and 15 s, respectively. These conditions have been obtained from the optimization procedures for the spontaneous decomposition and assembly of the dots.[9–11] The substrate for SAQDs is a thermally grown SiO_2 layer with the thickness of 300 nm, on a (100) *p*-type Si wafer. Figure 1(a) shows the top view of Si SAQDs. The diameter of the dots ranges from 8 to 10 nm and the average dot density is estimated to be 3.85×10^{11} cm^{-2}. Several aluminum (Al) pads with nanometer dimensions are deposited using standard *e*-beam lithography and liftoff procedures. Figure 1(b) shows an overview of the quantum-dot transistor. The sharp-edged Al pads with the gap $\leqslant$30 nm are used as the source and the drain electrode and the larger pad is the side gate for the dot potential control. The backside of the substrate has been contacted and been used as the back gate. Figure 1(c) shows the magnified image of the source and the drain pads. Simultaneous focusing of the Si dots and the metal pads is impossible due to the height difference. However, it is expected from the dot density that there are at most three quantum dots in the shortest path (along the maximum electric field line) between the source and the drain pads. The current–voltage characteristics between the source and the drain ($I_{DS}-V_{DS}$), the side-gate bias (V_{GS}) characteristics, and the back-gate bias (V_{BS}) characteristics have been measured using an HP 4155 parameter analyzer. The device has been shielded in the box which has been modified from an HP 16442A test fixture.

Figure 2 shows the $I_{DS}-V_{DS}$ and the differential conductance–voltage ($dI_{DS}/dV_{DS}-V_{DS}$) obtained from the transistor of Fig. 1 at room temperature. Clear staircases with the periodicity of 0.27 V can be seen both in the $I_{DS}-V_{DS}$ and in the $dI_{DS}/dV_{DS}-V_{DS}$ traces. Figure 3 shows the $I_{DS}-V_{BS}$ traces at several values of V_{DS}'s. The current oscillations are noticeable in the data of $V_{DS}=10$ and 30 mV and the magnitude of the oscillations becomes negligible when $V_{DS}=100$ mV. Neglecting small noisy peaks in the data, the periodicity of the oscillation is 0.56 V when $V_{DS}=10$ mV and 0.52 V when $V_{DS}=30$ mV. The current oscillations are observed also in the $I_{DS}-V_{GS}$ characteristics (Fig. 4). In the case of V_{GS} scans, the gate leakage current is comparable to I_{DS} when $V_{GS}\geqslant1.6$ V. In the range $0.8<V_{GS}<1.6$ V, where the leakage current is negligible, the amplitude of the oscillations in the case of $V_{DS}=100$ mV becomes smaller than in

[a)]Electronic mail: swhwang@kuccnx.korea.ac.kr

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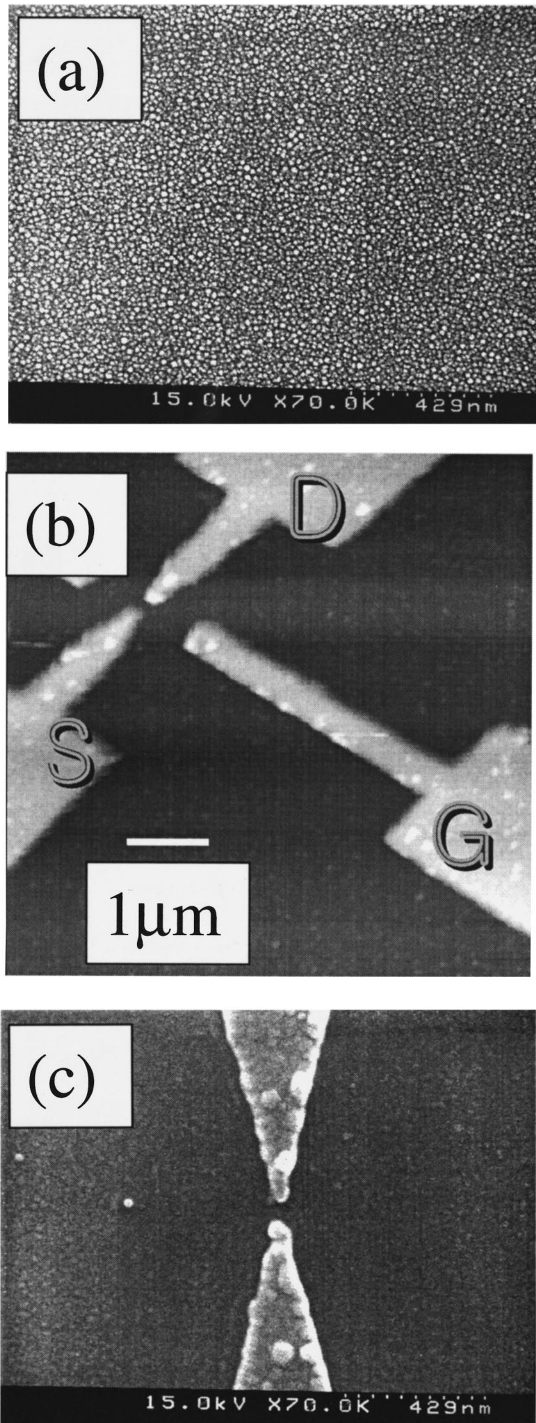

FIG. 1. (a) Scanning electron micrograph of self-assembled poly-Si quantum dots. (b) Atomic force microscope image of the quantum dot transistor fabricated by depositing several Al arms with nanometer sizes. (c) Magnified view of the active region of the quantum dot transistor.

the case of $V_{DS}=10$ and 50 mV. The strength of the oscillations in the range $V_{GS}\geqslant 1.6$ V does not diminish even when $V_{DS}=100$ mV. However, the same periodicity of 0.16 V persists in all the ranges of V_{GS}.

From the periodicity of the staircases, the sum of the junction capacitances of the dot, C_D+C_S is found to be 0.296 aF. The gate coupling capacitance C_G from the V_{GS} oscillation period is 0.285 aF and the back-gate coupling capacitance C_B from the V_{BS} oscillation is 1.01 aF. As a

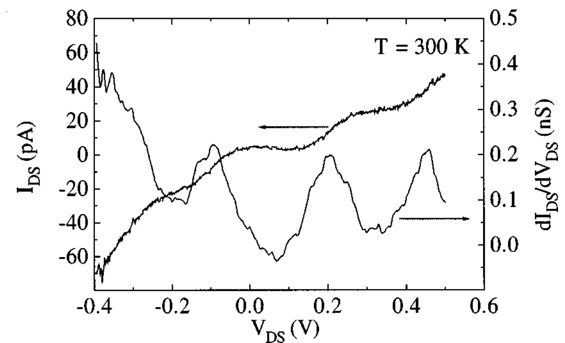

FIG. 2. $I_{DS}-V_{DS}$ and $dI_{DS}/dV_{DS}-V_{DS}$ characteristics measured from the quantum dot transistor at room temperature.

result, the total self-capacitance of the dot $(C_D+C_S+C_G+C_B)$ is 1.59 aF, which leads to the dot diameter of 7.3 nm. It is consistent with the average dot diameter observed in the scanning electron micrographs.

From the average dot density of 3.85×10^{11} cm^{-2}, the average dot-to-dot distance is estimated to be ~16 nm. Since the gap between the drain and the source electrode is approximately twice larger than the dot-to-dot distance, there is a possibility that the observed data are originated from a more complicated configuration of more than one dot, in the maximum electric field region between two sharp-edged pads. In the case of multiple dots, the oscillations in I_{DS} would show multiple periods if the gate-coupling capacitance of one dot is different from those of the others.[12] In our case, only one period is observed in the oscillations. The location of the gate in our transistor is much farther than the dot-to-dot distance. Furthermore, the sizes of the dots participating in the transport are expected to be uniform as can be seen in Fig. 1(a). These result in the same gate-coupling capacitance value for each dot, and thus, a single-period oscillation. The final point is whether Coulomb staircase can be seen in a multiple dot topology. A recent experiment[13] and calculation[14] suggest that Coulomb staircases are observable in the multiple dot structure when the variations in the dot size and the junction capacitance value are small, such as in our case.

The main difference between the back gate and the side gate is that the side gate is directly connected to the source and the drain electrode by many dots on the substrate. In the bias region where the side gate leakage current is comparable to I_{DS}, a current path consisting of a large number of dots

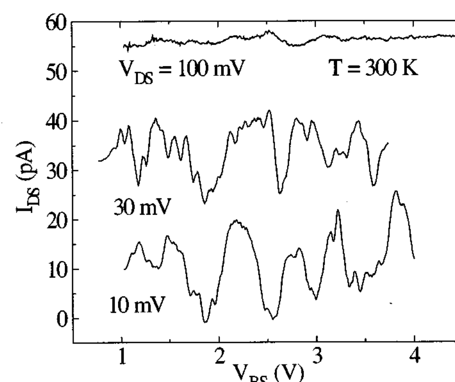

FIG. 3. $I_{DS}-V_{GS}$ characteristics at several different V_{DS} values.

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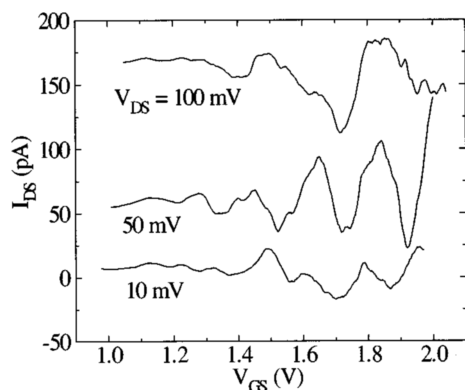

FIG. 4. $I_{DS}-V_{BS}$ characteristics at several different V_{DS} values.

and tunnel junctions between the side gate and the source electrode can be open. However, the oscillations in I_{DS} persist since the side gate still performs potential modulation of the dots.

In conclusion, the quantum-dot transistor incorporating Si SAQDs has been fabricated. The $I_{DS}-V_{DS}$, the $I_{DS}-V_{BS}$, and the $I_{DS}-V_{GS}$ characteristics measured from the transistor at room temperature have been interpreted as due to single electron tunneling through a small number of quantum dots between the drain and the source electrode.

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