Sub-5nm All-Around Gate FinFET for Ultimate Scaling

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Abstract

Sub-5nm all-around gate FinFETs with 3nm fin width were fabricated for the first time. The n-channel FinFET of sub-5nm with 1.4nm HfO_2 shows an I_{Dsat} of 497μA/μm at V_G=V_D=1.0V. Characteristics of sub-5nm transistor are verified by using 3-D simulations as well as analytical models. A threshold voltage increases as the fin width reduces by quantum confinement effects. The threshold voltage shift was fitted to a theoretical model with consideration of the first-order perturbation theory. And a channel orientation effect, based on a current-flow direction, is shown.

Key words: all-around gate, FinFET, sub-5nm, quantum effect

Introduction

Silicon-based transistors are scaled down continually in order to increase a density and speed. Multi-gate FinFETs have strengths of high robustness on short-channel effects (SCEs) and superior scalability using conventional processes [1-7]. However, the ultimate minimum feature-sized device operating at room temperature has been expected to be 1.5nm according to Heisenberg's uncertainty principle and *Shannon-von Neumann-Landauer* expression [8]. The fabricated sub-5nm all-around gate (AAG) FinFET is approaching to this fundamental limit. Table 1 summarizes the performance of sub-10nm devices: a bulk single-gate [3], an ultra-thin body single-gate [4], a double-gate FinFET [5], an omega FET [6], and a nanowire FinFET [7]. For ultimately scaled transistor, AAG FinFET is known to be the best structure to provide scalability and flexibility in device design [9]. This work primarily focuses on feasibility and scalability of sub-5nm AAG FinFET. A threshold voltage shift by quantum confinement and an effect of current-flow direction are reported.

Fabrications

Fig. 1 illustrates a process flow of AAG FinFET. As a starting material, (100) SOI wafers were used. 100nm silicon film was thinned down to 14nm by using thermal oxidations and HF wet etch. Dual-resist process for a fin and a gate patterning was used to define nanometer features by e-beam lithography and non-critical large-area patterns by optical lithography. After the silicon-fin etch, a sacrificial oxide was grown and removed to alleviate etching damages. Gate dielectrics were split into 1.4nm HfO_2 by atomic layer deposition and 2nm thermal SiO_2. Reasonable characteristics of sub-5nm devices were achieved in HfO_2 group. 30nm in-situ n^+ poly-silicon was deposited for the gate electrode. The gate was patterned by the dual-resist process, similarly. After the gate and spacer formation, arsenic ions were implanted to form the source and drain (S/D). 1000℃ spike annealing was utilized to activate the dopants of S/D. Finally, forming gas annealing at 450℃ was applied. Metallization was skipped for iterative annealing to optimize gate-to-S/D overlap. The fabricated device dimensions are sub-5nm gate length (L_G), averaged 3nm fin width (W_{Fin}), and 14nm fin height (H_{Fin}).

Results and Discussions

Fig. 2 shows a SEM top-view of 3nm silicon-fin and sub-5nm gate. Fig. 3 and Fig. 4 show TEM cross-sectional views of 3nm silicon-fin (a-a' direction of Fig. 2 inset) and sub-5nm gate on the silicon-fin (b-b' direction of Fig. 2 inset) with 1.4nm HfO_2. Fig. 5 shows C-V plot of HfO_2 and its inset shows gate current densities. An equivalent oxide thickness (EOT) of HfO_2 was extracted by using a dual-frequency technique [10] and verified by a simulation with consideration of quantum effects. The estimated EOT of 1.4nm HfO_2 was 1.2nm including 0.9nm interfacial oxide (IFO). NMOS I_D-V_G, g_m-V_G, and I_D-V_D of sub-5nm AAG FinFET with 3nm W_{Fin} are shown in Fig. 6 and Fig. 7. An on-state current is 497μA/μm at V_G=V_D=1.0V in Fig. 6, which is normalized by all-arounded channel perimeter: H_{Fin} and W_{Fin}. Due to the process limitation of gate dielectric (EOT=1.2nm), the device shows a large drain induced barrier lowering (DIBL=230mV/V) and subthreshold swing (SS=208mV/dec) in spite of all-around gate structure. Measured I_D-V_G plot was compared and matched with 3-D SILVACO simulation (effective gate length, L_{eff}= 5nm). Fig. 8 shows SS for various W_{Fin}, L_G, and L_d (drain potential decay length), which govern the SCEs [11]. A scaling factor (L_{eff}/L_d) was 3 for relatively thick EOT (1.2nm) even in the AAG natures. However, as the EOT scales down to 0.6nm, the factor tends to be unity, which satisfies a criterion of SS, 100mV/dec. A threshold voltage (V_T) roll-off with various W_{Fin} is shown in Fig. 9. A significant improvement on SCEs was achieved at a narrow fin device due to the increment of gate controllability [12]. The V_T shift by quantum confinement effects becomes significant as W_{Fin} decreases [13]. If the potential well composed of both gate dielectric barrier heights and the conduction band is assumed to be a parabolic shape, the measured V_T shift in Fig. 10 agrees to the analytical model, which is newly developed with consideration of the first order perturbation theory. Detailed analytical model is represented in the inset of Fig. 10. Fig. 11 shows a channel orientation effect of the on-state current according to the current-flow direction: 0°, 15°, and 30°. Due to a vertical nature of FinFET, the device lies in (110) plane at 0° but in (100) plane at 45° rotated device. The on-state current is expected to increase with the rotated angle increment because of the enhancement of electron mobility [14]. However, the measured on-state current decreases as the angle increases [15].

Conclusions

The sub-5nm all-around gate FinFETs were fabricated, the smallest silicon-based transistors. This report shows feasibility to continue the Moore's law beyond the sub-5nm. The device performances were compared and verified by 3-D simulation. The threshold voltage shift is analytically modeled and the on-state current dependence on the current-flow direction is reported.

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References

[1] Y.-K. Choi *et al., IEDM*, p.421, 2001. [2] T. Park *et al., VLSI*, p.135, 2003. [3] H. Wakabayashi *et al., IEDM*, p.989, 2003. [4] B. Doris *et al., IEDM*, p.631, 2003. [5] B. Yu *et al., IEDM*, p.251, 2002. [6] C. Jahan *et al., VLSI*, p.112, 2005. [7] F.-L. Yang *et al., VLSI*, p.196, 2004. [8] V. V. Zhirnov *et al., Proc. of IEEE*, vol.91, no.11, p.1934, 2003. [9] S. D. Suk *et al., IEDM*, p.735, 2005. [10] Z. Luo *et al., EDL*, vol.25, no.9, p.655, 2004. [11] G. Pei *et al., TED*, p.1411, vol.49, no.8, p.1411, 2002. [12] Q. Chen *et. al., TED*, vol.50, no.7, p.1631, 2003. [13] Q. Chen et al., IEEE Int. Conf. on SOI, p.183, 2003. [14] B. Doris *et al., VLSI*, p.86, 2004. [15] J. Wang *et al., IEDM*, p.537, 2005.

Structure	Bulk SG	UTB SG	DG FinFET	Omega FET	Nano-wire	This work
	Ref [3]	Ref [4]	Ref [5]	Ref [6]	Ref [7]	
Dielectric	SiON	SiON	SiO_2	HfO_2	SiO_2	HfO_2
L_G [nm]	5	6.5	10	10	10	5
W_{Fin} [nm]		8	10	10	10	3
EOT [Å]	12	12	17	19.2	19	12
V_{DD} [V]	0.4	1.2	1.2	1.2	1.0	1.0
I_{ON} [μA/μm]	37	260[1)]	446	326	522	497
DIBL[mv/V]	1400[1)]	104[1)]	71	130	80	230
SS	300[1)]	90	125	90	75	208

[1)] Estimated value

Table 1. Comparison of sub-10nm transistors with bulk single-gate (SG), ultra-thin body (UTB) single-gate, double-gate (DG) FinFET, Omega FET, and nanowire FinFET.

- **Body thinning**
- **Fin patterning**
- **Sacrificial oxidation**
- **Gate dielectric (HfO_2 vs. SiO_2)**
- **N^+ Poly-silicon deposition**
- **Gate etching**
- **Spacer formation**
- **Source/Drain implantation**
- **Spike annealing (1000°C)**
- **Forming gas annealing (450°C)**

Fig. 1. Process flow of all-around gate FinFET.

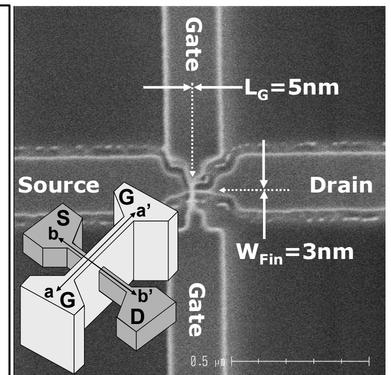

Fig. 2. SEM top-view of 3nm silicon-fin and sub-5nm gate. The schematic shows all-around gate FinFET.

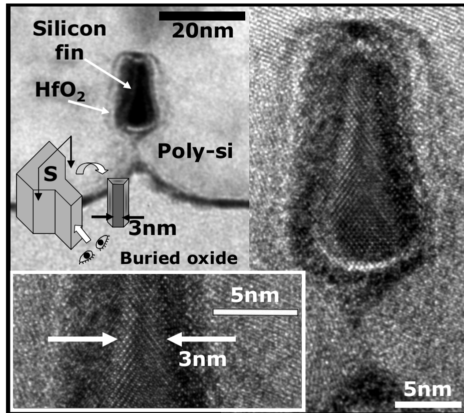

Fig. 3. TEM cross-sectional view of 3nm silicon-fin with 1.4nm HfO_2. The fin is all-arounded by the gate. A blurry boundary shows source(S) extension region.

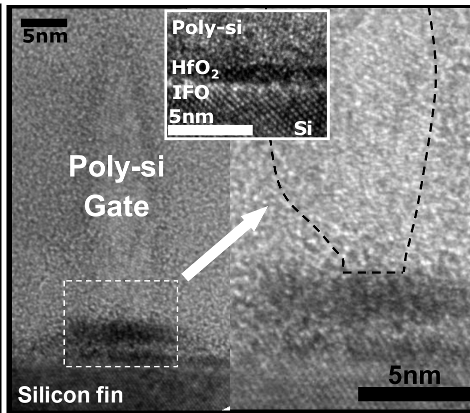

Fig. 4. TEM cross-sectional view of sub-5nm n^+ poly-silicon gate on the silicon-fin. Inset shows Silicon/IFO/HfO_2/Poly-silicon before spike annealing.

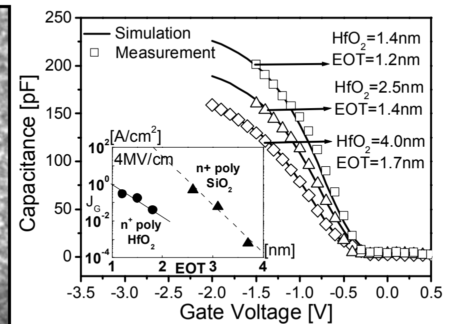

Fig. 5. Capacitance versus gate voltage with measurement and simulation data. EOT of 1.2nm was estimated from 1.4nm HfO_2. Gate current density versus EOT of HfO_2 and SiO_2 with n^+ poly-silicon is shown in inset.

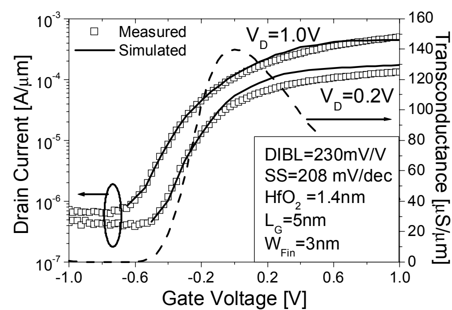

Fig. 6. Subthreshold I_D-V_G, from measurement and 3-D simulation, and g_m-V_G characteristics of L_G=5nm, W_{Fin}=3nm, and HfO_2=1.4nm (EOT=1.2nm).

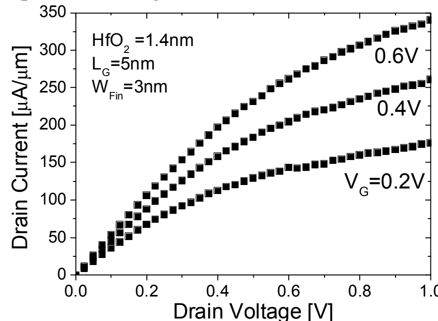

Fig. 7. I_D-V_D characteristics of L_G=5nm, W_{Fin}=3nm, and HfO_2=1.4nm (EOT=1.2nm). Current is normalized by channel perimeter.

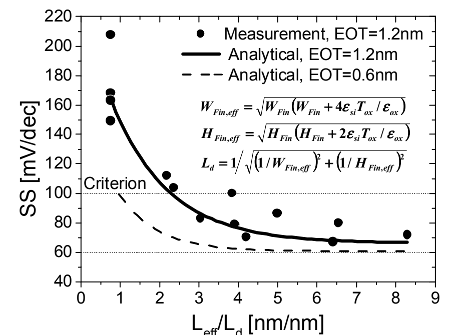

Fig. 8. Subthreshold swing for various W_{Fin} and L_G with EOT 1.2nm HfO_2. L_d is a drain potential decay length which characterizes the short channel effects.

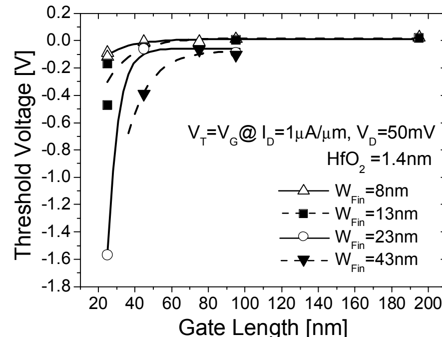

Fig. 9. V_T versus L_G with different W_{Fin}: 8nm, 13nm, 23nm, and 43nm. Improved V_T-roll off of the narrow fin device is achieved by enhanced gate controllability.

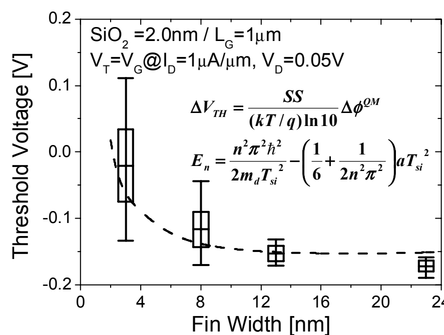

Fig. 10. V_T versus W_{Fin} of L_G=1 μm with 2nm SiO_2. The shift of V_T due to quantum confinement is shown with measurement and analytical model data.

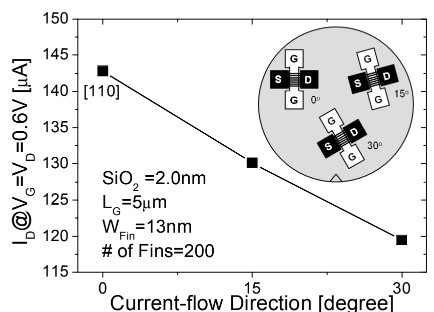

Fig. 11. On-state current versus channel rotation angle from 0° to 30°. Measured current decreases as the rotation angle increases.