Spread Spectrum Clock Generator with Delay Cell Array to Reduce the EMI from a High-Speed Digital System

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Abstract—In high-speed digital systems, most of the EMI from the system is caused by high-speed digital clock drivers and synchronized circuits. In order to reduce the EMI from the system clocks, spread spectrum clock (SSC) techniques that modulate the system clock frequency have been proposed. A conventional spread spectrum clock generator with a phase locked loop (SSCG-PLL) has been implemented by controlling a period jitter. However, the conventional SSCG-PLL becomes more difficult to implement at higher clock frequencies, in the GHz range, because of the random period jitter of the PLL. Furthermore, the attenuation of EMI is decreased due to the random period jitter of the PLL. To overcome these problems associated with the random period jitter, we propose a spread spectrum clock generator with a delay cell array (SSCG-DCA), which controls the position of clock transitions. Measurement and simulation have demonstrated that the proposed SSCG-DCA is easier to implement and more effective in attenuating the EMI compared with the conventional SSCG-PLL. The proposed SSCG-DCA was implemented on a chip using a 0.35μm CMOS process and achieved a 9dB attenuation of the EMI at 390MHz.

Keywords-Spread Spectrum Clock;Delay Cell Array;EMI

I. INTRODUCTION

In high-speed digital systems, clock drivers and associated circuits generate most of the EMI problems in the system. This is because of the periodic nature of signal with the highest frequency and fast transition time. Its energy is concentrated in narrow bands near the harmonic frequencies. In order to reduce the EMI from the system clock drivers and associated circuits, spread spectrum clock (SSC) techniques that modulate the system clock frequency have been introduced [1]. Recently, the SSC techniques have been applied to some commercial electronic products, such as a personal computer, offering considerable suppression of the EMI [2].

The conventional SSC is generated by adding intentional period jitter to a fixed period clock within the timing margin of the system. The shape of the imposed period jitter is defined as a modulation profile. The attenuation (A_{dB}) of spectrum is the suppressed EMI by virtue of the SSC. There are various modulation profiles including random pulses, sinusoidal, triangular, and SSCG modulation profiles. If we don't consider the RBW of a spectrum analyzer, the triangular modulation profile makes most effective attenuation of EMI [1], [3], [5].

When the triangular modulation profile is used, A_{dB} can be estimated by [4]. In the region between the cut-off frequency (f_m/δ) and the overlap frequency (f_0/δ), A_{dB} is directly proportional to the peak deviation (δ) and the harmonic frequency ($n \cdot f_0$), and inversely proportional to the modulation frequency (f_m). The peak deviation (δ) is equal to the maximum period jitter (ΔT_0) divided by the fundamental period T_0 and the modulation frequency f_m is the reciprocal of the modulation period ($T_m = K \cdot T_0$). In order to achieve the maximum attenuation, the peak deviation (δ) should be increased and the modulation frequency (f_m) should be decreased.

The deviation from ideal timing of a clock is called jitter. It comprises both deterministic and random components. Also it can be classified into a period jitter or an edge jitter as shown in Figure 1, depending on the timing reference from which it is defined. The period jitter is defined as a deviation of a period at each clock cycle from an ideal fixed period. On the other hand, the edge jitter is defined as a deviation of a transition edge at each clock cycle from an ideal fixed clock transition edge position. According to this definition, the period jitter is equal to the difference of successive edge jitters, and the edge jitter is equal to the summation of the period jitter.

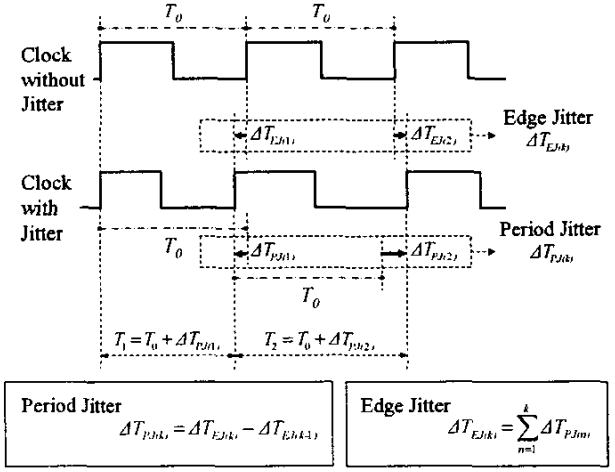


Figure 1. Jitter Definition. 'Period Jitter' and 'Edge Jitter' representation for SSC. The period jitter is the difference between period of every clock cycle and the fundamental period (T_0). The edge jitter is the difference between the transition edge of every clock cycle and their ideal position.

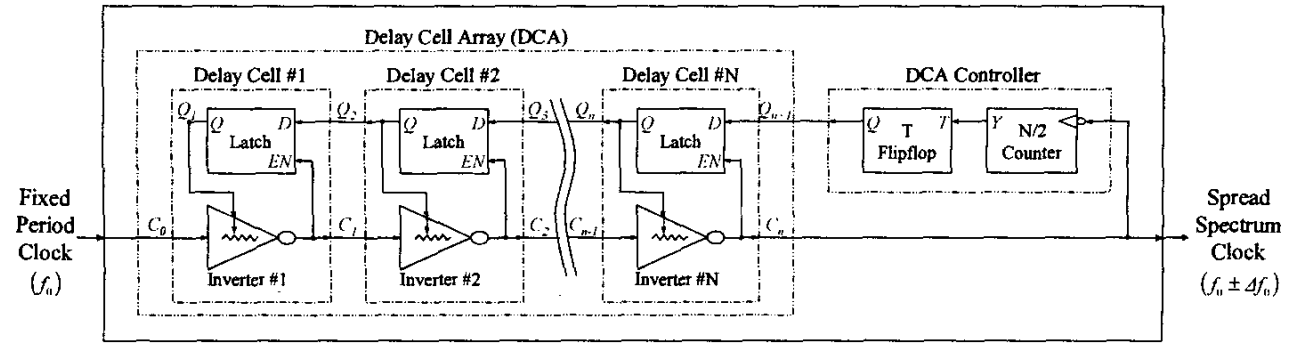


Figure 2. Proposed Spread Spectrum Clock Generator with Delay Cell Array (SSCG-DCA). The SSCG-DCA is composed of delay cell array and DCA controller. The DCA has N numbers of delay cell. The delay cell is composed of an inverter with controllable propagation delay and a latch.

A SSCG is realized by adding an intentional jitter to a fixed period clock within the timing margin of the system. In addition to the intentionally added jitter, that is, the SSC jitter, there are also an unintentional jitter such as a random jitter. The unintentional jitter results from crosstalk, simultaneous switching noise (SSN), EMI, and design errors. If the SSCG is carefully designed, the unintentional jitter can be reduced to be negligible but the random jitter still exists due to thermal noise, shot noise, or flicker noise. This random jitter poses critical limit on the performance of the conventional SSCG based on modulation of the period jitter of the PLL.

Most conventional SSCGs have been implemented using a phase locked loop (PLL) controlling the period jitter rather than the edge jitter [2]. The SSC period jitter is intentionally added to a fixed period clock by using a programmable counter and a VCO. However, the conventional SSCG-PLL has two critical problems, namely, (i) difficulty of implementation, and (ii) decrement of A_{dB} due to random period jitter. As clock frequency increases the SSC period jitter must be more finely controlled. If the SSC period jitter to be controlled becomes smaller than the random period jitter, implementation of the SSCG-PLL becomes difficult. Furthermore, in these circumstances, A_{dB} also decreases [5].

In this paper, a spread spectrum clock generator with a delay cell array (SSCG-DCA) is proposed in order to control the edge jitter with a triangular modulation profile and maximize the attenuation of the EMI in the SSCG. The proposed SSCG-DCA is more robust in that it is less affected by the random jitter. It is clearly demonstrated by measurement and simulation that the proposed SSCG-DCA has a more effective attenuation of the EMI and can be more easily implemented than the conventional SSCG-PLL. The proposed SSCG-DCA was implemented on a chip using a 0.35μm CMOS process and achieved a 9dB attenuation of the EMI at 390MHz.

II. Proposed Spread Spectrum Clock Generator with Delay Cell Array (SSCG-DCA)

The proposed spread spectrum clock generator is composed of a DCA and a DCA controller as shown in Figure 2. The DCA has N delay cells and each delay cell is composed of an inverter and a latch. The propagation delay of the inverter at each cell is controlled by the latch output Q. Hence, depending on the status of Q's on the N cells, the propagation delay of each clock transition will be different, resulting in the controlled edge jitter.

Figure 3 shows the operation of a delay cell. The clock signal is transferred to the next delay cell with a propagation delay dependent on the status of Q. The propagation delay at the n^{th} delay cell, PD_n is represented in (1). The additional propagation delay (ΔD_n) is the difference between two propagation delays according to the status of Q_n and causes the edge jitter. The SSC is constructed using this edge jitter. The total propagation delay through the DCA (PD_{DCA}), which is represented in (2), is composed of constant term, as given by (3), and edge jitter term, as given by (4). The SSC is created by the edge jitter (ΔT_{EJ}) that depends on Q_n.

$$PD_n = D_n + Q_n \cdot \Delta D_n \tag{1}$$

$$PD_{DCA} = \sum_{n=1}^{N} PD_n = \sum_{n=1}^{N} (D_n) + \sum_{n=1}^{N} (Q_n \cdot \Delta D_n) \tag{2}$$

$$PD_{CONST} = \sum_{n=1}^{N} (D_n) \tag{3}$$

$$\Delta T_{EJ} = \sum_{n=1}^{N} (Q_n \cdot \Delta D_n) \tag{4}$$

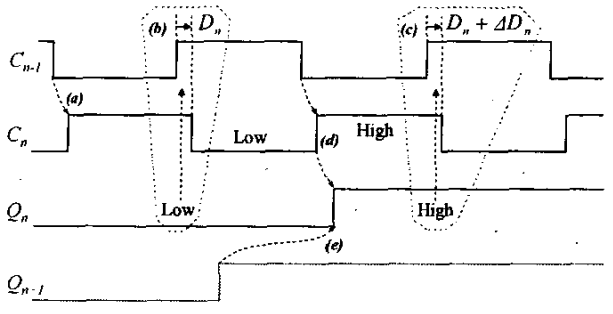


Figure 3. Operation of a delay cell. Clock C_{n-1} is inverted and propagated to C_n with some propagation delay shown as (a). If Q_n is low, Q_n=0, the propagation delay between C_{n-1} and C_n is D_n shown as (b). If Q_n is high, Q_n=1, the propagation delay is $D_n+\Delta D_n$ shown as (c). If C_n is high shown as (d), Q_{n-1} is transferred to Q_n shown as (e). The spread spectrum clock is generated using the edge jitter resulting from the additional propagation delay ΔD_n.

Q_n is transferred from a delay cell to the previous delay cell as shown in Figure 3. For normal operation, the status of all Q maintain 0 (low state) and in every clock transition edge, Q is charged with 1 (high state) one by one from a delay cell to the previous delay cell. After every cell is charged with 1 (high state), charging with 0 (low state) will be repeated again.

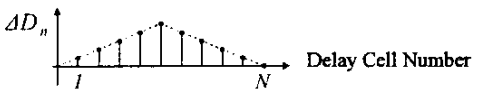
The propagation delay of the k^{th} transition edge of a fixed period clock through the DCA is represented by (5). Therefore, the edge jitter ($\Delta T_{EJ(k)}$) is as shown in (6) and the period jitter is as shown in (7).

$$PD_{DCA(k)} = PD_{CONST} + \Delta T_{EJ(k)} \tag{5}$$

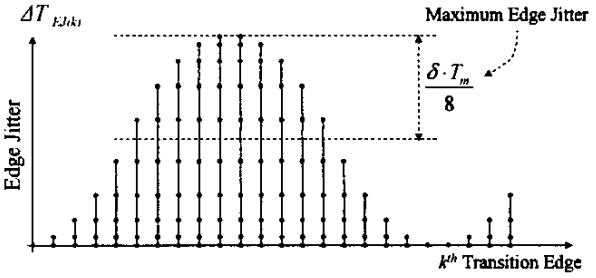
$$\begin{pmatrix} \Delta T_{EJ(1)} \\ \Delta T_{EJ(2)} \\ \Delta T_{EJ(3)} \\ \cdots \\ \Delta T_{EJ(N)} \\ \Delta T_{EJ(N+1)} \\ \Delta T_{EJ(N-2)} \\ \cdots \\ \Delta T_{EJ(2N-2)} \\ \Delta T_{EJ(2N-1)} \\ \Delta T_{EJ(2N)} \end{pmatrix} = \begin{pmatrix} \Delta D_N \\ \Delta D_{N-1} + \Delta D_N \\ \Delta D_{N-2} + \Delta D_{N-1} + \Delta D_N \\ \cdots \\ \Delta D_1 + \Delta D_2 + \cdots + \Delta D_{N-2} + \Delta D_{N-1} + \Delta D_N \\ \Delta D_1 + \Delta D_2 + \cdots + \Delta D_{N-2} + \Delta D_{N-1} \\ \Delta D_1 + \Delta D_2 + \cdots + \Delta D_{N-2} \\ \cdots \\ \Delta D_1 + \Delta D_2 \\ \Delta D_1 \\ 0 \end{pmatrix} \tag{6}$$

$$\Delta T_{PJ(k)} = \Delta T_{EJ(k)} - \Delta T_{EJ(k-1)} = \begin{pmatrix} \Delta T_{PJ(1)} \\ \Delta T_{PJ(2)} \\ \Delta T_{PJ(3)} \\ \cdots \\ \Delta T_{PJ(N)} \\ \Delta T_{PJ(N+1)} \\ \Delta T_{PJ(N+2)} \\ \cdots \\ \Delta T_{PJ(2N-2)} \\ \Delta T_{PJ(2N-1)} \\ \Delta T_{PJ(2N)} \end{pmatrix} = \begin{pmatrix} \Delta D_N \\ \Delta D_{N-1} \\ \Delta D_{N-2} \\ \cdots \\ \Delta D_1 \\ -\Delta D_N \\ -\Delta D_{N-1} \\ \cdots \\ -\Delta D_3 \\ -\Delta D_2 \\ -\Delta D_1 \end{pmatrix} \tag{7}$$

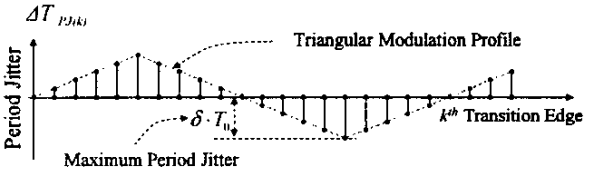
The proposed SSCG-DCA with a triangular modulation profile can be implemented as shown in Figure 4. If the additional propagation delay (ΔD_n) of each delay cell is designed as Figure 4(a), the edge jitter is determined as 4(b) and the period jitter is extracted as 4(c). Therefore, for the implementation of a SSC with a triangular modulation profile using the proposed SSCG-DCA, the additional propagation delay (ΔD_n) should be designed as shown in Figure 4(a). The maximum period jitter is determined by equation as shown in Figure 4(c) and the maximum edge jitter is determined by equation as shown in Figure 4(b). For example, supposing the fundamental frequency (f_0) is 100MHz, the modulation frequency (f_m) is 50kHz, and peak deviation (δ) is 0.01 (1%), the fundamental period (T_0) is 10ns, the maximum period jitter is 100ps, and the maximum edge jitter is 25ns. The maximum edge jitter is larger than the fundamental period as well as the maximum period jitter.



(a) Additional Propagation Delay at every Delay Cell



(b) Edge Jitter of Spread Spectrum Clock



(c) Period Jitter of Spread Spectrum Clock

Figure 4. "SSC Edge Jitter" and "SSC Period Jitter" of the proposed SSCG-DCA. (a) The additional propagation delay (ΔD_n) of every delay cell. (b) The SSC edge jitter. (c) The SSC period jitter. If the additional propagation delay has a triangular profile, the modulation profile of the SSCG-DCA is triangular.

III. COMPARISON OF THE PROPOSED SSCG-DCA AND THE CONVENTIONAL SSCG-PLL

In this chapter, the proposed SSCG-DCA is compared with the conventional SSCG-PLL. The conventional SSCG-PLL is implemented by controlling the SSC period jitter and the proposed SSCG-DCA is implemented by controlling the SSC edge jitter as shown in Figure 5. If the random edge jitter and the random period jitter do not exist, the spread spectrum clock from the SSCG-DCA will be same as that from the SSCG-PLL. However, because of the difference between the random period jitter in the SSCG-PLL and the random edge jitter in the SSCG-DCA, the spread spectrum clock from the SSCG-DCA is quite different from that from the SSCG-PLL.

Effects of the random period jitter in the SSCG-PLL and the random edge jitter in the SSCG-DCA were demonstrated using the numerical simulation in terms of attenuation of the EMI. The period and edge jitters of the SSCG-PLL and the SSCG-DCA are calculated, respectively. The random period jitter of the SSCG-PLL is on right of Figure 5 and the random edge jitter of the SSCG-DCA is on left of Figure 5 and both have the same gaussian distribution. The random period jitter that results in the random edge jitter of the SSCG-DCA is larger than the random period jitter of the SSCG-PLL. Because 25ns of the maximum edge jitter is much larger than 10ps of the maximum period jitter, the proposed SSCG-DCA is easier to implement than the conventional SSCG-PLL.

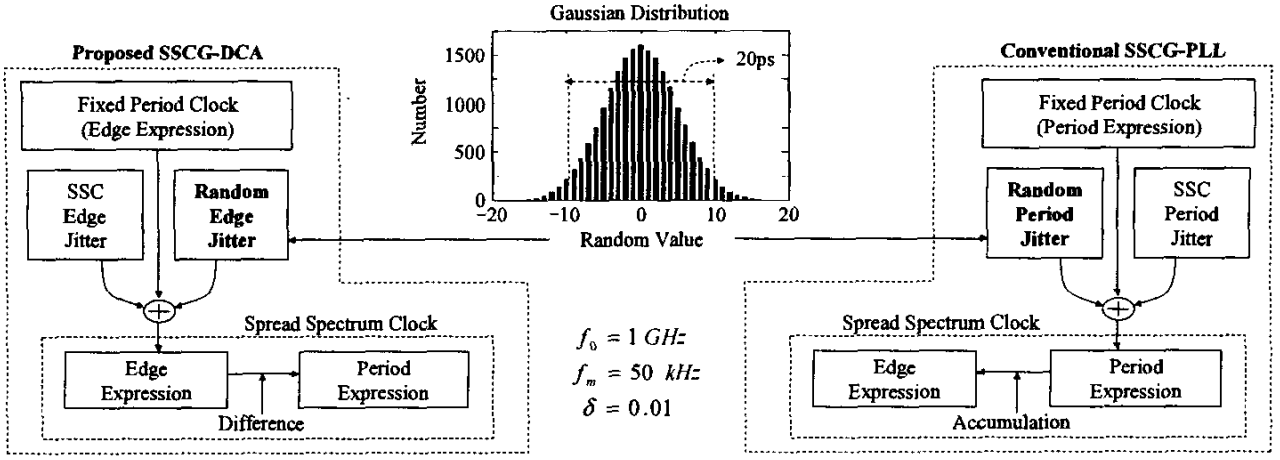


Figure 5. Principles of the proposed spread spectrum clock generator with delay cell array (SSCG-DCA) and the conventional spread spectrum clock generator with phase locked loop (SSCG-PLL). For the generation of SSC, either the edge jitter or the period jitter should be controlled. The proposed SSCG-DCA is implemented by the SSC edge jitter (ΔT_{EJit}) in the left figure. The conventional SSCG-PLL is implemented by the SSC period jitter (ΔT_{PJit}) in the right figure. The relation between the SSC period jitter and the SSC edge jitter is representated in figure 1. The random period jitter in the right figure and the random edge jitter in the left figure have Gaussian distribution.

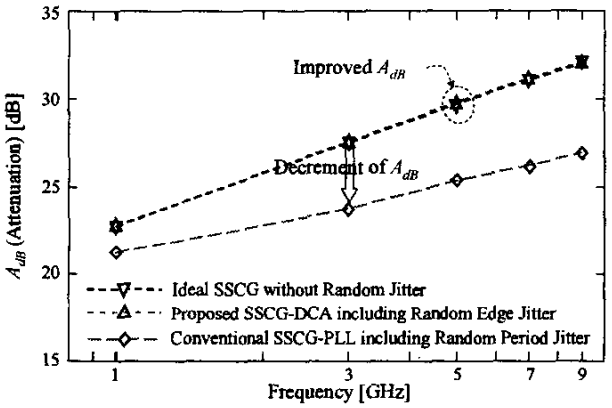


Figure 6. Attenuation from the SSCG-PLL and the SSCG-DCA. The attenuation from the SSCG-PLL decreased than that from the SSCG without random jitter. However, the attenuation from the SSCG-DCA is larger than the attenuation from the SSCG-PLL and is similar to the attenuation from the SSCG without the random jitter.

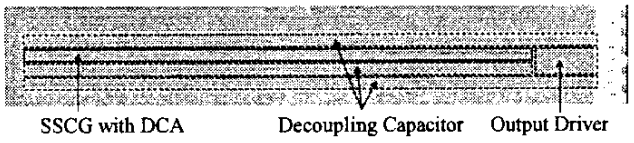
The simulated A_{dB} of the SSCG-PLL decreased as shown in Figure 6. This problem is called the 'decrement of A_{dB}'. However, the proposed SSCG-DCA has greater effective attenuation than the conventional SSCG-PLL. Although the SSCG-DCA has the larger period jitter, the A_{dB} of the SSCG-DCA is larger than the A_{dB} of the SSCG-PLL and is comparable to the A_{dB} of the ideal SSCG without random jitter. The decreased A_{dB} is caused by the huge amount of random edge jitter in the SSCG-PLL. The crucial problematic jitters are random period jitter in the SSCG-PLL and random edge jitter in the SSCG-DCA. Because the random edge jitter is the cumulative summation of the random period jitter, the random edge jitter resulting from random period jitter of the SSCG-PLL is much larger than the random edge jitter of the SSCG-DCA. Therefore, the proposed SSCG-DCA has more effective attenuation than the conventional SSCG-PLL.

If the clock frequency is increased further, the maximum SSC period jitter of the SSCG-PLL becomes comparable to its random period jitter. If the maximum SSC edge jitter is much larger than the SSC period jitter, as well as the random edge jitter, the proposed SSCG-DCA can be more easily implemented than the conventional SSCG-PLL. In addition, because the random edge jitter, which results from the accumulated random period jitters of the SSCG-PLL, is much larger than the random edge jitter of the SSCG-DCA, the proposed SSCG-DCA has more attenuation than the conventional SSCG-PLL.

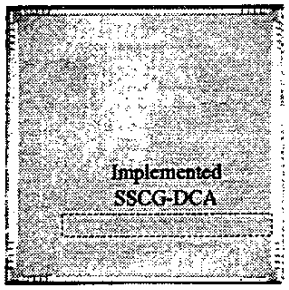
IV. Measurement of Jitter and EMI

The fabricated IC chip, package, and architecture are shown in Figure 7. The number of delay cells is 200. The size of MOS transistor is not optimized. For more simplified circuit diagram, a multiplexer instead of both a counter and a T-flip flop is used for the DCA controller. The operating fundamental frequency is approximately 100MHz. The IC chip was fabricated using 1-poly, 3-metal, and 0.35μm CMOS process, with 5mm x 5mm die size. The size of the implemented SSCG-DCA is 3400μm x 90μm. The power consumption is approximately 120mW for the 200 delay cells at 100MHz clock frequency. For power integrity, a 1nF on-chip decoupling capacitor was used.

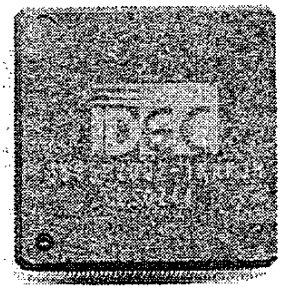
The simulated edge jitter is shown in Figure 8(a). The maximum edge jitter is observed at 3600ps. The simulated period jitter is shown in Figure 8(b). The maximum period jitter is observed at 250ps. The modulation profile is not an exact triangular modulation profile but a SSCG modulation profile. The spectrum of clock waveform was evaluated using the Fast Fourier Transform (FFT) as shown in Figure 8(c). The voltage spectrum of the fixed period clock is approximately 120dBμV at 500MHz and that of the spread spectrum clock is approximately 110dBμV at 500MHz. This 10dB attenuation of voltage spectrum means a 10dB reduction of EMI at 500MHz.



(a) SSCG-DCA, on-chip decoupling capacitor, and output driver

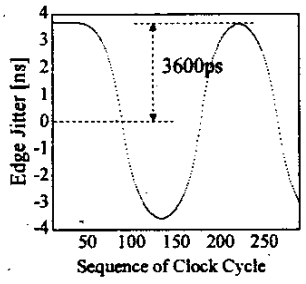


(b) Fabricated IC chip

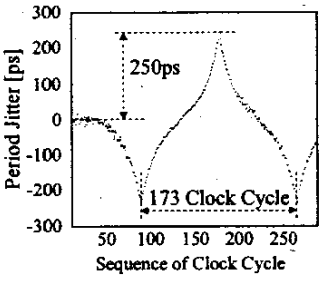


(c) Package (208 PQFP)

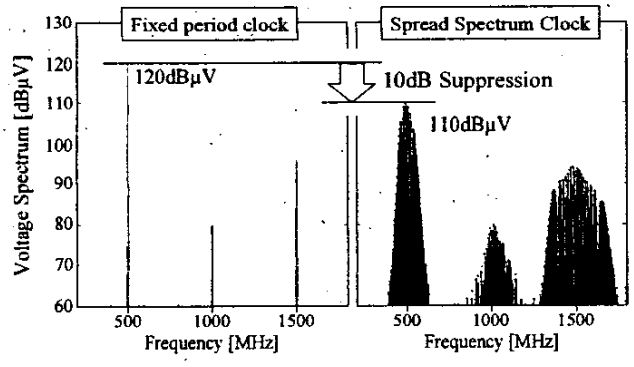
Figure 7. Implemention of the proposed Spread Spectrum Clock Generator with Delay Cell Array (SSCG-DCA). (a) Architecture of the SSCG-DCA (b) Fabricated IC chip (c) Packaged IC chip



(a) Simulated Edge Jitter



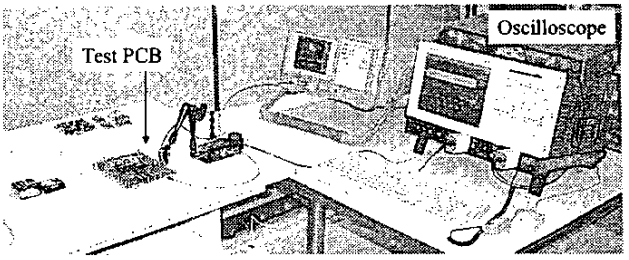
(b) Simulated Period Jitter



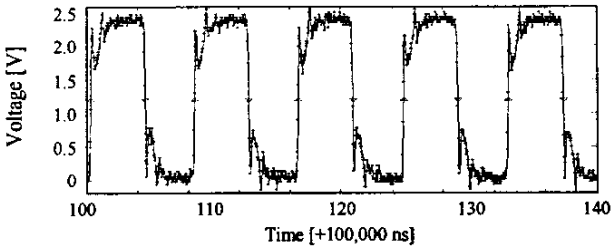
(c) Simulated spectra from the implemented SSCG-DCA

Figure 8. Simulation for the Implemented SSCG-DCA. (a) Simulated edge jitter. (b) Simulated period jitter. The edge jitter (a) and the period jitter (b) are extracted from simulated spread spectrum clock waveform. (c) Simulated spectra of the fixed period clock and the spread spectrum clock from the implemented SSCG-DCA.

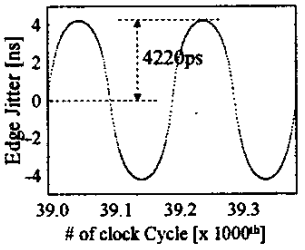
Figure 9(a) is the measurement setup for spread spectrum clock waveform using the oscilloscope's single shot technique. The oscilloscope used is Tektronix TDS7404 that has 50ps sampling time and 8MByte of memory. Using the measured SSC waveform as shown in Figure 9(b), the edge jitter as 9(c) and the period jitter as 9(d) were extracted. The measured jitter



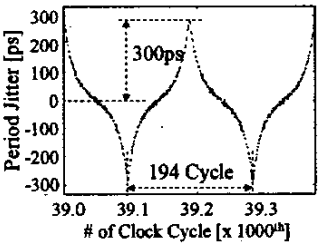
(a) Measurement setup for jitter of the implemented SSCG-DCA



(b) Spread Spectrum Clock of the implemented SSCG-DCA



(c) Measured Edge Jitter



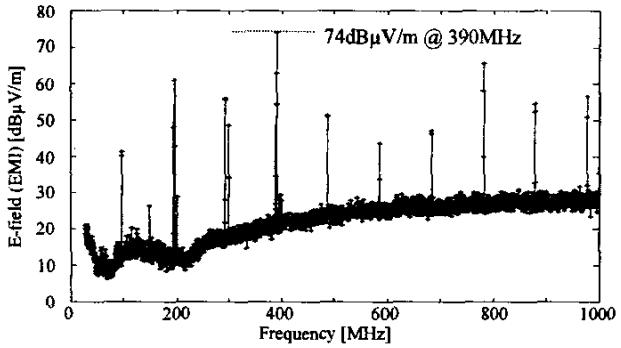
(d) Measured Period Jitter

Figure 9. Measurement for the implemented SSCG-DCA. (a) Measurement setup. (b) Measured spread spectrum clock waveform. The rising and the falling time are approximately 200ps. The measured operating frequency is approximately 100MHz. Using the measured spread spectrum clock waveform (b) and MATLAB program, the edge jitter as (c) and the period jitter as (d) are extracted.

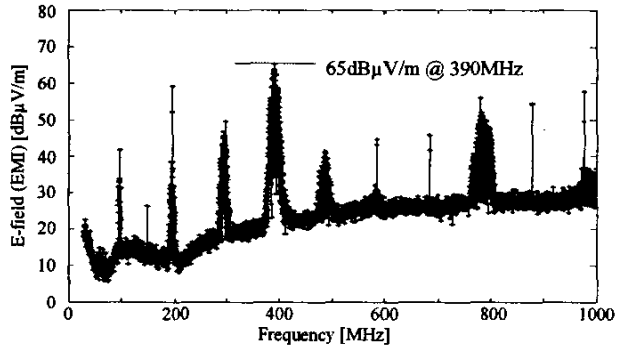
profiles as shown in Figure 9 are similar to the simulated jitter profiles using the HSPICE as shown in Figure 8.

To measure the EMI, a test PCB was designed and assembled. The test PCB was fabricated on a 2-layer FR-4 substrate. The size of the PCB is 195mm x 145mm and the height is 1mm. To generate the fixed period clock, a VCO was used. The operating frequency is approximately 100MHz. To measure the EMI, an additional micro-strip line was used. The length of interconnecting line is 150mm. The load capacitor is a 2pF ceramic chip capacitor. The EMI was measured in a 3m anechoic chamber.

Figure 10 is the measured EMI spectra of the fixed period clock and the spread spectrum clock from the implemented SSCG-DCA. The measured EMI for the fixed period clock is approximately 74dBμV/m at 390MHz and the measured EMI for the spread spectrum clock is approximately 65dBμV/m at 390MHz. The measured EMI was reduced by approximately 9dB at 390MHz using the proposed, and implemented SSCG-DCA.



(a) Measured EMI resulting from the fixed period clock



(b) Measured EMI resulting from the spread spectrum clock

Figure 10. Measured EMI spectra of the fixed period clock and the spread spectrum clock from the implemented SSCG-DCA.

V. CONCLUSIONS

In this paper, the spread spectrum clock generator with delay cell array (SSCG-DCA) is proposed to reduce electromagnetic interference (EMI) from high-speed digital systems. The edge jitter is controlled by implementing of the spread spectrum clock with a triangular modulation profile. The proposed SSCG-DCA has more effective attenuation and can be more easily implemented than the conventional spread spectrum clock generator with phase locked loop (SSCG-PLL). The proposed SSCG-DCA was implemented on an IC chip using a 0.35μm CMOS process and a 9dB attenuation of the EMI at 390MHz was measured.

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