A 4-W Master–Slave Switching Amplitude Modulator for Class-E1 EDGE Polar Transmitters

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***Abstract*—For Class-E1 EDGE polar transmitters, we proposed a 4-W master–slave switching amplitude modulator (MS-SAM) for both high efficiency and wide bandwidth. It consists of a combination of two step-down modules with different switching frequencies and different switch sizes. The master module was designed for wide bandwidth and the slave module for high efficiency. The paper also presents a new current-sensing circuit based on a sample-and-hold circuit operable under a high switching frequency ($>$ 40 MHz). We showed the topologies and operating principles. The chip was fabricated in a standard 0.35-μm CMOS process with an area of 6.45 mm ^{2}. The MS-SAM could drive the amplifiers of up to 4-W RF power in the experiment. We obtained an efficiency of 89%, and the converter's bandwidth was wide enough to meet the EDGE spectral requirements.**

***Index Terms*—Amplitude modulation, dc–dc power converter, current-sensing circuit, EDGE, polar transmitter, sample-and-hold (S/H) circuit.**

I. Introduction

IN MODERN wireless communication transmitters with higher data rate modulation formats, highly linear power amplifiers (PAs) are needed to avoid out-of-channel interference and distortion. PA efficiency is a key limiter of the battery life-span of wireless devices. Polar transmitter architecture has been proposed for the simultaneous achievement of high linearity and high efficiency. In such a system as shown in Fig. 1, an efficient power supply with a wide bandwidth called an amplitude modulator modulates the supply voltage for the RF PAs. The power supplies of RF PAs for EDGE polar systems require stringent specifications such as a low output ripple and wide bandwidth. In addition, battery-operated portable equipment requires an efficient and low-volume energy management circuit. Several approaches have been proposed to meet such requirements.

In polar transmitter applications, a low-dropout regulator is generally used for the power supplies because of the wide bandwidth [1]. However, this type of regulator inherently suffers from low efficiency. The most efficient energy conversion from a battery is achieved by means of a switching power converter, though this approach results in a limited bandwidth due to the limitation imposed on the switching frequency. A switching power supply based on the concept of interleaving delta modulation was suggested for polar transmitters in [2]. This amplitude modulator consumes a considerable amount of power and uses many external components. One recent approach used a hybrid structure consisting of a wideband linear amplifier and a switching amplifier [3]. However, the task of designing a linear amplifier faces various challenges, particularly the need for low output impedance, a wide bandwidth, and a high-current driving capability. Moreover, a linear amplifier uses a complex compensation circuit and an additional feedforward path.

We now present a master–slave switching amplitude modulator (MS-SAM) that provides high efficiency, wide bandwidth, and low output ripple voltage with easy implementation. A new current-sensing circuit is also proposed as a means of sensing the current at high switching frequency.

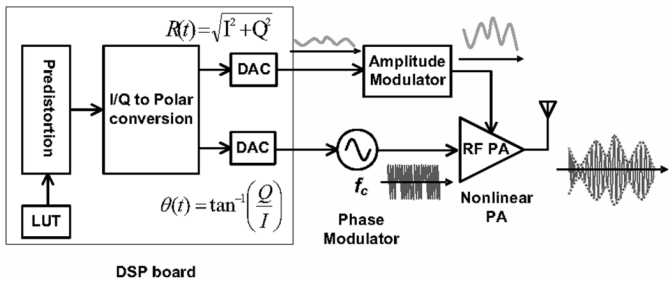

Fig. 1. Block diagram of a Polar transmitter.

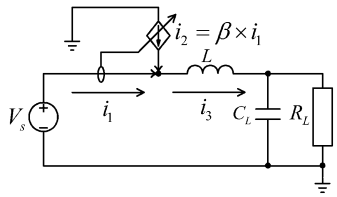

Fig. 2. Basic concept of MS-SAM.

II. Proposed Converter Demonstration

A. Basic Concept of the MS-SAM

Fig. 2 shows the basic concept of the proposed converter. It has a master–slave configuration that combines an independent voltage source with a dependent current source. This concept is similar to a mixed-mode amplifier as a hybrid structure consisting of a linear amplifier and a switching amplifier [4]. The hybrid structure was suggested for audio amplifiers.

From Fig. 2, the current equation is given by

$$i_3 = i_1 + i_2 = (1+\beta)i_1 = (1/\beta+1)i_2 \qquad (1)$$

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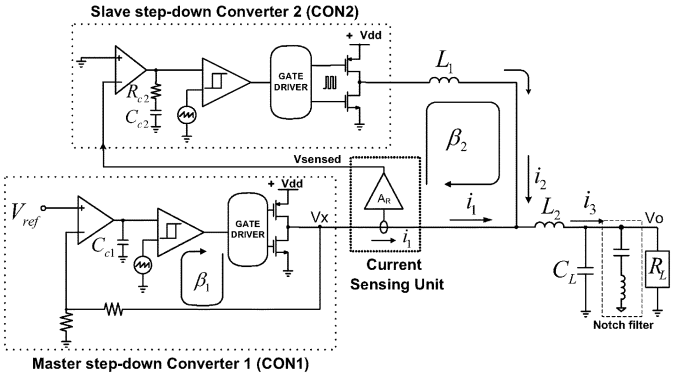

Fig. 3. Proposed MS-SAM topology.

where β is the current gain. In this equation, if β is sufficiently large, i_2 supplies most of the output current while controlling i_1 sufficiently small. Here, the independent voltage source should have a wide bandwidth and the dependent current source should have high efficiency in order to obtain wide bandwidth as well as high efficiency.

B. Detailed Description of the MS-SAM

In the case of the hybrid mode amplifier [3], the task of designing a wideband linear amplifier is not easy. Furthermore, it is hard to increase the efficiency of fast transient signals, as most of the fast transient currents should be supplied from the linear amplifier. In the structure shown in Fig. 3, MS-SAM replaces the linear amplifier of [3] with the switching step-down converter. High efficiency with low output voltage ripple can be attained by using fixed-frequency switching control known as PWM switching control. The predictable switching frequency ripple can be reduced further by a notch filter while keeping the bandwidth sufficiently wide. Furthermore, the converter has a high current driving capability, which leads to high efficiency for fast transient signals. The proposed converter offers a simple design and good compatibility with a conventional converter.

The proposed converter topology is shown in Fig. 3. It is composed of two step-down dc–dc converters having different switching frequencies and different switch sizes. Master step-down converter 1 (CON1) corresponding to an independent voltage source has a high switching frequency with small switches, whereas slave step-down converter 2 (CON2) corresponds to a dependent current source having relatively lower switching frequency with large switches. As a result of the high switching frequency of CON1, a wide bandwidth is consequently obtained, and the small switches lessen the switching loss. On the other hand, due to the lower switching frequency of CON2, higher efficiency is obtained and the large switches allow a larger current. By combining the two types of converters, we can achieve high efficiency as well as a wide bandwidth.

CON1 controls the output voltage and CON2 efficiently supplies most of the output current by sensing and amplifying the output current of CON1. Voltage loop β_1 is in charge of regulating the output voltage, and current loop β_2 makes the value of i_1 sufficiently small so that i_2 supplies most of the output current, i_3.

If we describe the operation in more detail, CON1's control loop β_1 makes V_o go up when $\mathrm{V}_{\mathrm{ref}}$ goes up. Then, i_1 also tends to increase in proportion to V_o. A current-sensing circuit senses the increment of i_1. The information from the current-sensing unit is delivered to CON2's control loop β_2. Loop β_2 makes i_2 continue to increase until i_1 is sufficiently small. Current i_2 has a ripple current, which is determined by inductor L_1. The excess ripple current flows into CON1 because β_1, the wide bandwidth loop, regulates V_o, which corresponds to an independent voltage source, that is, CON1 absorbs the ripple current of CON2.

The fact that the MS-SAM has higher efficiency than the conventional converter is well described through the following equations.

The main loss of a conventional converter can be given by

$$\begin{aligned} P_{\mathrm{loss}}(\mathrm{conventional\_converter}) &= P_{\mathrm{sw}} + P_{\mathrm{cond}} \\ &= W \cdot C_o \cdot V^2 \cdot f + (I^2 \cdot R)/W \end{aligned} \tag{2}$$

where P_{sw} is the switching power loss, $\mathrm{P}_{\mathrm{cond}}$ is the conduction power loss, W is the switch width, C_o is per unit capacitance related to the switch width, V is the switch drive voltage, f is the switching frequency, I is the conduction current, and R is the switch on resistance.

The optimum switch size is determined when $\mathrm{P}_{\mathrm{sw}} = \mathrm{P}_{\mathrm{cond}}$ to make the total loss minimum

$$W_{\mathrm{opt}} = \sqrt{(I^2 \cdot R)/(C_0 \cdot V^2 \cdot f)}. \tag{3}$$

If we denote the switching frequency and conduction current of CON1 (CON2) as $f\,(f/A)$ and $I/B\,(I)$, respectively, then the switch sizes are given by

$$\begin{aligned} W_{\mathrm{opt}}(\mathrm{CON1}) &= \sqrt{\{(I/B)^2 \cdot R\}/(C_0 \cdot V^2 \cdot f)} \\ &= \sqrt{(I^2 \cdot R)/(C_0 \cdot V^2 \cdot f)}/B \\ &= W_{\mathrm{opt}}/B \end{aligned} \tag{4}$$

$$\begin{aligned} W_{\mathrm{opt}}(\mathrm{CON2}) &= \sqrt{(I^2 \cdot R)/\{C_0 \cdot V^2 \cdot (f/A)\}} \\ &= \sqrt{A} \times \sqrt{(I^2 \cdot R)/(C_0 \cdot V^2 \cdot f)} \\ &= \sqrt{A} \cdot W_{\mathrm{opt}}. \end{aligned} \tag{5}$$

In this case, the power losses are given by

$$\begin{aligned} P_{\mathrm{loss}}(\mathrm{CON1}) &= \left(\frac{W_{\mathrm{opt}}}{B}\right) \times C_0 \cdot V^2 \cdot f \\ &\quad + \left\{\left(\frac{I}{B}\right)^2 \times R\right\} / \left(\frac{W_{\mathrm{opt}}}{B}\right) \\ &= (W_{\mathrm{opt}} \cdot C_0 \cdot V^2 \cdot f + (I^2 \cdot R)/W_{\mathrm{opt}})/B \end{aligned} \tag{6}$$

$$\begin{aligned} P_{\mathrm{loss}}(\mathrm{CON2}) &= (\sqrt{A} \cdot W_{\mathrm{opt}}) \times C_0 \cdot V^2 \cdot f \left(\frac{f}{A}\right) \\ &\quad + \frac{I^2 \cdot R}{\sqrt{A} \cdot W_{\mathrm{opt}}} \\ &= (W_{\mathrm{opt}} \cdot C_0 \cdot V^2 \cdot f + (I^2 \cdot R)/W_{\mathrm{opt}})/\sqrt{A} \end{aligned} \tag{7}$$

and the overall power loss is the sum of the two losses as

$$P_{\text{loss}}(\text{proposed}) = \frac{\left(W_{\text{opt}} \cdot C_0 \cdot V^2 \cdot f + \frac{I^2 \cdot R}{W_{\text{opt}}}\right)}{\sqrt{A}} + \frac{\left(W_{\text{opt}} \cdot C_0 \cdot V^2 \cdot f + \frac{I^2 \cdot R}{W_{\text{opt}}}\right)}{B} \quad (8)$$

If we compare the losses between this proposed converter and the conventional one, then we obtain

$$\alpha = \frac{P_{\text{loss}}(\text{proposed\_converter})}{P_{\text{loss}}(\text{conventional\_converter})} = \frac{1}{\sqrt{A}} + \frac{1}{B}. \quad (9)$$

From this equation, the proposed converter's power loss is less than that of a conventional one assuming the same converter bandwidth and output current because the values of A and B are designed to be greater than 1. In this case, constant A means the frequency ratio between CON1 and CON2 while constant B means the conduction current ratio between CON2 and CON1. Constant A is determined by the choice of the circuit designer while constant B is determined by the loop gain β_2 in Fig. 3. The value of A is limited by the analog circuit operation frequency. The loop β_2 pursues to make i_1 be 0; hence, for a large value of β_2, constant B is large. However, to ensure the stable operation of MS-SAM, the loop β_2 should have enough phase margin. This means that, for high-frequency operation, β_2 is relatively low. This factor is the limitation of B for high-frequency operation. For example, for $A = 10$ and $B = 10, \alpha$ is 0.461, showing that the power loss can be reduced to more than one half that of the conventional converter.

Our master module (CON1) is designed to operate at a 40-MHz switching frequency for a wide bandwidth and a fast transient response, whereas the slave module (CON2) is designed to run at 4 MHz for high efficiency and large current sourcing. CON1 uses a one-cycle control for easy compensation [5]. Because loop β_1 has no inductor, one-pole compensation is enough to ensure that the loop is stable with a wide bandwidth. Due to the effective series resistance of the inductor, some voltage error is induced, however as confirmed by the experimental results, the error is too small to affect the PA's power spectral density over a wide load range.

To meet the EDGE spectral requirement, we have to ensure the bandwidth of the amplitude modulator be higher than 2 MHz. Also, the output ripple voltage should be less than 20 mV_{pp} so as not to violate the spectral requirement of -60 dBc [3]. When the bandwidth of CON1 is wide enough, the bandwidth of the MS-SAM is limited by the output filter (L_2 and C_L). Therefore, the resonant frequency of the output filter is designed to be 4 MHz. The current ripple of CON2 is largely absorbed by the wide bandwidth of CON1. The ripple voltage generated by CON1 and CON2 is decayed by the output filter (L_2 and C_L). Because the output filter was insufficient to meet the voltage ripple specification of the EDGE system, finally we adopted an additional notch filter while keeping the bandwidth sufficiently wide. The remaining challenge is to develop a means to precisely sense the high-frequency current.

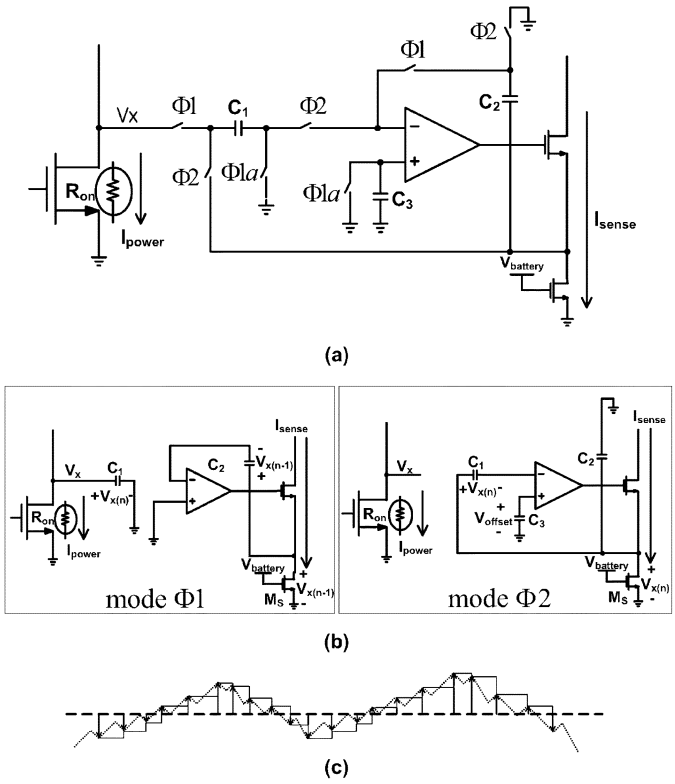

Fig. 4. Proposed current sensing circuit. (a) Description of proposed current sensing circuit. (b) The operation of the current sensing circuit. (c) S/H operation point of proposed current-sensing circuit.

III. Proposed Current-Sensing Circuit

The most common method of sensing a current is to use a sensing resistor, which induces considerable power dissipation. Another method is to use a current transformer, which is bulky for implementation. Neither of these two methods is suitable for integrated circuits. Some effort has been made to sense the output current utilizing on resistance of a power switch [6]. However, the current-sensing circuit is limited in the high-frequency region because of the limited bandwidth of the op-amp. The role of the op-amp is to make the source–drain voltage of the power switch and sensing transistor be equal. Fig. 4(a) shows the proposed nMOS current-sensing scheme. The pMOS current-sensing circuit is a counterpart of Fig. 4(a). The proposed circuit uses a sample-and-hold (S/H) circuit to sense the source–drain voltage of the power switch. In contrast with conventional circuits, the proposed circuit has no negative feedback limiting the operating frequency. Thus, the circuit operation does not suffer from the finite bandwidth of the op-amp. Moreover, because the role of the op-amp in the S/H circuit is to define the ground level, the requirements of the op-amp, such as the bandwidth and the input common mode range, are not stringent.

In mode Φ_1, C_1 is charged to the V_x value and C_2 holds the previous value of V_x. In mode Φ_2, the voltage of C1 is transferred to sensing transistor M_s. This operation is shown in Fig. 4(b), and we show in Fig. 4(c) the sampling point of the S/H circuit. The upper S/H circuit (PMOS current sensing) samples the voltage difference between V_{battery} and the V_x node, while the lower S/H circuit (NMOS current sensing) samples

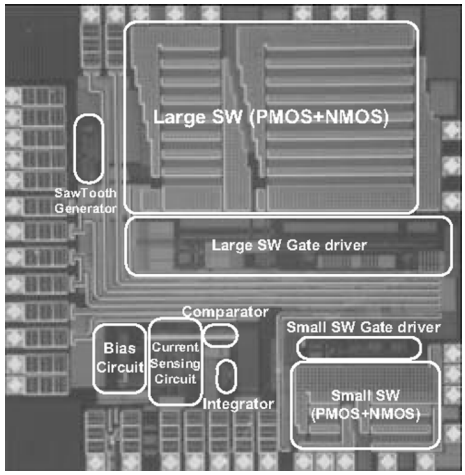

Fig. 5. Chip micrograph.

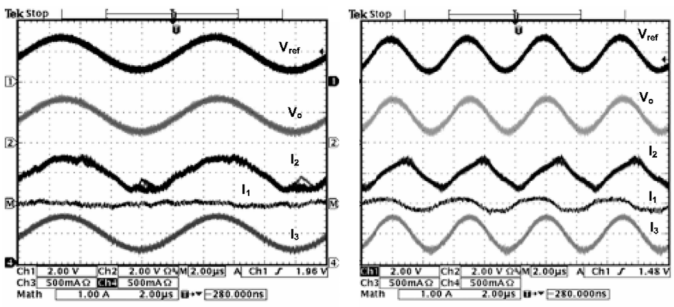

Fig. 6. Measured waveforms for (a) 100 kHz and (b) 200 kHz sine-wave with 4.

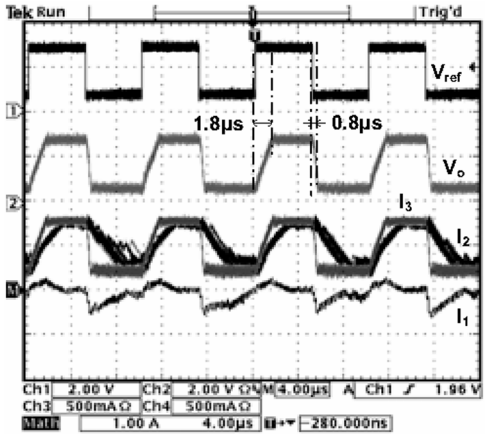

Fig. 7. Ramp timing response for 100-kHz square-wave signal with 4.

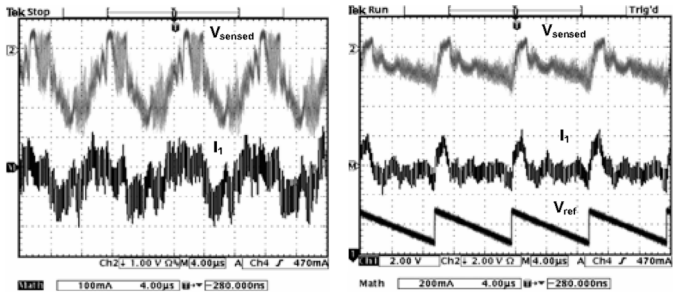

Fig. 8. Measured current sensing waveforms for (a) sine wave reference and (b) sawtooth wave reference.

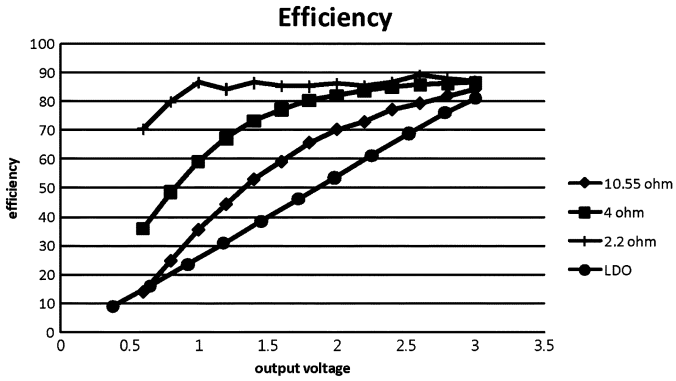

Fig. 9. Efficiency versus output voltage for various load conditions.

the voltage difference between V_x and the ground node. When the pMOS is on, the upper S/H circuit works; when the nMOS is on, the lower S/H circuit works. The sampling timing is determined by either the pMOS off-time or the nMOS off-time, depending on the current direction. When the inductor current flows in a positive direction from the battery to the output, the positive peak current is sampled; however, when the inductor current flows in a negative direction from the ground to the output, the negative peak current is sampled. The sampled value is held in the capacitor until the next sampling point. The sizes of the power switches and sensing transistors are in a ratio of 10000:32. The role of C_3 is to compensate the offset-voltage caused by the operational amplifier. To minimize the charge injection errors, we used a slightly advanced off-time clock Φ_{1a}.

By using this current-sensing circuit, we enable the inductor current to be sensed without any frequency limitation and both the positive and negative direction inductor currents can be sensed successfully at 40 MHz. This current-sensing circuit is also suitable for other applications such as for the current-mode control scheme and for the short-circuit protection schemes.

IV. Experimental Results

The MS-SAM was implemented with a standard 0.35-μm process. Fig. 5 shows a micrograph of the chip. The total die area is 6.45 mm^2. The sizes of power transistors are 110 000 μm/0.5 μm for the pMOS and 30 000 μm/0.5 μm for the NMOS.

The values of $L_1, L_2, C_L, R_L, C_{C1}, C_{C2}$, and R_{C2} in Fig. 3 are chosen to be 4.7 μH, 500 nH, 3 nF, and 4 Ω, 20 pF, 200 pF, and 2 kΩ, respectively. The input voltage changes from 3.8 to 4.5 V, which is the battery voltage, and the output voltage varies from 0.6 to 3.0 V. To show the proposed circuit operation under a wide bandwidth, 100-kHz and 200-kHz sinusoidal reference signals are applied. Fig. 6 shows the waveforms with a 4-Ω load. In the plot, the waveform of current I_1 is generated by the math function of the oscilloscope, which corresponds to $I_3 - I_2$. Because the node V_x in Fig. 3 is very sensitive to parasitic components, the task of measuring I_1 directly from the circuit is difficult. For a frequency higher than 150 kHz, I_2 cannot supply all of the load current I_3; thus, I_1 makes up the current shortfall. These results show that the MS-SAM works well as described in the previous analysis. The output voltage can follow up to a 230-kHz full-power sine signal that varies from 0.6 to 3.0 V

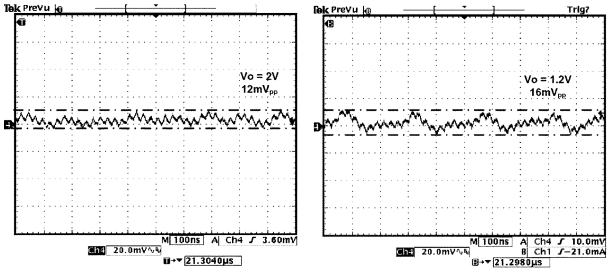

Fig. 10. Output ripple voltage.

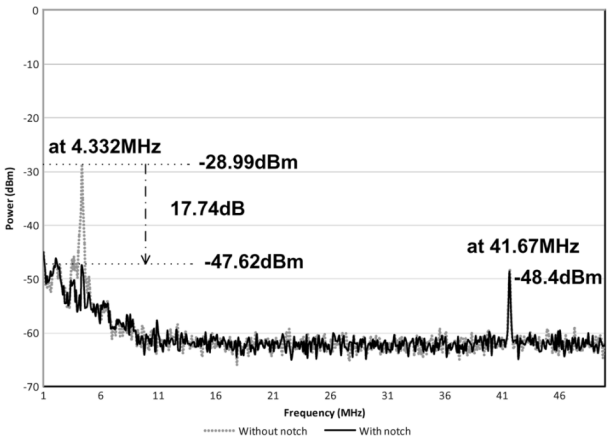

Fig. 11. Effect of a notch filter to output ripple voltage.

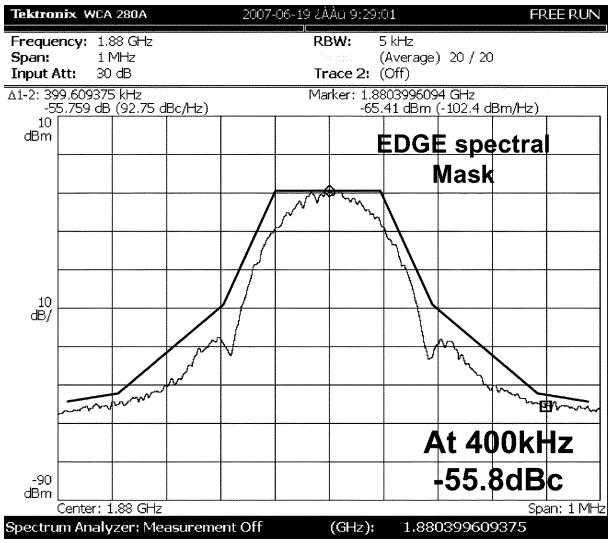

Fig. 12. Output spectrum.

without distortion. Fig. 7 shows the ramp timing response for a 100-kHz square-wave signal with a 4-Ω load. The ramp-up response is about 1.8 μs and the ramp-down response is about 0.8 μs. Fig. 8 shows that the proposed current-sensing circuit can follow a 40-MHz current signal well for various reference signals. Fig. 9 plots the measured efficiency for various load conditions. The MS-SAM can supply a maximum 4 W to a 2.2-Ω load. If the RF PA has a maximum efficiency of 50%, the load that corresponds to a Class-E1 power condition of 33 dBm is about 2.2 Ω. The maximum efficiency is 89% with a 2.2-Ω load. Compared to the efficiency of a commercial LDO, the

TABLE I
PERFORMANCE OF MS-SAM

Technology	AMS 0.35μm process with I/O device
Input Voltage	3.8 ~ 4.5V
Output Voltage	0.6 ~ 3V
Switching frequency	40MHz, 4MHz respectively
Converter Bandwidth	Enough to meet the EDGE spectral mask
Maximum output power	4W (Class-E1 EDGE)
Output voltage ripple	Under 20mV_{pp}
Output settling time with ramp up	1.8μs
Output settling time with ramp down	0.5μs
Maximum efficiency	89%
Chip area	6.45mm^2

MS-SAM shows higher efficiency under a heavy load condition. Fig. 10 shows the output ripple voltage according to 1.2-V and 2-V output voltage. The ripple voltages contain both 4-MHz and 40-MHz ripple. Output ripple voltages of 4 and 40 MHz are under 20 mV_{pp}. The effect of the notch filter is demonstrated in Fig. 11, which is measured by spectrum analyzer. The output voltage ripple is decayed by 17.74 dB when we use the notch filter. Fig. 12 shows the spectral response for an EDGE signal generated from a DSP board. The carrier frequency is 1.88 GHz. In the EDGE experimental setup, we used a commercial RF PA and a DSP board for the predistortion and EDGE signal generation. The experimental setup satisfies the EDGE spectral mask. The measured performance is summarized in Table I.

V. CONCLUSION

We proposed a new type of master–slave switching amplitude modulator that employs a new current-sensing circuit. Our description includes the basic concept of the MS-SAM and the detailed operation of the MS-SAM. We also suggested a new current-sensing circuit operable under frequencies higher than 40 MHz. The amplitude modulator achieves a wide bandwidth without suffering from switching loss. Therefore, this modulator provides high efficiency as well as wide bandwidth. The measured efficiency is as high as 89%. The output voltage ripple is small enough to meet the EDGE specification. Thus, the integrated chip allows a polar transmitter module to meet the Class-E1 EDGE specifications with good power efficiency.

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