SP 23.5: CMOS Current-Controlled Oscillators Using Multiple-Feedback-Loop Ring Architectures

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Three types of high-frequency current-controlled oscillators (ICO) having multiple-feedback loops are implemented in a 0.8μm CMOS technology. Three stage single-feedback-loop ICO (SICO) and double-feedback-loop ICO(DICO) and four-stage triple-feedback-loop ICO (TICO) are tested and compared. They all use the differential current steering logic (DCSL). Using the multiple-feedback-loop ring architectures, the operation frequencies of the ICO's are considerably improved and obtained 1.69GHz.

Controlled oscillators are common building blocks used widely in communication systems, especially in such applications as phase-locked loops. Important characteristics of controlled oscillators are frequency of operation, linearity of voltage/current-to-frequency characteristic, tuning range, phase noise, frequency stability with temperature variation and cost of fabrication. High-frequency controlled oscillators are implemented as ring oscillators, relaxation oscillators and recently monolithic LC oscillators. Monolithic LC oscillators using spiral inductors or bonding wire inductors have low phase noise but relatively narrow oscillation frequency range and large silicon area [1, 2]. Ring oscillators and relaxation oscillators tend to have poor phase-noise characteristics and poor frequency stability at high frequencies, but usually have wider range of oscillation and relatively small die size.

These CMOS ICO building blocks are for use in communication areas such as frequency synthesizers and clock recovery circuits. Fully-differential architecture with the differential-current steering logic (DCSL) delay cells reduce supply-induced phase-noise of the ICO. In these differential architectures, the supply current ideally remains constant throughout the period of oscillation, improving the phase-noise characteristics of the oscillators. By introducing the multiple-feedback-loop ring architecture, the delay of the unit cell in the ICO is minimized. From the experimental results, the TICO has 55% speed improvement compared to the SICO and 26% speed improvement compared to the DICO at their maximum operating frequencies.

The basic circuit diagrams are shown in Figure 1. Figure 1a is a single-ended current steering logic (CSL), Figure 1b, 1c, and 1d are differential versions of CSL that is differential current steering logic (DCSL) [3]. To accommodate the multiple-feedback-loop ring oscillators, Figure 1c and 1d have the additional auxiliary differential input pairs (M1A, M2A) and (M1B, M2B). If the ring oscillators are constructed using the cells as in Figure 1, the supply current remains constant throughout the oscillation period of the ICO. Since the supply current remains constant, the voltage across the parasitic leakage inductance, Ldi/dt, is zero which means lower supply-voltage fluctuations, and relatively low phase-noise compared to the conventional differential delay cells [4].

Figure 2 shows simplified schematics of the three types of ICOs. In Figure 2a, multiple-feedback-loop is composed as follows: through the input transistors, M1 and M2, the main 4-stage loop is formed and the auxiliary 3- and 2-stage loops are formed through the additional input transistor pairs , (M1A, M2A) and (M1B, M2B), respectively. A similar multiple-feedback-loop is composed in Figure 2b. Figure 2c is the 3-stage SICO. The output driving currents in the DCSL are the sum of the drain currents from M1, M1A and M1B. The counter action occurs in M2, M2A and M2B. Since the phases of the gate driving voltages for M1A (M2A) and M2A (M2B) lead the phases for M1 and M2, the auxiliary 3- and 2-stage loops serve to reduce the effective gate delay of the main 4-stage loop. The device sizes of the main and auxiliary differential input transistors must be ratioed to operate properly. By using input main transistors M1 and M2 larger than the auxiliary input transistors, TICO operates properly as 4-stage ring oscillator with reduced gate delay. The maximum oscillation frequency and the output voltage swing can be controlled by the ratios of the input transistors and the diode transistors. All of the transistors are scaled in terms of speed and output swing. To drive the mixer in PLLs, the delay cells have 1V output voltage swings at their maximum speed.

This chip is fabricated with 0.8μm double-poly double-metal CMOS process. A micrograph of the TICO with drivers to drive 50Ωoff-chip load is shown in Figure 3. The die measures 790x745μm². The core occupies 135x200μm². Another chip that includes SICO and DICO is fabricated on the same wafer with the output drivers. The core areas of SICO and DICO are about 100x200μm². Figure 4 shows the output waveform of the TICO. The tuning characteristics of the various ICO s are shown in Figure 5. This curve shows that the frequency range of oscillation is wide: about 0.95-decade for TICO and 1-decade for DICO and SICO. They also show good linearity of control current in the appropriate frequency range. The output spectrum of the TICO is shown in Figure 6. The power-delay product curves of the three types of ICOs are shown in Figure 7. The curves indicate that the multiple-feedback-loop is more efficient ring oscillator architecture in terms of speed and power. The maximum operating frequencies of SICO, DICO and TICO are 1.39GHz, 1.58GHz, and 1.69GHz, respectively. The power dissipations of the cores of SICO, DICO and TICO at their maximum speeds are 123mW, 110mW and 78mW, respectively, with 5V single supply.

Acknowledgment:

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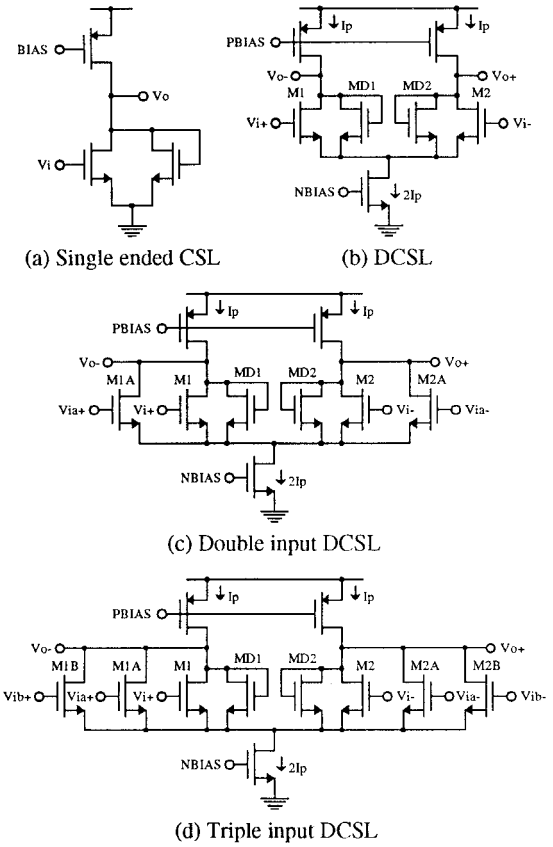
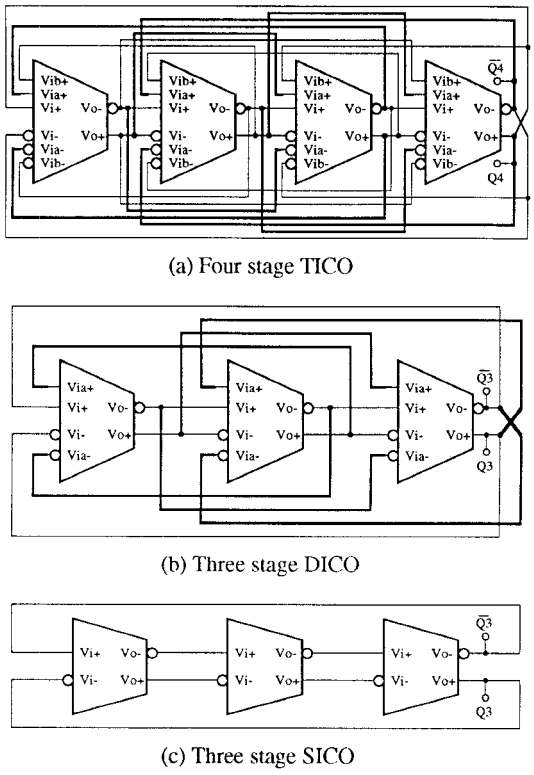


(a) Single ended CSL (b) DCSL

(c) Double input DCSL

(d) Triple input DCSL

Figure 1: Current steering logic delay cells.
(a) Single ended CSL.(b) DCSL.
(c) Double input DCSL.(d) Triple input DCSL.



(a) Four stage TICO

(b) Three stage DICO

(c) Three stage SICO

Figure 2: Simplified schematics of the three types of ICO's.
(a) Four stage TICO.(b) Three stage DICO.
(c) Three stage SICO.

Figure 3: See page 490.

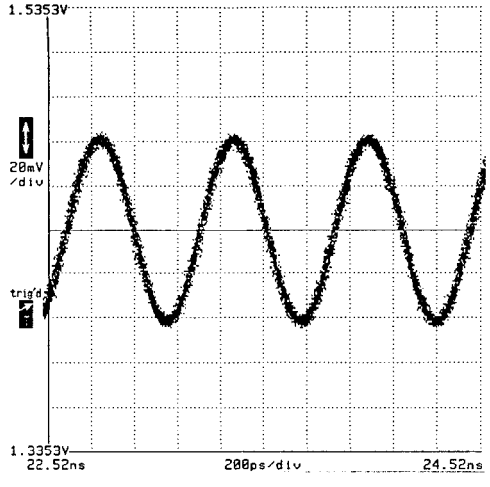


Figure 4: Output waveform of the 4-stage TICO(1.67GHz).

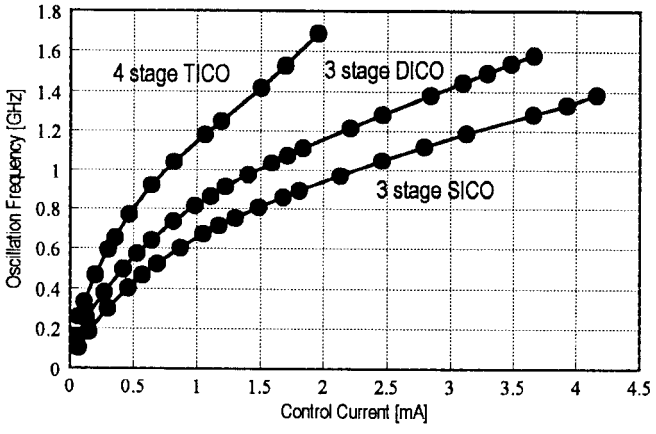


Figure 5: Tuning characteristics of the 3 types of ICOs.

Figure 6, 7: See page 490.

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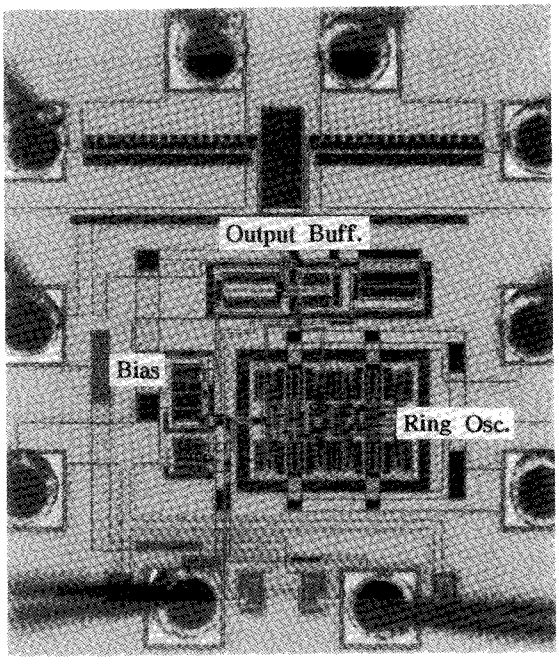

Figure 3: Four stage TICO chip micrograph.

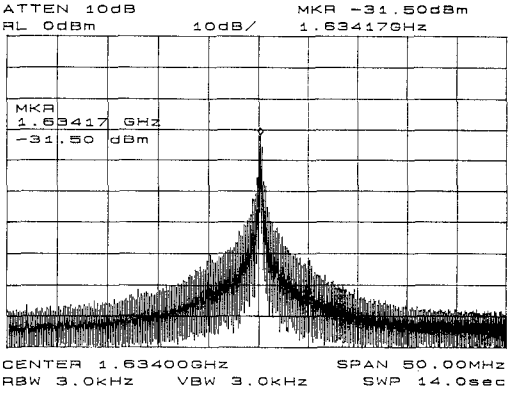

Figure 6: Output spectrum of the four stage TICO.

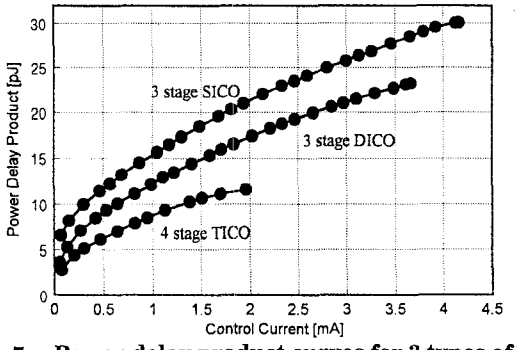

Figure 7: Power-delay product curves for 3 types of ICOs.

SP 23.7: A Balanced 1.5GHz Voltage Controlled Oscillator 390with an Integrated LC Resonator

(Continued from page 391)

f_0 (GHz)	1.476	1.760	2.360	2.048	0.913	0.85	1.75
Power (mW)	40	24	54	3	10	30	70
Pout (dBm)	-6.6(diff)	-35	-13.5	-25	-3 (diff.)	-25	-25
V_{cc} (V)	3.6	3	3.6	3	3	3	5
$L(f_m)$ dBc/Hz	-105 @ 100 kHz	-107 @ 100 kHz	-92 @ 1 MHz	-74 @ 100 kHz	-101 @ 100 kHz	-85 @ 100 kHz	-88 @ 100 kHz
Tuning Range (MHz)	150 (10%)	79.2 (4.5%)	N/A	N/A	N/A	120 (14%)	200 (11%)
Area (mm^2)	0.5	5.18	0.5	N/A			0.2
Min. V_{cc} (V)	2.5	N/A	2.6	2.7	2.7	N/A	N/A
Diff./Single	Diff.	Diff.	Single	Diff.	Diff.	Diff.	Single
Process	11 GHz BiCMOS	0.7µm CMOS	12 GHz BiCMOS	20 GHz BiCMOS	25 GHz Bipolar	1µm CMOS	10 GHz BiCMOS
Reference	This	[5]*	[6]	[7]	[8]	[9]	[10]

*Note: This VCO uses bond wire inductors and is not truly monolithic.

Table 1: Monolithic VCO performance.