A Unity Power Factor Electronic Ballast for Fluorescent Lamp having Improved Valley Fill and Valley Boost Converter

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Abstract -- A new PF correction topology, Improved Valley Fill (IVF) with Valley Boost Converter (VBC) used in the electronic ballast for fluorescent lamp is presented. Different from the conventional valley fill, the IVF has the different charging operation to the electrolytic capacitors and can adjust the valley voltage higher than half the peak line voltage. Hence, there is no pulsating line current around the line voltage peak, PF and THD are significantly improved. The IVF also improves lamp current CF by the energy transfer action. The VBC is added to the IVF to achieve unity PF and to increase the valley voltage. The VBC operates only during valley region to decrease the loss of switching devices and the voltage stress of resonant inverter. The VBC can be constructed with small size and low cost having very simple controller. The measured PF and THD for a prototype electronic ballast are 0.997 and 5%, respectively, and the lamp current CF is as low as 1.5.

I. INTRODUCTION

The fluorescent lamp is today's one of the most popular lighting system because of its higher luminous efficacy (lm/W) which is the energy conversion efficiency of the lamp. A ballast is needed for fluorescent lamp or gaseous discharge lamp because this has negative resistance characteristic in the desired region of operation [1]. Usually, in combination with capacitor, a lossless inductor or high-leakage transformer is used. The ballast plays the roles of providing sufficiently high starting voltage, current limiting after starting, and probably raising input power factor.

Typical electronic ballasts have a bridge rectifier followed by an electrolytic energy storage capacitor to provide a smooth dc voltage to the subsequent high frequency resonant inverter driving the lamp. The resultant high frequency lamp current has low double line frequency modulation and has a current crest factor (CF) of about 1.5, which meets the traditionally acceptance limit of 1.7. However, this comes at the expenses of very low power factor (PF<0.6) and very high line current harmonic distortion (THD>130%) [2].

A circuit, referred to as valley fill, attempts to address the above issues [3]. Fig. 1 is the basic diagram and waveforms of the conventional valley fill circuit. This is composed of two electrolytic capacitors(C1,C2), three rectifying diodes(D1~D3). Around the line peak, C1 and C2 are charged through D3 to half the peak line voltage. As long as the line voltage remains above each capacitor voltage, the line supplies the ballast directly. When the line voltage falls below each capacitor voltage, i.e., valley voltage, bridge rectifier diodes is back-biased, and D1 and D2 conduct to feed the ballast. Thus the voltage supplied to the ballast follows the line voltage for about 120 degree symmetrically around the peak and follows the capacitors voltage for about 60 degree near the line zero crossings. However, a pulsating line current happens to charge the capacitors near the peak line voltage, which deteriorates the PF(~0.95) and the THD(~40%). As a result, a large front-end inductor(>10mH) is required to filter out the pulsating line current. Also, the lamp current has high double line frequency modulation, in other words, high current CF reducing lamp efficacy and life. This is due to the large ripple voltage (half the peak line voltage) of dc bus.

This paper introduces a new valley fill topology called Improved Valley Fill (IVF) circuit. Compared with the conventional valley fill, the IVF charges the electrolytic capacitors with the resonant inverter current resulting in smooth line current. To obtain unity PF, in addition, we combine the IVF with a valley boost converter (VBC) named because it operates during the valley region only. Thus the resulting PF correction circuit has nearly unity PF, very low THD, and excellent lamp current CF.

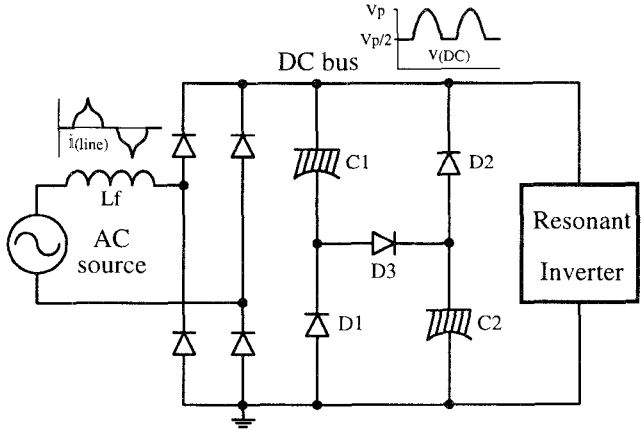

Fig. 1. Conventional valley fill circuit and waveforms

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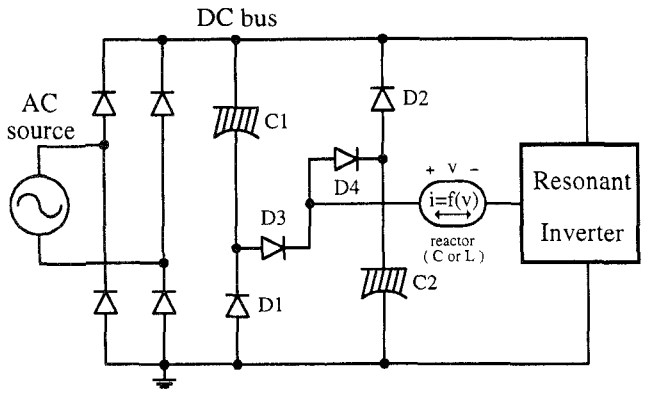


Fig. 2. Improved valley fill (IVF) circuit

II. Improved Valley Fill

The functional basic diagram of the new improved valley fill (IVF) is shown in Fig. 2. The IVF is composed of two electrolytic capacitors(C1,C2), two rectifying diodes(D1,D2), two fast recovery diodes(D3,D4), and extra a small reactor. Comparing the IVF with the conventional valley fill shown in Fig. 1, we substitute the one rectifying diode(D3 in Fig. 1) with the two fast recovery diodes(D3,D4). D3 and D4 are to charge up C1 and C2 according to the direction of the high frequency resonant inverter current.

Essentially, the IVF performs a similar operation to the conventional valley fill. As long as the line voltage remains below C1 and C2 voltage (valley region), D1 and D2 conduct to feed the ballast. When the line voltage goes above C1 and C2 voltage (direct region), the line supplies the ballast. In this interval, unlike the valley fill, C1 and C2 are charged alternately through a extra reactor and one diode (D3 or D4) with the cyclic current generated by the resonant inverter. The reactor is a small capacitor or inductor whose reactance value controls the charging current of the capacitors. If the reactance is very high, the charging current of the capacitors becomes very small and the capacitor voltage is nearly half the peak line voltage. On the other hand, if the reactance is getting lower, each capacitor voltage becomes high above half the peak line voltage compared with the previous high reactance case. The more the charging current of the capacitors increases, the more the capacitor voltage increases. To maximize each capacitor voltage, we can remove and then short the reactor. Hence, the IVF can control each capacitor voltage (valley voltage) above half the peak line voltage by adjusting the reactance value, that is, the charging current of the capacitors.

As a result, the dc bus voltage and the line current can be depicted as Fig. 3. The line current becomes a quasi sine waveform dependent on the nonconduction angle α. This is under the assumption that the ballast operates as a constant load, so the line current is directly proportional to the line

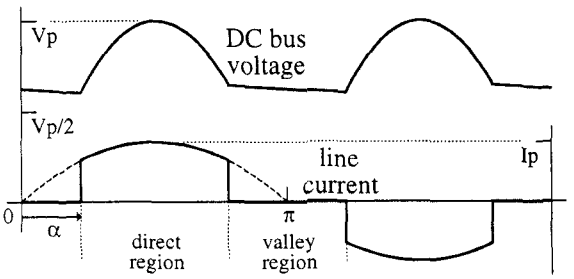


Fig. 3. The waveforms of improved valley fill with variable nonconduction angle

voltage. By the valley fill operation, the valley voltage can not be reduced under the Vp/2. So the minimum value of α is $\pi/6$. The dc bus voltage supplied to the ballast follows the line voltage during π-2α degrees symmetrically around the peak and follows the capacitors' voltage during 2α degrees near the line zero crossings. The α is dependent on the amount of the capacitors' charging current, and determines the valley voltage directly as (1).

$$V_{DC\,bus,valley} = V_{line,peak} * \sin\alpha \tag{1}$$

The magnitude of the line current harmonics is equal to (there are only odd harmonics)

$$I_{n\,(1,3,5,\ldots,\infty)} = \left(\frac{2}{\pi}\right)\left[\frac{\sin(n-1)\theta}{2(n-1)} - \frac{\sin(n+1)\theta}{2(n+1)}\right]_{\alpha}^{\pi-\alpha} \tag{2}$$

PF is the ratio of the rms of the fundamental input line current to the rms of the total line current. Also THD is the ratio of the total harmonic component to the fundamental component of the input line current. Using (2), we derive the PF and THD in (3).

$$\begin{aligned} PF &= \frac{I_{fund,rms}}{I_{total,rms}} = \frac{(\pi-2\alpha+\sin 2\alpha)/\sqrt{2}\pi}{\sqrt{(\pi-2\alpha+\sin 2\alpha)/2\pi}} = \sqrt{\frac{\pi-2\alpha+\sin 2\alpha}{\pi}} \\ THD &= \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_{fund}} = \frac{\sqrt{I_{total,rms}^2 - I_{fund,rms}^2}}{I_{fund,rms}} \\ &= \frac{\sqrt{1-PF^2}}{PF} = \sqrt{\frac{2\alpha-\sin 2\alpha}{\pi-2\alpha+\sin 2\alpha}} \end{aligned} \tag{3}$$

Equation (1) and (3) for different values of the α are depicted in Fig. 4 which shows the valley voltage, PF, and THD.

The presented IVF circuit has several advantages over the conventional valley fill. The IVF can control the capacitors' voltage (valley voltage) above half the peak line voltage by adjusting the reactance value, that is, the charging current of the capacitors. As the capacitors' voltage is above half the

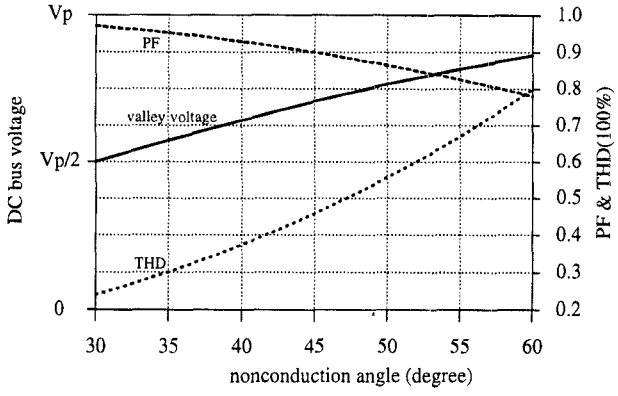


Fig. 4. DC bus voltage, PF&THD in improved valley fill

peak line voltage, it is impossible to charge the capacitors passing through the dc bus directly. So there is no pulsating line current around the line peak and a large front-end inductor(Lf in Fig. 1) to raise the PF is not required. Besides, the lamp current in the IVF has lower double line frequency modulation, i.e., lower current CF than that of the conventional valley fill, because the ripple of dc bus voltage is decreased by the raised valley voltage. As a note, the low lamp current CF is desirable from efficacy and lamp life.

Although, in case that the reactor is optimally chosen to have the valley voltage nearly half the peak line voltage (Vp/2, α=30 in Fig. 4), the PF and the lamp current CF is more improved than that of the conventional valley fill. The quasi sine wave without pulsating line current has PF about 0.97 compared with 0.95 in the conventional one. Also the lamp current is more increased in the valley region and reduced in the direct region to get the same rated output power, because the resonant inverter in the IVF transfer the energy from direct region to valley region. On the contrary, the conventional valley fill supply the energy of valley region from input line directly. Thus the lamp current CF of the IVF is more reduced than the that of the conventional one.

III. Improved Valley Fill combined with Valley Boost Converter

Though the IVF improves the lamp current CF, the valley voltage has to be increased as high as possible to minimize the lamp current CF for efficacy and lamp life. So the large value of α is required to increase the valley voltage as shown in Fig. 4. However, this implies that the PF decreases and the THD increases. In order to overcome this drawbacks and to get a unity PF, therefore, a Valley Boost Converter (VBC) composed of L_B, D_{B1}, D_{B2} and M_B in Fig. 5 is combined to operate during the valley region only. The D_{B2} is added to pass the line current to the resonant inverter directly in direct region, which reduces the loss generated by L_B. The reactor in Fig. 2 is removed and shorted to maximize the valley

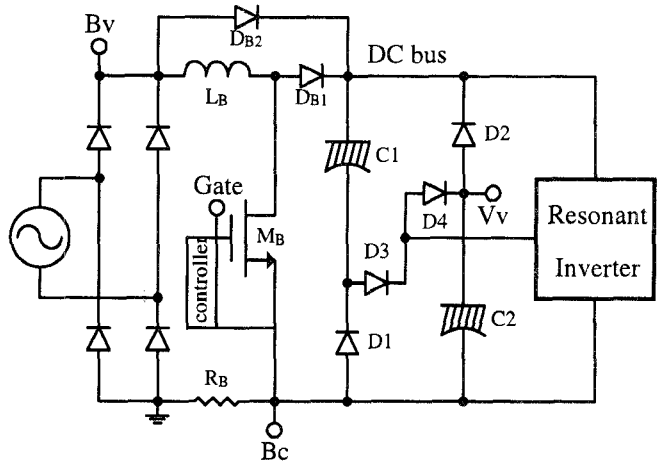


Fig. 5. Improved valley fill (IVF) combined with valley boost converter (VBC)

voltage. This is due to the fact that the PF is unity by the action of the VBC independent of the nonconduction angle α, in other words, the valley voltage.

This limited operation region of the VBC decreases the loss of switching devices. The voltage stress of main inverter is also reduced significantly compared with the others using the conventional boost converter for high PF. This results from the fact that the peak voltage of the dc bus is equal to the peak line voltage in this suggested scheme while the dc bus voltage is controlled higher than the peak line voltage in the conventional one. The rms current of this VBC becomes small due to the limited range of operation (2α duration), which results in small size of the power device and inductor as well. Besides, the VBC controller can be designed very simple because the shape of the line current needs not be very precise during 2α in order to keep high PF at the line side. Even the continuous conduction mode operation of the VBC is possible due to its small current and low voltage (valley region) operation. And thus, the harmonic components of the line current is much reduced.

Fig. 6 is the operation waveforms of Fig. 5 circuit. The valley voltage is increased much higher than half the peak line

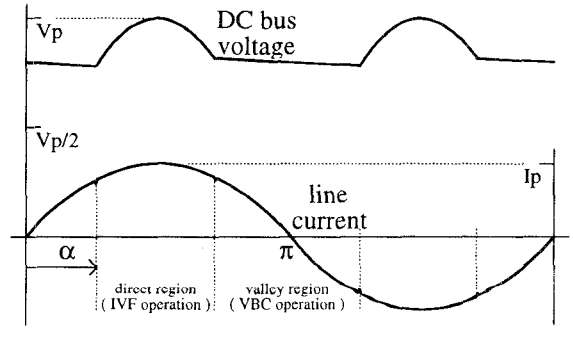


Fig. 6. The waveforms of IVF combined with VBC

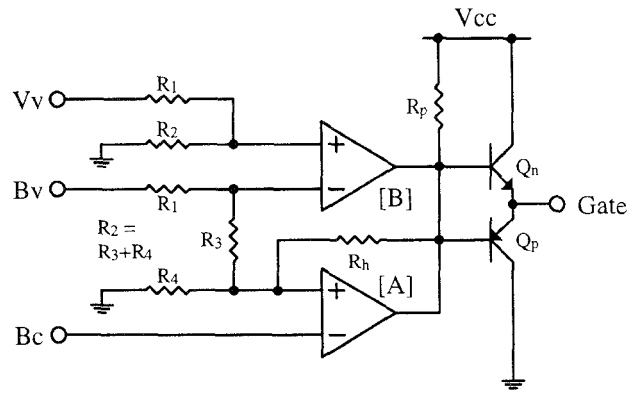


Fig. 7. Simple valley boost converter (VBC) controller

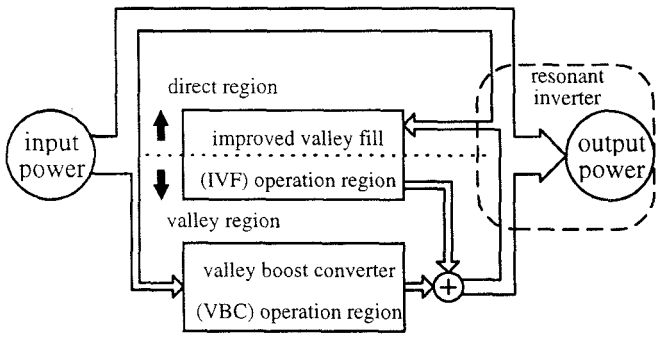


Fig. 8. Power flow in the presented IVF with VBC

voltage with the VBC and the line current is very smooth. The latter results from the facts that the VBC operates in continuous current mode and there is no pulsating line current around the peak by the action of the IVF as mentioned previously.

The VBC has a very simple control circuit which is composed of one chip comparator and several resistors as shown in Fig. 7. The one chip comparator such as LM393 has two internal comparable circuits. The comparator [A] is used for boost action operated in continuous current mode, and the comparator [B] is to guarantee the VBC being operated in the limited valley region.

Fig. 8 is the power flow diagram of the presented IVF combined with the VBC. There are two regions, direct region and valley region. In direct region, the most power of input is supplied to the lamp output directly, and a little input power is stored at the electrolytic capacitors by the IVF operation. In valley region, the VBC as well as the electrolytic capacitors stored in direct region supply the lamp output power. With the addition of the VBC, this scheme has higher valley voltage and more lamp current in the valley region compared with the conventional valley fill. In addition, the lamp current is reduced in the direct region because the resonant inverter transfers the energy from direct region to valley region.

As a result, the lamp current has little double line frequency modulation regardless of the ripple of the dc bus voltage. Thus the lamp current CF of the presented PF correction scheme is more reduced than the that of the IVF and the conventional valley fill. The low lamp current CF is desirable from efficacy and lamp life as stated before.

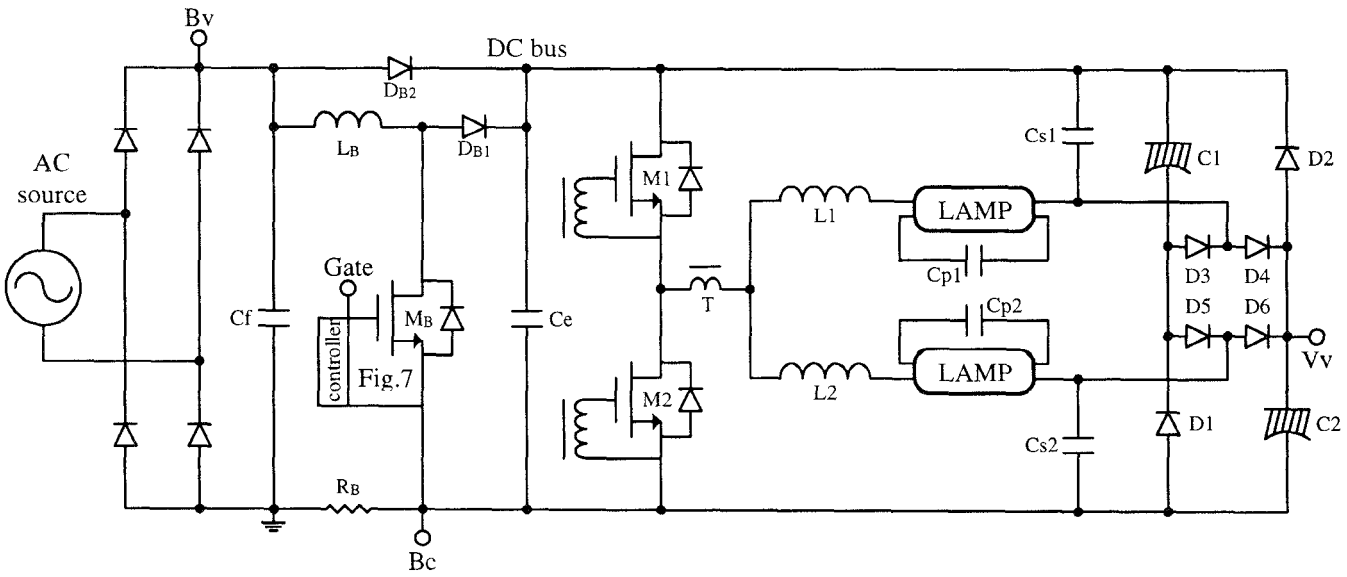
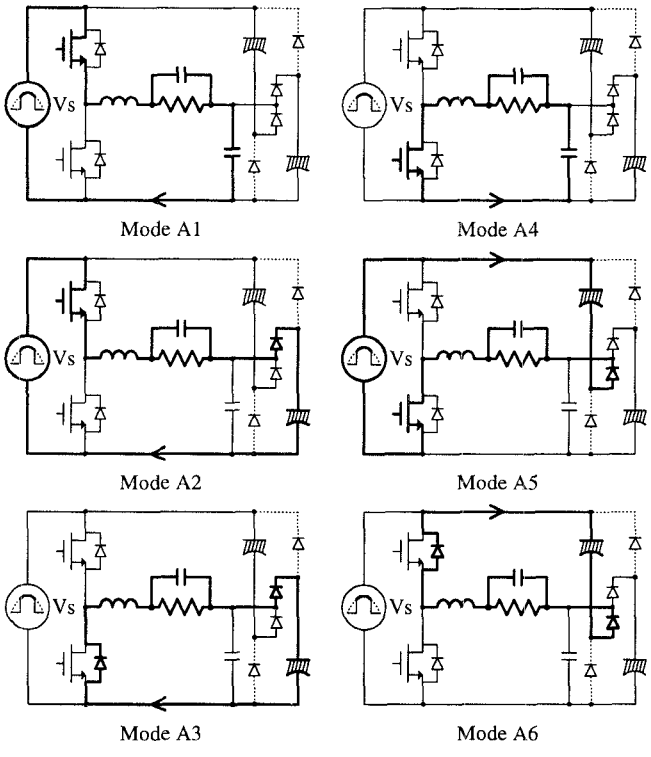
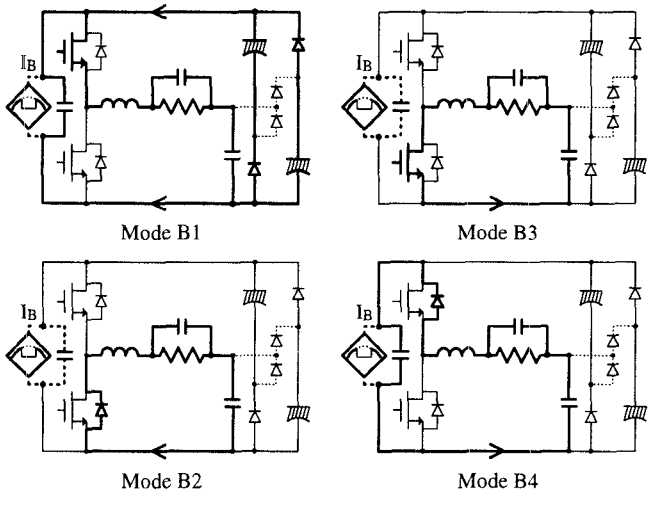


Fig. 9. Overall configuration of electronic ballast for two fluorescent lamps



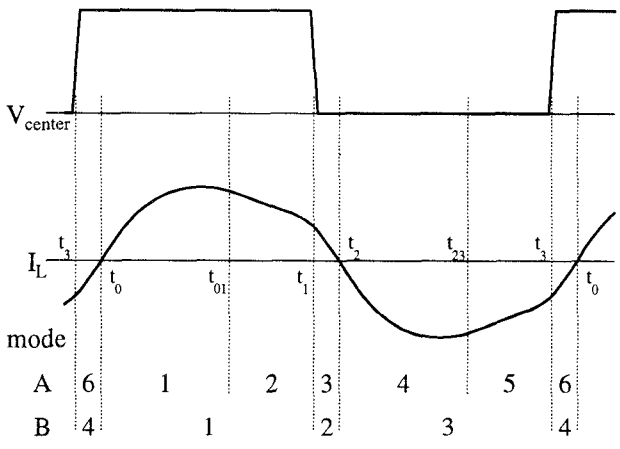
(A) direct region : IVF operation mode



(B) valley region : VBC operation mode

IV. Electronic Ballast having The Presented Power Factor Correction Topology

The overall configuration of the electronic ballast with the proposed circuits is shown in Fig. 9. This is a typical self-excited half-bridge parallel loaded series resonant electronic ballast for two fluorescent lamps. The IVF is connected directly with the series resonant capacitors(Cs1,Cs2). As it were, the reactor in Fig. 2 is shorted to increase the valley



(C) the waveforms of two operation mode

Fig. 10. Mode diagram for one lamp in Fig. 9

voltage as high as possible. Ce is to transfer the current of the VBC into the nearly valley voltage(V_{C1},V_{C2}), and Cf is added to filter out the high frequency component of input line voltage.

Fig. 10 is the operation modes and waveforms of Fig. 9 in the two regions, and is simplified to the equivalent resonant inverter for one lamp (lower lamp of Fig. 9). The explanation of Fig. 10 is described as follows:

(A) direct region : improved valley fill (IVF) operation

In this region, the input ac source supplies the current to the resonant inverter directly and some input current charges up C1 and C2 by the IVF operation. Just before instant t_0, the inductor current I_L decreases to zero with the (-) direction. It flows through the anti-parallel diode of M1 and charges up C1 to store the energy for the valley region. At this interval, M1 is turned on at zero voltage.

Mode A1 (t_0~ t_{01}) : At instant t_{01}, I_L changes the direction from (-) to (+) by resonance and then flows through M1 turned on during previous mode. It goes up and down until V_{Cs} becomes V_{C2}. In this mode, the input line supplies power to the resonant inverter.

Mode A2 (t_{01}~ t_1) : V_{Cs} becomes equal to V_{C2} at instant t_{01} and D6 starts to conduct I_L. The input line supplies power to the resonant inverter as the same as the previous mode and the most energy of C2 is stored in this mode.

Mode A3 (t_1~ t_2) : At instant t_1, M1 is turned off. I_L decreases to zero and freewheels through C2 and the anti-parallel diode of M2. At this interval, C2 is charged up and M2 is turned on at zero voltage.

Mode A4 (t_2~ t_{23}) : At instant t_2, I_L changes the direction to (-) and then freewheels through M2. It goes up and down until V_{Cs} becomes V_{DC}-V_{C1}.

Mode A5 (t_{23}~ t_3) : V_{Cs} becomes equal to V_{DC}-V_{C1} at instant t_{23} and D5 starts to conduct I_L. The input line supplies power to the resonant inverter and the most energy of C1 is stored in this mode.

Mode A6 (t_3~ t_0) : At instant t_3, M2 is turned off. I_L decreases to zero and freewheels through C1 and the anti-parallel diode of M1. At this interval, C1 is charged up and M1 is turned on at zero voltage. By the periodic resonance, the mode A1 is repeated at the end of this mode.

(B) valley region : valley boost converter (VBC) operation

In this region, two voltage sources supply the current to the resonant inverter. One is a pair of C1 and C2, and the other is Ce. A pair of C1 and C2 has been precharged in the previous direct region to transfer the energy into this region. Ce is charged up to nearly V_{C1},V_{C2} by the VBC operation independent of the switching cycle of the resonant inverter. The flow of resonant current and the switching pattern are similar to those of the previous direct region as shown in Fig. 10, so the explanations about these are omitted.

Mode B1 (t_0~ t_1) : Only in this mode, the energy of the resonant inverter is supplied.

Mode B2 (t_1~ t_2) and Mode B3 (t_2~ t_3): The resonant inverter freewheels on the direction of I_L.

Mode B4 (t_3~ t_0) : I_L charges up Ce, so the energy of Ce is restored slightly.

V. Experimental Results

The electronic ballast having the proposed PF correction scheme as shown in Fig. 9 is constructed and tested in the laboratory. The line source voltage is 220Vac and two F40T12 fluorescent lamps are used. The component values of the resonant inverter are the following:

L1=L2 = 2mH, L_B = 1.5mH
Cp1=Cp2 = 8.2nF/1000V, Cs1= Cs2 = 15nF/400V
C1=C2 = 22uF/250V, Ce = 100nF/400V, Cf = 1nF/400V
M1, M2, M_B : IRF740 power MOSFET
D1, D2, D_{B2} : 1N4004 rectify diode
D3~D6, D_{B1} : 1N4937 fast-recovery diode
T : 2/35/35 turns on core EE16/14(TDK)

We confirmed by experiments that the new IVF combined with the VBC operates to the desired results. Fig. 11 shows that the line current is very smooth, because the VBC operates in continuous current mode and there is no pulsating line current around the peak by the action of the IVF. The measured PF and THD is 0.997 and 5%, respectively. Fig. 12 shows that the IVF and the VBC perform their action alternately in every half line period and the valley voltage is very high more than 240V in 310Vp. Fig. 13 and Fig. 14 show that the lamp current is maintained almost constant in spite of the fluctuation of the dc bus voltage. This is due to the fact that by the operation of the presented PF correction scheme, the valley voltage is increased and the lamp current is stabilized during the two regions (direct and valley). The reason of the latter is that the resonant inverter transfer the energy from direct region to valley region, so the lamp current is reduced in the direct region as stated before. It is clear that the lamp current CF is as low as 1.5.

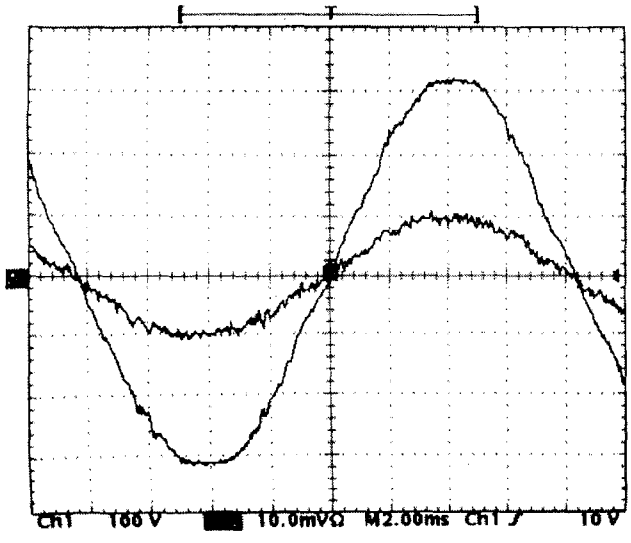


Fig. 11. line voltage (100V/div) & line current (0.5A/div)

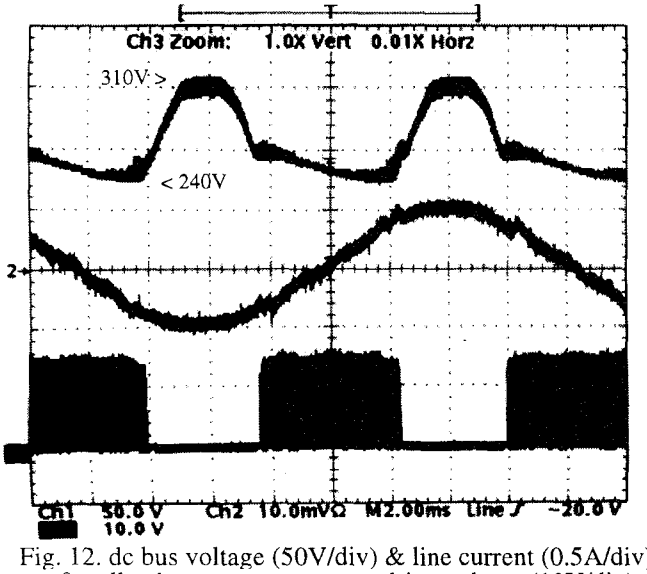


Fig. 12. dc bus voltage (50V/div) & line current (0.5A/div) & valley boost converter gate drive voltage (10V/div)

VI. Conclusion

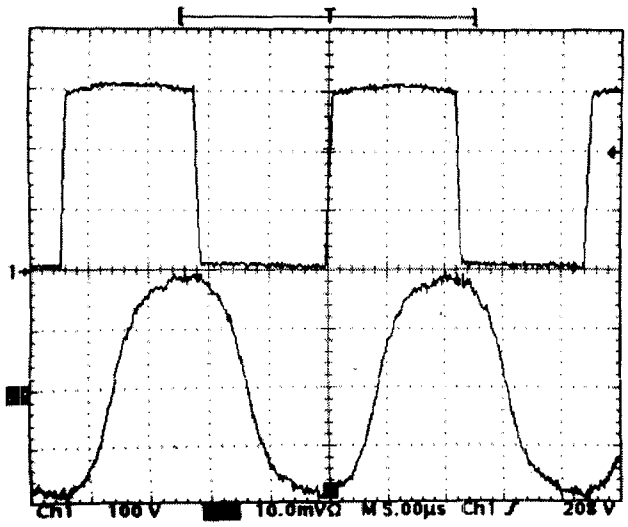


Fig. 13. half bridge center voltage (100V/div) & lamp current (0.2A/div) in maximum dc bus voltage (310V)

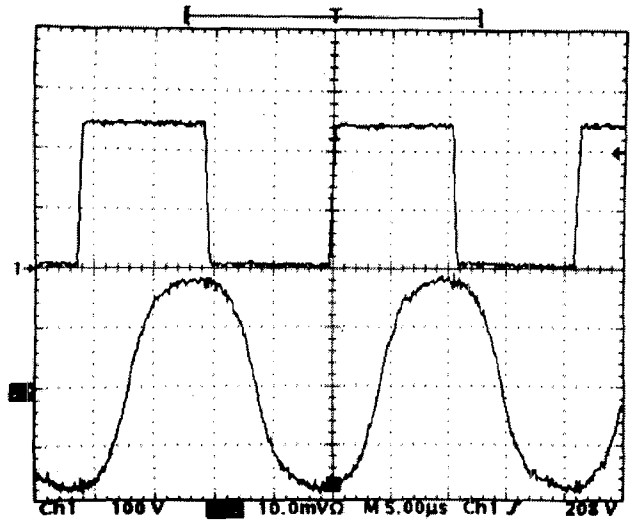


Fig. 14. half bridge center voltage (100V/div) & lamp current (0.2A/div) in minimum dc bus voltage (240V)

We proposed a new valley fill topology, referred to as the Improved Valley Fill (IVF), and the IVF combined with a valley boost converter (VBC) to achieve a unity PF electronic ballast for fluorescent lamp. The IVF can adjust the valley voltage above half the peak line voltage. Around the line peak, hence, there is no pulsating line current which deteriorates the PF and THD. Also, the IVF improves lamp current CF by the energy transfer operation from direct region to valley region. To obtain unity PF, in addition, we combined the IVF with the VBC controlled simply by single chip comparator and several resistors. The VBC in continuous conduction mode operates only during the valley region to decrease the loss and the voltage stress of switching devices and resonant inverter. The valley voltage is much increased by the VBC action. In the experiments, we obtained the PF and THD to 0.997 and 5%, respectively, with quite low lamp current CF about 1.5 by using the proposed circuit.

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