Novel Off-Line Zero-Voltage-Switching PWM AC/DC Converter for Direct Conversion from AC Line to 48VDC Bus with Power Factor Correction

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ABSTRACT

A novel off-line zero-voltage-switching(ZVS) PWM AC/DC converter for single stage preregulation in distributed power system is proposed. The proposed AC/DC converter provides both of input power factor correction and direct conversion from 110-220VAC line to 48VDC bus with single power stage. Comparing to the conventional two-stage approach(boost rectifier followed by off-line DC/DC step down converter), the proposed approach reduces the loss of one power stage. A new simple auxiliary circuit provides zero-voltage-switching(ZVS) condition to all semiconductor devices without imposing additional voltage and current stresses and loss of PWM capability. Operational principle, analysis, control of the proposed converter together with the simulation results of 1KW prototype are presented.

I. Introduction

Recently, the two stage distributed power system was suggested as an alternative to the centralized approach[1-2]. The use of two power conversion stages allows functional partitioning for improved system performance. The first stage, the *line converter(or front-end converter),* provides the isolated 48VDC bus from 110-220VAC line, and the second stage, the *load converters*, are designed to optimize for maximum power density and fast response time. A simplified block diagram of the distributed power system is shown in Fig. 1.

As the line converter, the conventional switching power supply which includes simple diode rectifiers with filter capacitor can be considered. However, it draws pulsating ac line current, resulting in low power factor(generally less than 0.65) and high RMS line current. With the increasing demand for more power and better power quality from a standard 110-220VAC line, this approach(simple diode rectifier followed by DC/DC converter) is no longer suitable as the line converter. To get a high power factor on the line, the use of power factor correction circuit is best way and the boost converter has been popularly used. So, the most common construction of the line converter is completely separated boost converter

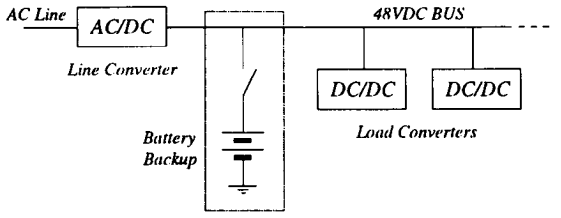

Fig. 1 Block diagram of the distributed power system

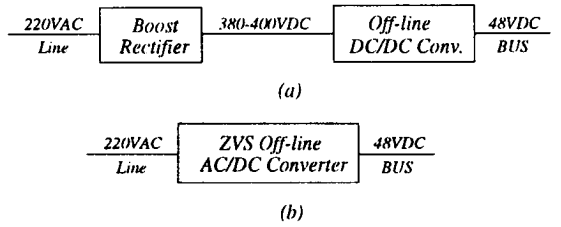

Fig. 2 Block diagram of the line converter with power factor correction: (a) conventional two stage approach, (b) proposed single stage approach.

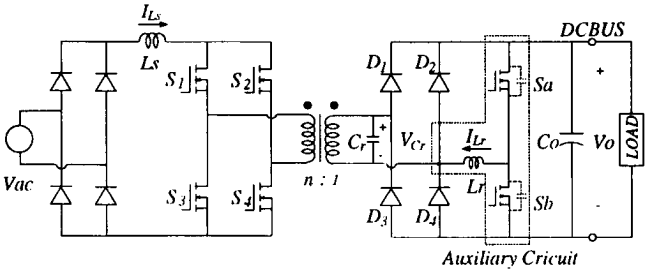

Fig. 3 Circuit topology of the proposed ZVS true PWM AC/DC converter.

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to attain high power factor followed by a off-line step down DC/DC converter to produce the regulated 48VDC output as shown in Fig. 2(a). In the recent years, there have been a great deal of researches on this subject[3-10]. As a result, for both of the boost power factor correction circuit and the off-line step down converter, effective soft switching techniques with modeling, design and control techniques were well established[3-9]. The zero-voltage-transition(ZVT) PWM boost converter[6] and ZVS full-bridge PWM DC/DC converter[7-9] can be effectively used for each application due to their distinctive advantages such as effective ZVS, minimum device voltage and current stresses, simple circuit topology, etc. Even though each of them is well optimized, this approach is inefficient and costly as the power is converted twice. Overall system is rather complex because both have the auxiliary circuit for ZVS, control circuits, and sensing circuits, etc. To overcome this problem, an approach of single stage line converter was suggested by using PWM and zero-current-switching(ZCS) quasi resonant-SEPIC converter to achieve input power factor correction and direct conversion from 110-220VDC line to 48VDC bus[10]. Its available power range, however, is very low because of the switching loss and/or the very high device voltage and current stresses. So, it is also not effective one as line converter since the high power capacity is generally required for distributed power systems.

In this paper, a novel off-line ZVS PWM AC/DC converter is proposed for single stage line conversion. The proposed AC/DC converter is basically a full bridge PWM boost converter as shown in Fig. 3. A new simple auxiliary circuit which operates only on switching instants once a switching cycle, provides ZVS condition to all semiconductor devices. The PWM operation of the proposed converter can be achieved under minimum device voltage and current stresses. With a single power stage, it is possible to achieve a sinusoidal line current at unity power factor as well as the isolated 48VDC output. The output voltage can be directly used as DC bus for distributed power systems as shown in Fig. 2(b). Comparing to that of the conventional approach(Fig. 2(a)), overall efficiency of the proposed converter is highly improved due to effective ZVS of all devices as well as single stage power conversion and the overall system is quite simplified. Thus, it can be operated at high switching frequency(up to several hundreds of KHz) allowing use of small size input inductor. Minimum device voltage and current stresses make it high power(up to several KW) application possible. Operational principle, analysis and control of the proposed converter are shown. Practical design consideration and simulation results of 1 KW prototype are also presented.

II. Operational Principle

The basic structure of the proposed AC/DC converter is a full bridge boost converter with isolation transformer as shown in Fig. 3. The high frequency transformer provides electrical isolation and extend the control range of output voltage to lower level of the input voltage according to its turn ratio. The simple auxiliary circuit which includes resonant inductor, resonant capacitor and two active devices, operates only on switching instants to provide ZVS condition to all semiconductor devices.

To illustrate basic operation of the proposed converter, all input devices and components are assumed ideal and the AC input voltage is treated as a constant DC voltage source during a switching period. Fig. 4 shows operational mode diagrams of the proposed converter. One switching cycle can be divided into eight mode and conduction paths in the converter circuit for each mode are denoted by solid line. Fig. 5 shows the corresponding waveforms for each mode.

Mode 1: Four primary switches are turned on and the input inductor current I_{Ls} is linearly increased with the initial current I_1 as follows:

$$I_{Ls}(t) = \frac{V_s}{Ls} t + I_1. \tag{1}$$

The inductor current at the end of this mode can be given by

$$I_{Ls}(T_{M1}) \equiv I_2. \tag{2}$$

where, T_{M1} is the time interval of mode 1.

Mode 2: After on-duty period, the cross part switches S_2, S_3 are turned off. The input inductor current is rushed into the resonant capacitor C_r and the capacitor voltage V_{Cr} is

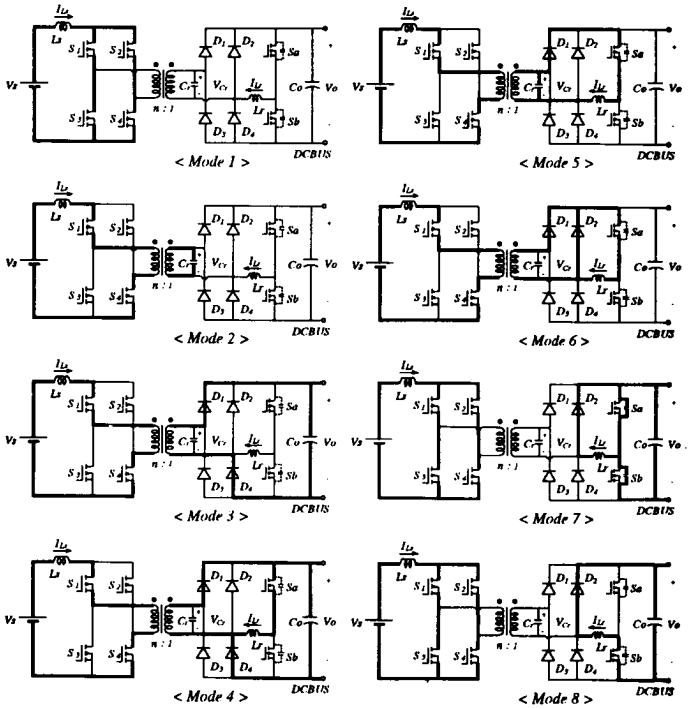

Fig. 4 Operational mode diagrams of the proposed converter (AC input voltage source is treated as a DC one during a switching period).

increased almost linearly because the input inductor is large enough to be treated as a constant current source during this mode. This turn-off process is virtually lossless because the resonant capacitor limits the instantaneous rate of rise of the primary switch voltage. It is noted that the ZVS is achieved without any assistance of the auxiliary circuit. In the next switching cycle, however, the other two switches S_1, S_4 should be turn off to prevent the transformer from going saturation. The resonant capacitor voltage is given by

$$V_{Cr}(t)=\frac{nI_2}{Cr}t. \tag{3}$$

and the time interval of this mode T_{M2} is obtained from the condition of $V_{Cr}(T_{M2})=V_o$ as follows:

$$T_{M2}=\frac{Cr}{nI_2}V_o. \tag{4}$$

Mode 3: The resonant capacitor voltage is clamped with the output voltage by conducting the secondary bridge diodes D_1, D_4. The input inductor current is linearly decreased as follows:

$$I_{Ls}(t)=I_2-\frac{nV_o-V_s}{Ls}t. \tag{5}$$

The inductor current at the end of this mode can be given by

$$I_{Ls}(T_{M3})=I_2-\frac{nV_o-V_s}{Ls}\cdot T_{M3}\equiv I_3. \tag{6}$$

Mode 4: To terminate the off-duty period, the off-state primary switches S_2, S_3 should be turned on. At this situation, the ZVS condition can not be obtained from the main circuit itself. To provide ZVS conditions to secondary diodes to be turned off as well as primary switches to be turned on, the auxiliary switch S_a is turned on and then, the resonant inductor current I_{Lr} is linearly increased up to $nI_{Ls}(t)$. The $I_{Lr}(t)$ and $I_{Ls}(t)$ are given by

$$I_{Lr}(t)=\frac{V_o}{Lr}t, \tag{7}$$

$$I_{Ls}(t)=I_3-\frac{nV_o-V_s}{Ls}t. \tag{8}$$

The time interval of this mode T_{M4} can be obtained from the condition of $I_{Lr}(T_{M4})=nI_{Ls}(T_{M4})$ and the I_{Ls} at the end of this mode can be given by

$$I_{Ls}(T_{M4})\equiv I_4. \tag{9}$$

Mode 5: When the I_{Lr} is reached to nI_4, the secondary diode D_4 is turned off with both of ZVS and ZCS conditions as shown in Fig. 5. Then, the Lr and Cr start to resonate and the V_{Cr} is decreased until it reaches to zero. The $I_{Lr}(t)$ and $V_{Cr}(t)$ are given by

$$I_{Lr}(t)=\frac{V_o}{Zr}\cdot\sin(\omega_r t)+nI_4, \tag{10}$$

$$V_{Cr}(t)=V_o\cdot\cos(\omega_r t). \tag{11}$$

where, $Z_r=\sqrt{Lr/Cr}$, $\omega_r=1/\sqrt{LrCr}$. From the condition of $V_{Cr}(T_{M5})=0$, the T_{M5} is obtained as follows:

$$T_{M5}=\frac{\pi}{2}\sqrt{LrCr}. \tag{12}$$

Mode 6: When the V_{Cr} is reached to zero, the diode D_2 start to conduct. The resonant inductor current I_{Lr} freewheels though S_a and D_2 while the input inductor current I_{Ls} flows through D_1 and D_2. During this mode, the primary voltage is always zero and the off-state switches S_2, S_3 can be turned on with complete ZVS condition. The time interval of this mode can be adjusted for convenience of the switch control.

Mode 7: The primary switches S_2, S_3 are turned on with complete ZVS condition and then, the secondary diode D_1 is turned off with complete ZVS condition, too.
The I_{Ls} starts to increase again. In addition, the auxiliary switch S_a is turned off to recover the energy of resonant inductor to the output capacitor. This turn-off process is also lossless due to snubber action of the internal capacitor of MOSFETs. The time interval of this mode is very short enough to neglect because the internal capacitance of the auxiliary MOSFETs is very small comparing to Cr. So, the waveforms for this mode is omitted in Fig. 5.

Mode 8: The input inductor current is continuously increased and it is given by

$$I_{Ls}(t)=\frac{V_s}{Ls}t+I_4, \tag{13}$$

if the variation of I_{Ls} during mode 5 to mode 7 is neglected. The resonant inductor current is recovered to output capacitor through D_2 and the body diode of the MOSFET S_b

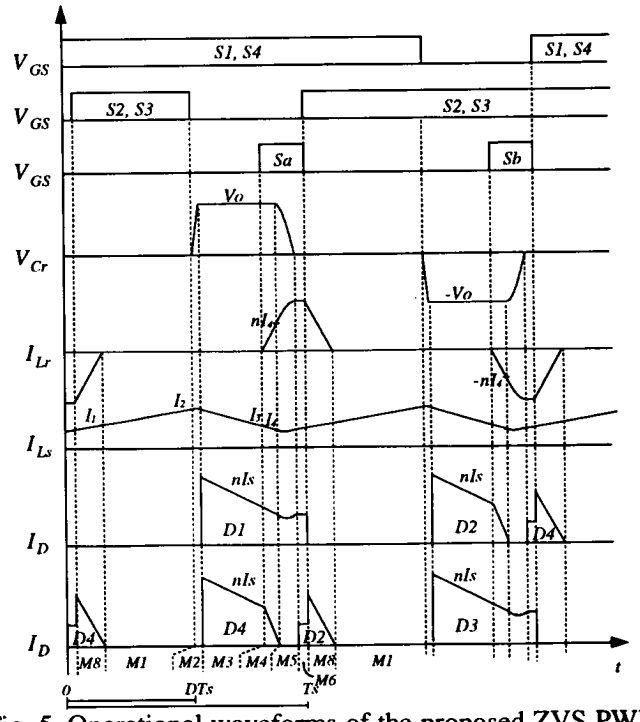

Fig. 5 Operational waveforms of the proposed ZVS PWM AC/DC converter.

until it dies out as follows:

$$I_{Lr}(t)=\frac{V_o}{Zr}+nI_4-\frac{V_o}{Lr}t. \tag{14}$$

The time interval of this mode T_{M8} is obtained from the condition of $I_{Lr}(T_{M8})=0$ as follows:

$$T_{M8}=\frac{Lr}{V_o}\cdot\left(nI_4+\frac{V_o}{Z_r}\right). \tag{15}$$

One switching cycle is completed at the end of mode 8 and complete switching waveforms are shown in Fig. 5. It can be seen that the waveforms of the input inductor current and voltage of main switches are almost same as those of the hard switched PWM boost converter. If the proposed converter is operated by PWM, the sum of time durations of mode 6, mode 8 and mode 1 will be on-duty of switching period while the sum of remained time will be off-duty. It can be seen that the basic operation and waveforms are very similar to those of the ZVT PWM boost converter[6].

III. Control Strategy

The main control object is to shape the line current into a sinewave keeping in phase with the line voltage and regulate the output voltage to the desired reference. This results in near unity power factor and greatly reduces line current harmonics. The regulation of output voltage with standard 48VDC bus leads to the direct power conversion from AC line to DC bus, which greatly improves the overall efficiency. The overall control block diagram is shown in Fig. 6.

The AC line current is shaped to follow a sinusoidal reference current. The reference current is in phase with the line voltage and has correct magnitude to supply the necessary power to the load as shown in Fig. 6. For input power factor correction and output voltage control of the boost converter, several algorithms have been reported[3-5,10]. Among them, nearly all algorithms can be used for the proposed converter. To test the performance of the proposed converter, one of well known algorithm, constant frequency PWM control with PI controller, is considered as shown in Fig. 6. To avoid very fast switching action of the switches at the end of a rectified line cycle, where the voltage approaches zero, a small dead time is introduced. The input power factor will decrease with the length of dead time(θ)[4] and it is given by

$$pf=\sqrt{\frac{1}{\pi}(\pi-2\theta+\sin 2\theta)}. \tag{16}$$

The regulation of output voltage is accomplished by varying the amplitude of the reference of input current. The output voltage control loop can be effectively controlled by applying the discrete control theory[5]. The discrete PI controller with 120 Hz sampling frequency is used for regulation of the output voltage as shown in Fig. 6. The output voltage is sampled once per cycle and a new magnitude of the reference current is calculated as follows;

$$I_M(k+1)=I_M(k)+\alpha\cdot(V_{o\_ref}-V_o) \tag{17}$$

where, $k=0,1,2,\cdots$. The sampling of output voltage is taken at the zero crossing of the ac source voltage to minimize the influence of the 120 Hz ripple in the output voltage.

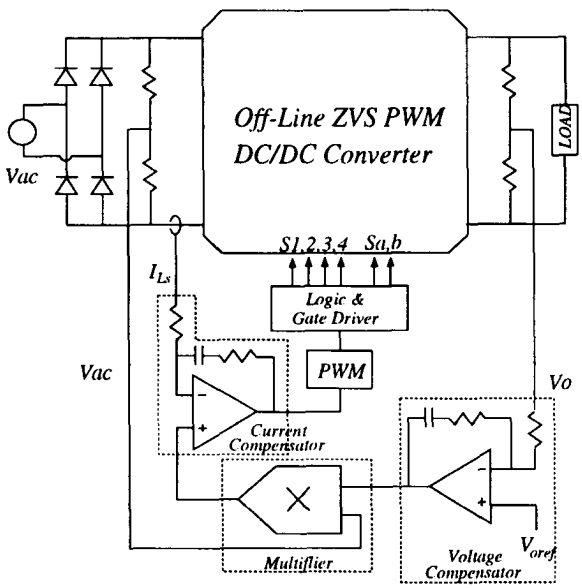

Fig. 6 Block diagram of the output voltage control with input power factor correction.

IV. Novel Features and Characteristics

A. Direct Conversion from AC Line to 48VDC Bus

The 48VDC is commonly used for DC bus in distributed power supply systems as shown in Fig. 1. To obtain 48VDC from 110 or 220VAC line with high input power factor, the line converter includes the functions of power factor correction as well as output voltage regulation. Thus, the most common construction of the line converter is boost converter to obtain high input power factor followed by off-line step down converter to obtain the regulated 48VDC output. In the proposed converter, however, the 48VDC output is directly obtained from AC line with single power stage. Comparing to the conventional two stage approach, the proposed approach saves the loss of one power stage. Therefore, the circuit topology and controller are quite simplified and the overall efficiency is considerably increased.

B. Effective ZVS for Active and Passive Devices

As shown in Fig. 3, the proposed converter is basically full bridge boost converter and a new simple

auxiliary circuit is adopted to provide ZVS conditions to all semiconductor devices. Since the auxiliary circuit is inserted into the secondary rectifier side, the feature of ZVS of the secondary diodes is somewhat different from that of the other ZVS converters. The secondary rectifying diodes are switched under both of ZCS and ZVS conditions while the active devices(MOSFETs) are switched under ZVS condition only. This novel feature is very important for high voltage, high frequency applications because the dominant portion of switching loss in the high voltage, high frequency switching power supplies is generally due to loss by diode reverse recovery rather than that of the active devices(MOSFETs., IGBTs, etc.). The switching waveforms of the diodes under several conditions are comparatively illustrated in Fig. 7. Fig. 7(a) shows the typical hard switching waveforms of diodes and it can be seen that the reverse recovery problem is quite series and results in a large amount of switching loss and EMI. Fig. 7(b) shows the switching waveforms under ZCS condition. The peak reverse recovery current is alleviated but the some amount of switching loss is still remained. Fig. 7(c) shows the switching waveforms under ZVS condition. The peak reverse recovery current is very high but the loss is decreased due to soften reverse voltage. Fig. 7(d) shows the switching waveforms under both of ZCS and ZVS conditions. It can be seen that the switching loss is almost zero and EMI noise level is very low due to soften voltage waveforms. So, the proposed converter can be operated in the range of very high voltage, high frequency with high efficiency and low EMI noise.

The auxiliary circuit operates only when the secondary diode are turned off, once a switching cycle, and its operation interval is very short with respect to the switching period. So, the rating of auxiliary devices can be very small compared to the main devices and the conduction loss in the auxiliary circuit is also very small.

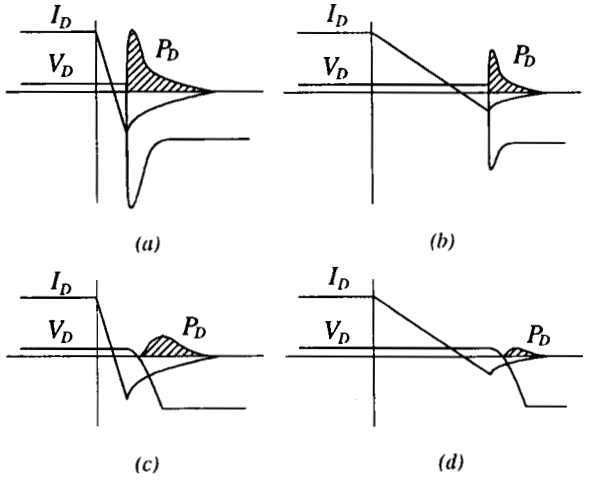

Fig. 7 Illustrative switching waveforms of diodes under the condition of (a) hard switching, (b) ZCS only, (d) ZVS only, and (d) both ZVS and ZCS.

C. Conserved PWM Converter Characteristics

Most of ZCS or ZVS converters which have been presented in the literature are constructed by including resonant inductor(s) and capacitor(s) to the hard switching PWM converters(e.g. Series or Parallel Resonant Converters(SRCs or PRCs), Quasi-Resonant Converters(QRCs), Multi-Resonant Converters(MRCs), etc.). The ZCS or ZVS condition is achieved by the resonance between resonant inductor(s) and capacitor(s). In these converters, the resonant inductor(s) and capacitor(s) are located at the main power flow path. This results generally high device voltage and/or current stresses, loss of PWM capability, limited ZCS or ZVS range, and sometimes nonlinear characteristics. From Fig. 3, it can be seen that the resonant inductor and capacitor, however, are located completely out of the main power flow path and the resonance takes place only during switching instants. As a result, the switching waveforms of the main devices are almost same as those of the PWM converter and the PWM operation is always possible. All devices including auxiliary devices are subjected to minimum voltage and current stresses and the ZVS is maintained for the whole load and line range. Therefore, almost all of characteristics of the conventional hard switching PWM converters are conserved in the proposed converter and thus, most of modeling, design, and control techniques for PWM converters can also be used for the proposed converter.

V. Practical Design Considerations

A. Parasitic Ringing in Primary Side

The ZVS-PWM-FB converter[7-9] achieves ZVS condition using the stored energy in the leakage inductance of transformer. So, the transformer is designed so that the leakage inductance is large enough to maintain ZVS for the given load range. The interaction between the leakage inductance and the parasitic capacitance of secondary diodes causes severe voltage overshoot and ringing across the diodes. In the proposed converter, the similar ringing effect arises in the primary side due to interaction between the parasitic capacitance of the primary devices and the leakage inductance. If the transformer is designed with allowing large leakage inductance, the high voltage overshoot will arise in the primary side and this implies the use of higher voltage rating devices. In addition, the instantaneous rate of rise of the primary device voltage at turn-off will be very high since the secondary resonant capacitor Cr is separated from the primary side by the leakage inductance and the parasitic capacitance of the primary devices are rather small. This results additional switching loss in the primary devices due to imperfect ZVS.

To reduce the voltage overshoot and ringing effect, first of all, it is desirable to minimize the transformer leakage inductance. It is noted that the leakage inductance is unwanted component in the proposed converter. Second,

a small capacitor can be added to the primary side as shown in Fig. 8 to reduce the rate of rise of the device voltage at turn-off, which reduces the switching loss as well as the ringing effect. Fig. 9 shows the primary and secondary device voltage waveforms at turn-off of the primary devices with and without the additional capacitor C_p. It can be seen that the rate of rise of the primary voltage and peak ringing voltage are considerably reduced by adding additional C_p, comparing to those of the waveforms without C_p. Optimum value of C_p is obtained from several computer simulation runs. The small ringing shown in Fig. 9(b) will be rapidly died out by the damping elements such as transformer dynamic resistance, conduction drop of devices, etc. For the protection of the primary devices, the clamping circuit[7] and the active snubber[9] can also be used. The clamping circuit, however, is simpler and better

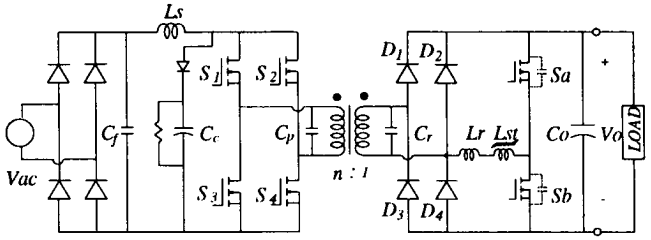

Fig. 8 Practical circuit diagram of the proposed converter.

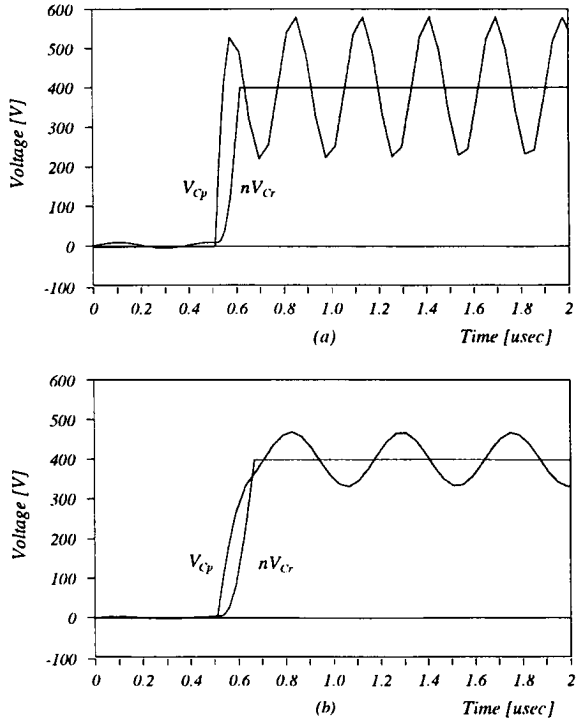

Fig. 9 Voltage waveforms of primary and secondary sides at turn-off of the primary devices: (a) without additional C_p , (b) with $C_p = 1[nF]$, (circuit parameters of Table 1 are used and equivalent parasitic capacitance of primary devices is assumed as 500[pF]).

for the proposed converter as shown in Fig. 8 since the ringing energy is very small due to small leakage inductance.

B. Parasitic Ringing in Auxiliary Circuit

There is another ringing effect in the proposed converter. The interaction between the resonant inductor and the parasitic capacitance of auxiliary devices also causes ringing effect. However, it can easily be eliminated by adding a saturable inductor in series with the resonant inductor. The practical circuit diagram of the proposed converter considered the parasitic ringing effect and device protection is shown in Fig. 8.

VI. Simulation Results

In order to verify the operational principles and test the performance of the proposed ZVS off-line AC/DC converter, The computer simulation is done by using Pspice with the parameters as listed in Table 1.

Table 1. Parameters used in Simulation.

Nominal Line Voltage(V_{ac})	220 *VAC*
Output Voltage(V_o)	48 *VDC*
Output Power(P_o)	1 *KW*
Resonant Inductor(L_r)	4 μ*H*
Resonant Capacitor(C_r)	0.1 μ*F*
Input Inductor(L_s)	1 *mH*
Output Capacitor(C_o)	6800 μ*F*
Transformer Turn Ratio(n)	8
Switching Frequency(fs)	60 *KHz*

Fig. 10 shows waveforms of input inductor current, resonant inductor current and capacitor voltage, and secondary diode currents. The appearance of small ringing in waveforms is caused by the interaction between parasitic inductors and capacitors. It can be seen that all waveforms are well matched with the theoritical ones. Fig. 11(a) shows the waveforms of input voltage and current and output voltage. It can be seen that the input current waveforms show sinusoidal waveforms keeping in phase with input voltage. The dead angle is set to 10 degrees and the calculated input power factor is 0.99. Fig. 11(b) shows the frequency spectrum of the input current harmonics and it can be seen that the harmonic contents of input current is very low. The output voltage is regulated to the reference voltage, 48VDC. The proposed converter, however, has a demerit of 120 Hz ripple in the output voltage, which is about 5% of V_o in this case. However, it may not be any problem, if the line regulation capabilities of the load converters are good enough to reject the 120 Hz ripple voltage.

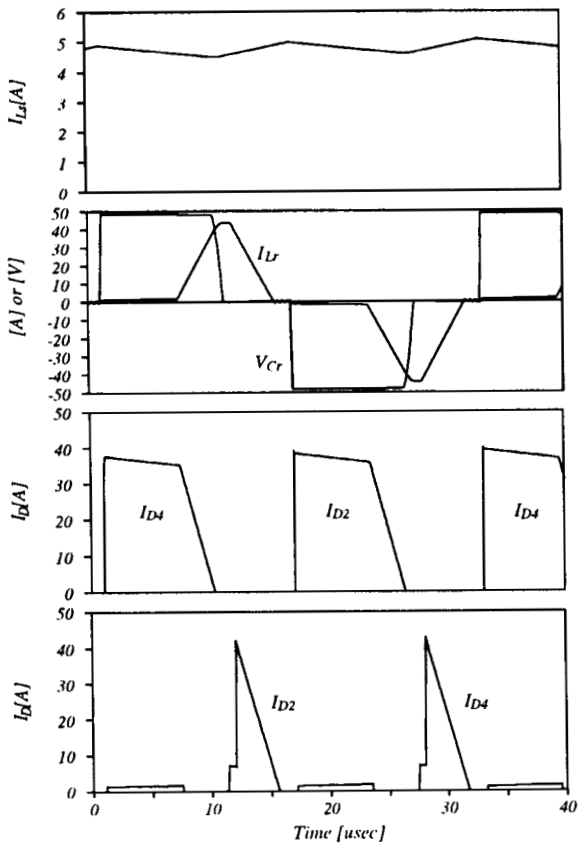

Fig. 10 Simulated switching waveforms: input inductor current, resonant inductor current and capacitor voltage, and secondary diode currents.

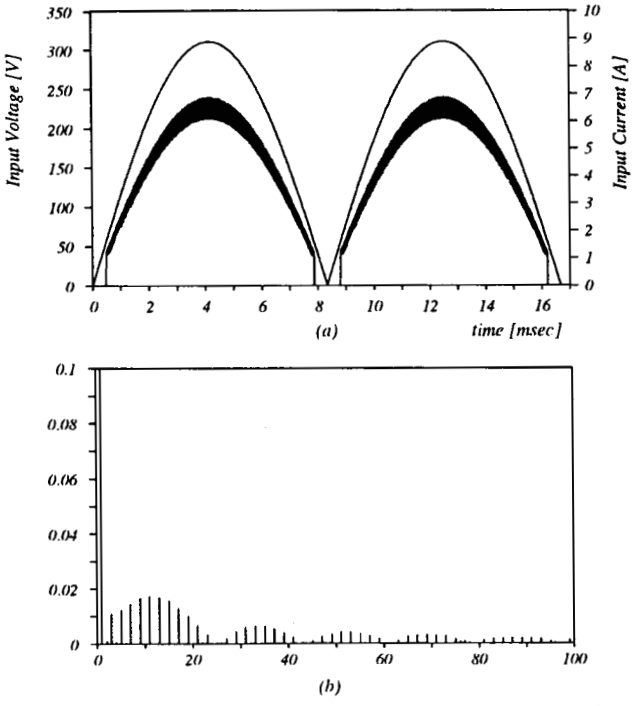

Fig. 11 Simulated waveforms; (a) input voltage and current and output voltage, (b) frequency spectrum of input current harmonics.

VII. Conclusion

A novel off-line ZVS PWM AC/DC converter for single stage preregulation in distributed power systems is presented. Operation, analysis and control of the proposed converter are described and computer simulation is done with 1 KW power level. It is shown that the proposed converter provides both of input power factor correction and the direct conversion from 110-220VAC line to 48VDC bus with single power stage. Due to distinctive advantages including simple topology, high efficiency due to single power stage conversion and effective ZVS, low EMI, minimum device voltage and current stresses and PWM capability, the proposed converter can be thought to be effectively used for high power, high frequency power factor correction circuit, especially for line converter in distributed power supply systems.

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