A HIGH VOLTAGE LARGE CAPACITY DYNAMIC VAR COMPENSATOR USING MULTILEVEL VOLTAGE SOURCE INVERTER

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ABSTRACT

A multilevel PWM voltage source inverter, especially five-level one, is introduced to a static Var compensator(SVC) as a large scale power source. The SVC can be directly connected to ac mains of 6600 volts allowing full utilization of semiconductor devices like GTOs. The voltage balancing condition of the DC side capacitors is pointed out based on the fundamental circuit modeling of the inverter and a five-level PWM is employed to meet the condition. Owing to multilevel approach, a low distortion in the input currents results and thus, filter size is minimized.

I. INTRODUCTION

It is well known that a voltage source inverter(VSI) can be used as a static Var compensator(SVC) supplying fundamental reactive power. Capability of controlling the magnitude and phase as well as frequency of the output voltage in VSI provides continuous variation of leading or lagging reactive power supplied to the ac mains. In addition, the SVC has not only less and smaller reactive components which may result in smaller size, weight and cost but also some possibility of eliminating or suppressing harmonic components in the ac mains [1][2][3].

For a large scale Var compensation, however, high power/high voltage VSIs have their limitations to handle high power/high voltage and to operate at high switching frequency due to lack of high power self commutated semiconductor switches with high switching frequency characteristics (>1kHz). Moreover, various PWM switching strateges are no longer applicable to such large scale SVC systems. Hence, the high power/high voltage VSI is indispensable to large scale SVC system and we can say that the structure of the inverter primarily affects the system performance along with several control schemes [1][2].

So far, conventional high power VSIs should be made up of either problematic series/parallel switch combinations or several small inverter combinations. Of them, multiple inverter systems with coupling components such as transformers have been accepted as a reasonalble solution to cope with such high power applications, which makes it possible to utilize the switching devices at hand relatively easily. In addition, the multiple inverter system provides multilevel output voltages and thus it is also preferred in the context of harmonic reduction. But to prevent excessive harmonic current injection into the network, either a number of inverter stages or several harmonic filter legs should be employed and thus such an SVC system becomes expensive,

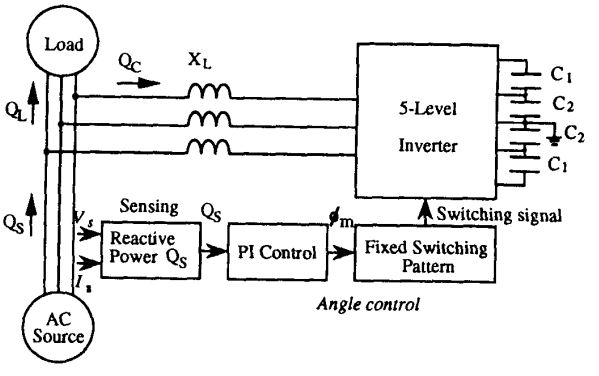

Fig. 1. Block diagram of the SVC system with five-level inverter.

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complicated and large in volume and thus may suffer from system derating [2][5].

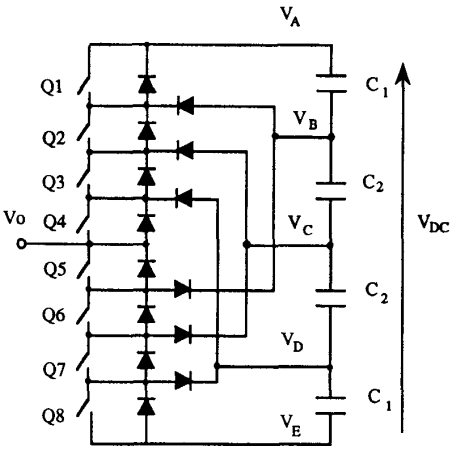
Recently, a general circuit structure of multilevel inverter has been reported [4]. The multilevel inverter can realize any multilevel PWM strateges which lead to harmonic reduction and provides full utilization of presently available semiconductor devices like GTOs especially in high power range where high voltage could be applied.

This paper suggests a high power/high voltage three phase SVC with the multilevel VSI, especially five-level inverter. It is pointed out that the multilevel PWM for the control of the SVC system has some features such that the multilevel modulation index depend on the values of DC side capacitors to meet the DC side voltage balancing. The DC side voltage balancing is basically required in order for the inverter to operate with allowable voltage stress at each active devices. The description of the compensator circuit, the modeling of the SVC system in the fundamental frequency domain, the DC capacitor voltage balancing condition and a five-level PWM scheme taking into account the balancing condition are presented.

II. System Description

Fig. 1 shows the SVC system diagram presented in this paper. The SVC system consists of a multilevel PWM voltage source inverter, especially five-level one, a set of linked AC reactor X_L and series connected DC capacitor tank, linear load considering only Var compensation and the ac mains. The five-level VSI plays a key role in the system which has a capability of controlling the amplitude and the phase for the output phase voltage.

The actual structure of the the five-level PWM inverter presented in [4] is shown in Fig. 2(a) and the associated basic switching table is followed in Fig. 2(b). Note that the voltage stress of each active switches is clamped to only one capacitor voltage and thus the semiconductor power devices could be fully utilized. Moreover, the circuit structure allows the five-level PWM which would result in relatively low harmonics in the line current and thus smaller filter size. Also, using the multilevel inverter makes it possible to eliminate the bulky transformer which is usually required to get the



(a)

Vo	V_A	V_B	V_C	V_D	V_E
Q1	1	0	0	0	0
Q2	1	1	0	0	0
Q3	1	1	1	0	0
Q4	1	1	1	1	0
Q5	0	1	1	1	1
Q6	0	0	1	1	1
Q7	0	0	0	1	1
Q8	0	0	0	0	1

1 = ON, 0 = OFF

(b)

Fig. 2. (a) A pole of the five-level inverter, (b) Basic switching table for the five-level inverter.

appropriate input voltage at AC side of the inverter.

The SVC system requires no separate DC sources for the DC side capacitors and some active power would be supplied through the inverter by means of controlling the phase angle of the inverter. Then, the switching pattern and thus modulation index M_i for the inverter will be fixed. A kind of programmed PWM is adopted considering some requirements such as stable operating condition, elimination of unwanted harmonics, reduction of current harmonics and thus filter size and so on.

Fig. 3 shows the block diagram of the Var control in the system. Controlling Var injected/absorbed from the inverter into the network can be performed as follows. Sensing the source reactive power Q_S at the ac mains imposes the reactive power Q_I which should be compensated by the inverter. In other word, Q_S indicates error quantity between Var demand in the load side and Var supplied by the inverter. The control target is to regulate Q_S to be zero by means of adjusting the phase angle ϕ_m of the inverter. When $Q_S = 0$, $\phi_m = 0$ and the output phase voltage of the inverter becomes in phase with the line-to-neutral voltage in the ac mains.

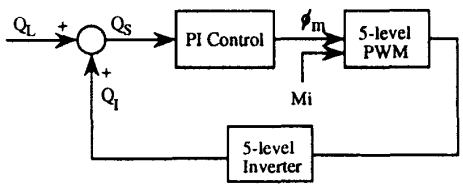


Fig. 3. Control block diagram of the SVC system.

III. MODELING OF THE SVC SYSTEM

Fig. 4 shows the schematic of the SVC system consisting of series connected DC side capacitors and the five-level PWM inverter which is connected to the ac mains through linked reactors. A pole of the five-level inverter can be regarded as a multiplexer which may be switched to any DC side potentials according to the multilevel PWM strategy employed. Utilizing these DC voltages, the objective of the five-level PWM adopted is to produce the output voltage waveform as sinusoidal as possible despite switching operation. The source voltages with angular speed ω are assumed ideal and balanced ones and are given as follows:

$$v_{sa} = V_{sa}\sin(\theta) \tag{1}$$

$$v_{sb} = V_{sb}\sin(\theta - \frac{2\pi}{3})$$

$$v_{sc} = V_{sc}\sin(\theta + \frac{2\pi}{3})$$

Fig. 5 illustrates the five-level PWM assuming balanced switching. Then, the respective existence functions d_1^a through d_5^a can be expressed as follows:

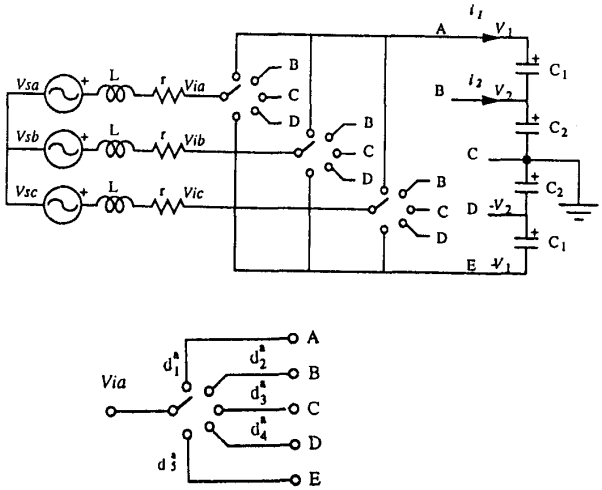


Fig. 4. (a) The schematic of five-level inverter, (b) A switch model as a multiplexer.

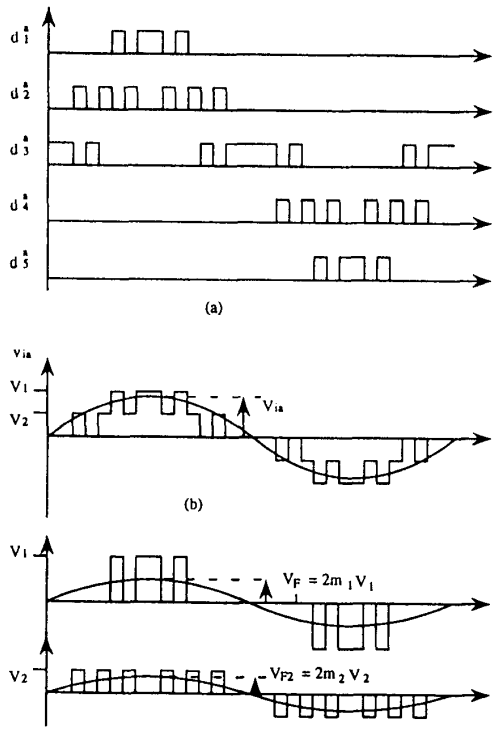


Fig. 5. (a) Existence functions, (b) the resultant output phase voltage, (c) decomposition of five-level PWM into two three-level PWMs.

$$d_1^a = D_1 + m_1 \sin(\theta + \phi_m) \quad (2)$$

$$d_2^a = D_2 + m_2 \sin(\theta + \phi_m)$$

$$d_3^a = D_0 + m_0 \sin(\theta + \phi_m)$$

$$d_4^a = D_2 - m_2 \sin(\theta + \phi_m)$$

$$d_5^a = D_1 - m_1 \sin(\theta + \phi_m) .$$

Eq. (2) represents only the DC and fundamental components of the corresponding existence function and thus will be free from a specific five-level PWM strategy. The superscript in Eq. (2) denotes a-phase quantity and ϕ_m is a phase angle of the inverter with respect to the AC source voltage. Thus,

$$d_n^b(\theta) = d_n^a(\theta - \frac{2\pi}{3}) \quad (3)$$

$$d_n^c(\theta) = d_n^a(\theta + \frac{2\pi}{3})$$

with $n = 1, \cdots, 5$. Therefore, the fundamental component of the output phase voltage can be found to be

$$v_{ia} = d_1^a v_1 + d_2^a v_2 + d_3^a(0) + d_4^a(-v_2) + d_5^a(-v_1)$$

$$= (2m_1 v_1 + 2m_2 v_2) \cdot \sin(\theta + \phi_m) \quad (4)$$

Similarly,

$$v_{ib} = (2m_1 v_1 + 2m_2 v_2) \cdot \sin(\theta + \phi_m - \frac{2\pi}{3}) \quad (5)$$

$$v_{ic} = (2m_1 v_1 + 2m_2 v_2) \cdot \sin(\theta + \phi_m - \frac{2\pi}{3}) \quad (6)$$

Note that a five-level PWM can be decomposed into two three-level PWM's as shown in Fig. 5(c), so that a five-level PWM has not two control variables, modulation index controlling the amplitude and phase angle, but three, that is, m_1, m_2 and ϕ_m. Fig. 6 depicts decomposition of a five-level PWM. In Fig. 6, two three-level inverters seems to be series connected in that their single-pole-triple-throw switches are exclusively grounded. Then, each three-level modulation indexes are defined as

$$M_1 = 2m_1 \quad (7)$$

$$M_2 = 2m_2$$

On the other hand, the DC side currents flowing into each nodes connecting the capacitors depend on the AC side line currents and the corresponding existence functions as follows:

$$i_1 = \mathbf{d}_1^{abc} \cdot \mathbf{i}_{abc} \quad (8)$$

$$= m_1 \cdot \mathbf{SIN}(\theta + \phi_m) \cdot \mathbf{i}_{abc}$$

where

$$\mathbf{d}_1^{abc} = [\, d_1^a \;\; d_1^b \;\; d_1^c \,], \quad \mathbf{i}_{abc} = [\, i_a \;\; i_b \;\; i_c \,]^T \quad (9)$$

$$\mathbf{SIN}(\theta + \phi_m) =$$

$$[\, \sin(\theta + \phi_m) \;\; \sin(\theta + \phi_m - \frac{2\pi}{3}) \;\; \sin(\theta + \phi_m + \frac{2\pi}{3}) \,] \quad (10)$$

Driving Eq. (8), no assumption is made for the AC line currents. Similarly,

$$i_2 = \mathbf{d}_2^{abc} \cdot \mathbf{i}_{abc} \quad (11)$$

$$= m_2 \cdot \mathbf{SIN}(\theta + \phi_m) \cdot \mathbf{i}_{abc}$$

with $\mathbf{d}_2^{abc} = [\, d_2^a \;\; d_2^b \;\; d_2^c \,]$.

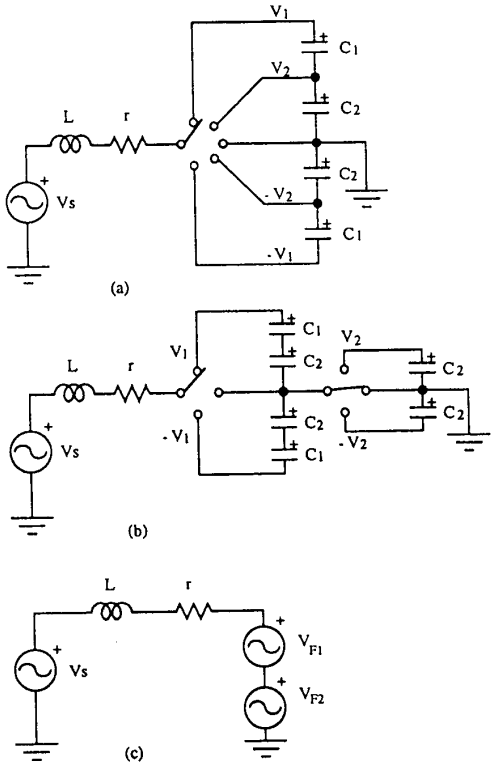


Fig. 6. Illustration of decomposition of a five-level inverter. (a) the original circuit, (b) two three-level inverters, (c) fundamental circuit modeling.

Taking the balanced switching operation into account,

$$i_4 = -i_2, \quad i_5 = -i_1 \tag{12}$$

Thus, i_3 becomes zero for the fundamental component. Using Eqs. (4), (5), (6), (8) and (11), we can draw out the fundamental equivalent circuit extracted from the original switching circuit as shown in Fig. 7. The resultant fundamental circuit model is no longer time varying and attributes linear as long as the control variables of the inverter do not change. Moreover, it is found that the five-level inverter can be modeled as a set of voltage controlled voltage sources and current controlled current sources on the fundamental frequency domain.

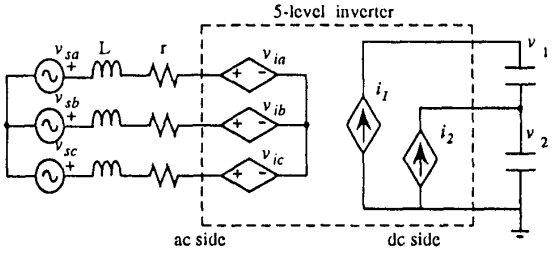


Fig. 7. Extraxted fundamental circuit model for the SVC system.

IV. STEADY STATE OPERATION

In steady state operation, referring to Fig. 7, the DC side voltages v_1 and v_2 remain constant and the DC side currents i_1 and i_2 become zero. On the other hand, the AC side of the SVC system can be reduced to single phase equivalent circuit with the per-phase phasor diagrams as shown in Fig. 8. Assuming no system losses, the voltages V_S and V_I are controlled to be in phase. A small amount of real power, hower, is needed to cover the losses and r stands for such a loss term. The amplitude of output phase voltage V_I can be controlled by adjusting phase angle ϕ_m whereby the corresponding DC voltages could be build up. In such a case, the phase angle ϕ_m determines the operating point for the SVC system. Neglecting the resistance r, the per-phase active and reactive powers from the inverter to the ac mains is expressed by

$$P = \frac{V_S V_I}{X_L} \sin\phi_m \tag{13}$$

$$Q = \frac{V_S \cdot (V_I \cos\phi_m - V_S)}{X_L} \tag{14}$$

respectively, with $V_S = V_{sa}/\sqrt{3}$, $V_I = V_{ia}/\sqrt{3}$. It should be noted that the SVC could be open loop controlled while injecting the active and reactive powers into the ac mains as long as the resistance r is not equal to zero, as found in [7].

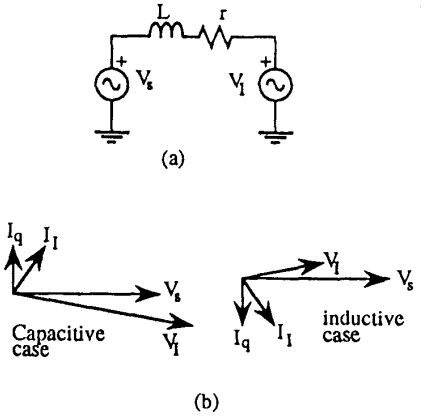


Fig. 8. (a) Simplified model of the ac side under steady state, (b) phasor diagrams.

V. DC CAPACITOR VOLTAGE BALANCING

The multilevel structure of the inverter inherently requires the DC side voltages which is equivalued and series connected. In such a case, the distinct structure of the inverter make it possible to reduce the active device stress and to fully utilize the semiconductor devices. In addition, the programmed multilevel PWM strategy is based on the equivalued DC side voltage. As a result, the DC side voltage balancing is of basic importance. Referring to the model in Fig. 7, the DC side capacitor voltages v_{C1} and v_{C2} are controlled by the dependent current sources i_1 and i_2. From Eq. (8), (11), it is found that i_1 and i_2 have some proportional relation as follows

$$i_1 = \frac{m_1}{m_2} i_2 \tag{15}$$

Note that Eq. (15) holds at every instances related to not only steady state but also transient state. Therefore, the amount of charges flowing into each capacitors during any transient state, and thus the variation of stored charges have the following relation

$$\Delta Q_{C1} = \frac{m_1}{m_1 + m_2} \Delta Q_{C2} \tag{16}$$

Hence, in order for the voltage variations to be the same, that is $v_{C1} = v_{C2}$ at each time, the relation below should be kept.

$$\frac{C_1}{C_2} = \frac{m_1}{m_1 + m_2} \tag{17}$$

Eq. (17) shows that two three-level modulation indexes m_1 and m_2 associated with a five-level modulation process should be determined under some constraint to preserve the DC capacitor voltage balancing.

VI. THE FIVE-LEVEL PWM

As before mentioned, the control variables of the inverter becomes m_1, m_2 and ϕ_m, where m_1 and m_2 are associated with three-level modulation process acting on the DC side voltages v_1 and v_2 respectively. Then, the resultant five-level modulation index M_i is represented by

$$M_i = \frac{\textit{amplitude of the output phase voltage}}{\textit{summation of DC side capacitor voltages } v_{C1} \text{ and } v_{C2}} = \frac{2m_1 v_1 + 2m_2 v_2}{v_1} \tag{18}$$

If v_{C1} and v_{C2} is controlled so as to be the same,

$$M_i = 2m_1 + m_2 \tag{19}$$

From Eq. (17), (19),

$$m_1 = M_i \cdot \frac{k_c}{1 + k_c} = M_i \cdot \hat{m_1} \tag{20}$$

$$m_2 = M_i \cdot \frac{1 - k_c}{1 + k_c} = M_i \cdot \hat{m_2} \tag{21}$$

where $k_c = C_1/C_2$, $\hat{m_1} = k_c/(1+k_c)$ and $\hat{m_2} = (1-k_c)/(1+k_c)$.

Eq. (20), (21), shows that, in order for the DC side voltage to be balanced, m_1 and m_2 should be determined depending on both the capacitance ratio k_c and five-level modulation index M_i. Also m_1 and m_2 are scaled by M_i with respect to their specific values $\hat{m_1}$ and $\hat{m_2}$. For given capacitance ratio k_c, such $\hat{m_1}$ and $\hat{m_2}$ are depicted in Fig. 9.

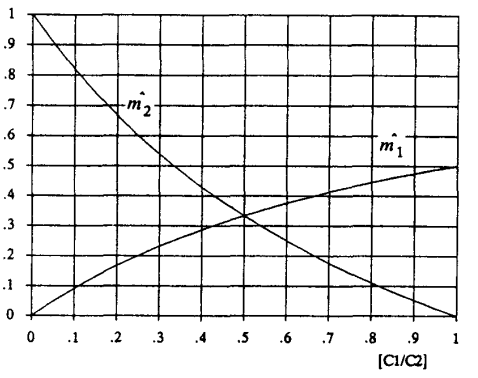


Fig. 9. variations of $\hat{m_1}$ and $\hat{m_2}$ versus capacitance ratio k_c.

As a design example, a possible switching pattern related to five-level PWM is shown in Fig. 10 where the angles α_1 through α_6 in a quarter cycle will be found from appropriate criteria. A quarter-wave symmetry in the waveform is assumed. In this paper, selective harmonic elimination for the output phase voltage of the inverter is carryed out because owing to multilevel approach considerable harmonic suppression seems to be achieved. As shown in Fig. 10, a quarter cycle of the five-level PWM may be split into two three-level ones according to the voltage level modulated. Each of them have their fundamental components V_{F1} and V_{F2} with modulation indexes M_1 and M_2, respectively. Therefore, tacking into account the DC voltage balancing condition,

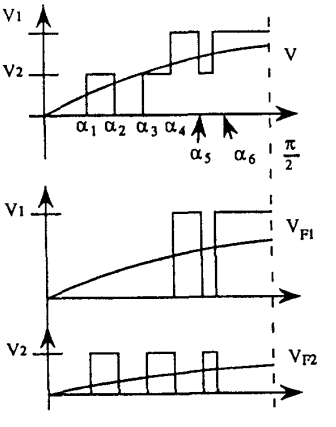


Fig. 10. A possible switching pattern for the inverter.

$$\frac{V_{F1}}{v_1} = \frac{4}{\pi}[\cos\alpha_4 - \cos\alpha_5 + \cos\alpha_6] = 2m_1 \quad (22)$$

$$\frac{V_{F2}}{v_2} = \frac{4}{\pi}[\cos\alpha_1 - \cos\alpha_2 + \cos\alpha_3 - \cos\alpha_4 + \cos\alpha_5 - \cos\alpha_6] = 2m_2 \quad (23)$$

The Fourier coefficients of the switched output phase voltage v_o (see Fig. 10) are given by

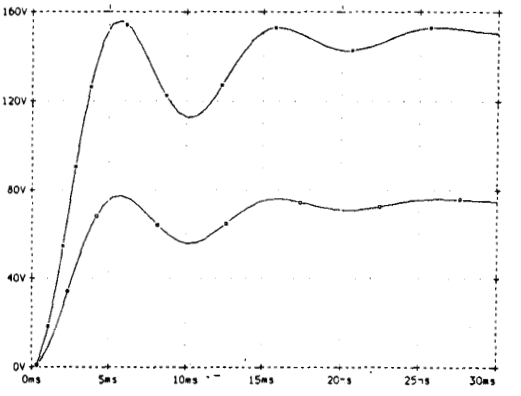
$$C_n = \frac{4v_2}{n\pi}[\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4) - \cos(n\alpha_5) + \cos(n\alpha_6)] \quad (24)$$

Six equations are needed to solve the above transcendental equations. Thus, from Eqs. (22), (23), it can be seen that four harmonics can be eliminated and 5, 7, 11, 13th harmonics will be vanished. If given C_1/C_2 = 1/3 and modulation index M_i = 0.8, then m_1 = 0.25, m_2 = 0.5, as seen in Fig. 9. Thus, $m_1 = M_i \cdot m_1 = 0.2$, $m_2 = M_i \cdot m_2 = 0.4$. With numerical computation, all the α's in radian can be obtained as follows: α_1 = 0.1084, α_2 = 0.3857, α_3 = 0.5445, α_4 = 0.7954, α_5 = 0.9995, α_6 = 1.4207.

VII. SIMULATED RESULTS

To confirm the validity of the fundamental circuit modeling of the SVC system with a five-level inverter, the system was simulated using commercial simulation packages such as PC-SIMNON for the switched circuit and PSPICE for the modeled circuit. In the simulation, the circuit parameters and controlling conditions are as follows: V_s=100V, f=60Hz, r=1Ω, L=5mH, C_1=500μF, C_2=1500μF, M_i=0.8.

In open loop test, attention is especially made on the DC side voltage balancing and thus, given ϕ_m, whether the DC side capacitor voltages are equivalued or not. Fig.11 shows the variation of v_1 and v_2 starting from zero initial conditions with ϕ_m=5°, and thus the open-loop controlled inverter seems to inject the capacitive reactive power into the ac mains. From Fig.11, it can be seen that, at each time, $v_1 = v_2$ and a DC side voltage of the system is stable, i.e. it dose converge to some value. Also, from Fig.11 it is found that the modeling of the system is valid. Fig. 12 shows the dymamic response for step change of load from capacitive to inductive one. In such case, the DC side voltages increase at the same rate and during the transient time, some active power flows into the inverter as shown in Fig. 12(d).



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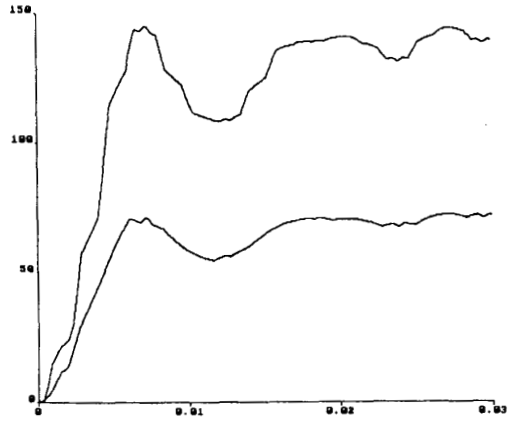
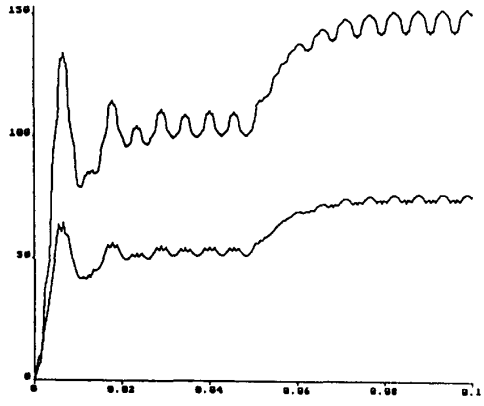


(b)

Fig. 11. Variations of DC side voltages v_1 and v_2 (ϕ_m=5°), (a) simulation with the fundamental circuit, (b) simulation with the switched circuit.

VIII. CONCLUSION

In this paper, a static Var compensator system using the multilevel inverter is suggested for high power high voltage application. The multilevel inverter has many advantages over the other inverter as a high power source such that high utilization of the switching devices, lower switching frequency at each semiconductor switches and multilevel output. To do so, the DC side capacitor voltage balancing is basically required and it is found that, depending on the DC side capacitances and the modulation index, such a condition can be determined. Also, this paper modeled the SVC system in the fundmental frequency domain and simulation result has shown the validaty of the model.



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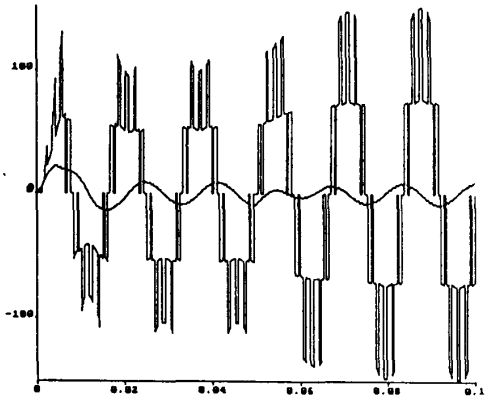

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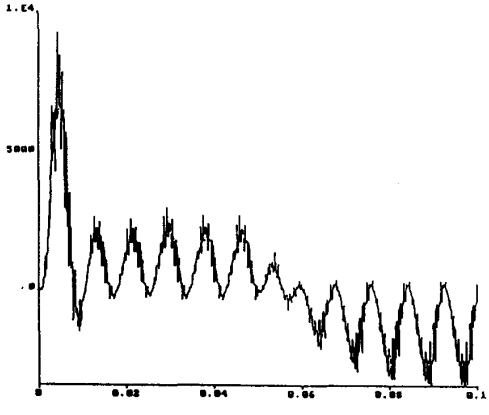

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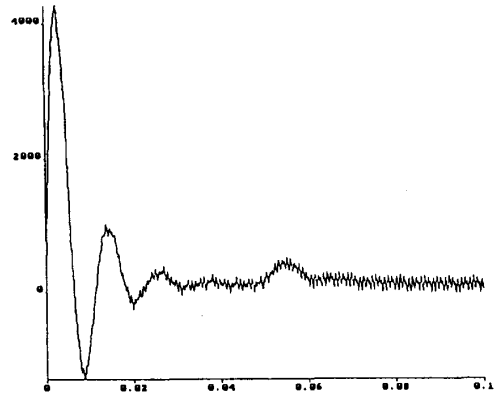

(d)

Fig. 12. Response to ϕ_m change from negative to positive, (a) DC side voltages v_1 and v_2, (b) inverter output phase voltage v_{ia} and line current flowing into the inverter i_a, (c) reactive power flowing into the inverter, (d) active power flowing into the inverter.

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