A 2 W CMOS Hybrid Switching Amplitude Modulator for EDGE Polar Transmitters

Tae-Woo Kwak, *Student Member, IEEE*, Min-Chul Lee, *Student Member, IEEE*, and Gyu-Hyeong Cho, *Member, IEEE*

***Abstract*—This paper presents a hybrid switching amplitude modulator for class-E2 EDGE polar transmitters. To achieve both high efficiency and high speed, it consists of a wideband buffered linear amplifier as a voltage source and a PWM switching amplifier with a 2 MHz switching frequency as a dependent current source. The linear amplifier with a novel class-AB topology has a high current-driving capability of approximately 300 mA with a bandwidth wider than 10 MHz. It can also operate on four quadrants with very low output impedance of about 200 mΩ at the switching frequency attenuating the output ripple voltage to less than 12 mV_{pp}. A feedforward path, a PWM control, and a third-order ripple filter are used to reduce the current burden of the linear amplifier. The output voltage of the hybrid modulator ranges from 0.4 to 3 V for a 3.5 V supply. It can drive an RF power amplifier with an equivalent impedance of 4 Ω up to a maximum output power of 2.25 W with a maximum efficiency of 88.3%. The chip has been fabricated in a 0.35 μm CMOS process and occupies an area of 4.7 mm^2.**

***Index Terms*—Buffer, class AB, dc–dc converter, EDGE, low dropout (LDO), low output impedance, operational amplifier, polar transmitter, power amplifier (PA), pulsewidth modulation (PWM), switching amplifier.**

I. Introduction

EVEN THOUGH amplitude variations of a phase-modulated carrier require inefficient linear RF power amplifiers, recent wireless systems tend to use amplitude modulation as well as phase modulation to achieve a high data rate. Polar transmitters as shown in Fig. 1 are known as good candidates for such high-data-rate systems because they can obtain high efficiency by using efficient switched-mode RF power amplifiers. However, when a complex signal is being split into its amplitude and phase components, the bandwidth of each component becomes wider than that of the original signal [1], [2]. This is why wideband low-dropout (LDO) linear amplifiers are still used in the amplitude path of most polar transmitters in spite of their low efficiencies. Recently, many efforts have been made to replace LDO amplifiers with switching ones to obtain better efficiency. Nevertheless, a switching amplifier has difficulty in efficiently following a high-frequency amplitude signal because a high switching frequency is required, and switching loss increases with switching frequency. Moreover, it has been implemented with many external components or expensive high-speed processes such as GaAs or SiGe. Although a CMOS amplitude modulator based on the concept of interleaving delta modulation has been suggested in [3], it still consumes considerable power and requires many external components—especially binary-weighted inductors. However, our proposed CMOS hybrid switching amplifier achieves both high speed and high efficiency through the combination of a wideband linear amplifier with a very efficient switching amplifier.

The organization of this paper is as follows. In Section II, we review the concept of the hybrid switching amplifier and present the auxiliary circuits, such as a feedforward path and a third-order ripple filter. In Section III, we present the proposed low-output-impedance buffer amplifier. In Section IV, we discuss the experimental results. Finally, in Section V, we present our conclusions.

Manuscript received May 1, 2007; revised August 15, 2007. This work was supported by the University IT Research Center (ITRC) Program of the Government of Korea.

The authors are with the Division of Electrical Engineering, School of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, 305-701 Daejeon, Korea (e-mail: twkwak@gmail.com).

Digital Object Identifier 10.1109/JSSC.2007.908769

II. Hybrid Switching Amplifier

A. Concept of a Conventional Hybrid Switching Amplifier

As shown in Fig. 2(a), the hybrid switching amplifier has a master–slave structure consisting of a wideband linear amplifier as a voltage source and a switching amplifier as a current-controlled current source. The wideband linear amplifier accurately controls the output voltage with good linearity, and the switching amplifier efficiently supplies most of the output current by sensing and amplifying the output current of the former.

Assuming that the current loop $\beta(\equiv i_d/i_a)$ has a large loop gain and a wide bandwidth, the linear amplifier only delivers the switching ripple current of the switching amplifier because the switching amplifier supplies most of the output current through the relation of $i_o = i_a + i_d = (1+\beta)\cdot i_a$. In reality, however, as shown in Fig. 2(b), the output current of the switching amplifier (i_d) is slower and less than the output current (i_o) because of the finite loop gain β. Thus, the linear amplifier must provide some amount of signal current in addition to the ripple current to compensate for the distortion that results from the phase lag of the switching stage in the high-frequency region. With the magnitude of loop gain $|\beta|$, the phase of loop gain θ, and the output current i_o at a specific frequency, the required output current of the linear amplifier i_a and the phase delay of the switching stage α are given by

$$|\beta| = \frac{\sin(\theta-\alpha)}{\sin\alpha}$$
$$i_a = i_o \cdot \frac{\sin\alpha}{\sin\theta}. \quad (1)$$

Although this hybrid switching concept has been suggested for audio [4], [5] and envelope elimination and restoration

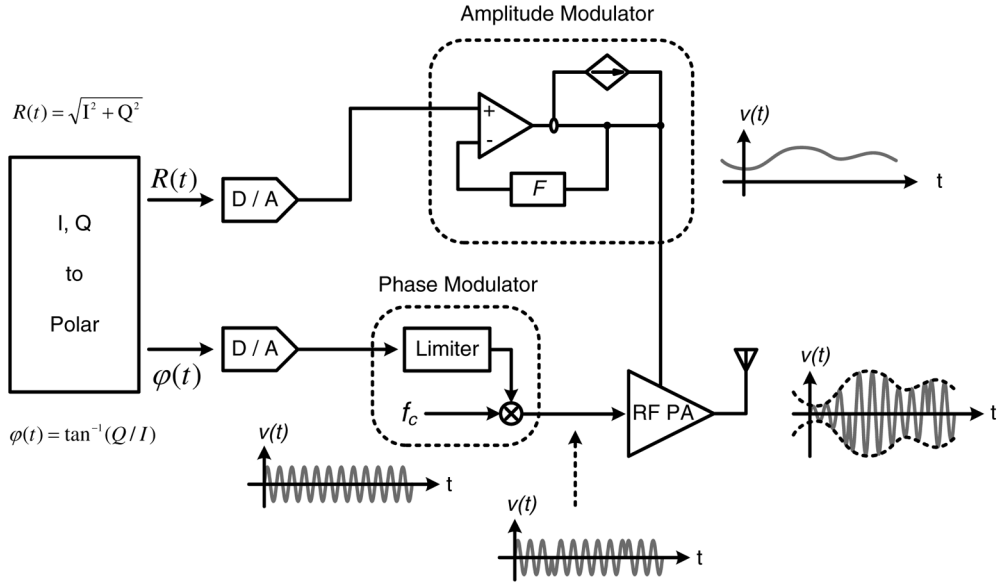


Fig. 1. Block diagram of a polar transmitter.

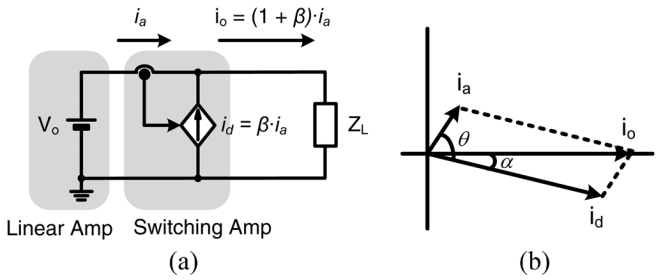


Fig. 2. (a) Conceptual diagram of the hybrid switching amplifier. (b) Phase diagram of each current.

(EER) applications [6], it has not been used for polar transmitters in CMOS process because of the difficulty of designing a linear amplifier with a wide bandwidth, a low output impedance, and a high current-driving capability. However, if the switching stage with a wide bandwidth and a low ripple current is used for the hybrid switching amplifier, such burdens of the linear amplifier can be reduced. By the way, a bandwidth and a ripple current are influenced by the control method. Compared with pulsewidth modulation (PWM) control, a hysteretic control of the switching amplifier relatively has a narrow bandwidth and a large constant ripple current because the switching frequency varies according to the output voltage and the bandwidth is limited by the minimum switching frequency. Therefore, the conventional hybrid switching amplifier based on the hysteretic control has a relatively lower bandwidth and a larger ripple current. To extend the narrow bandwidth wider, the linear amplifier must have a high current-driving capability according to (1) to provide more signal current for making up for the distortion from the switching stage. In case of a large ripple current, in particular, the linear amplifier must have a lower output impedance at the switching frequency to reduce the output ripple voltage because the multiplication of the output impedance of the linear amplifier and the ripple current makes the output ripple voltage.

B. Proposed Hybrid Switching Amplifier

As shown in Fig. 3(a), the PWM control is used for the switching stage to mitigate the difficulties in the design of the linear amplifier. Hence, the switching frequency f_s is fixed, which makes the unity-gain frequency constant as well. In addition, the peak-to-peak ripple current of the PWM-based hybrid switching amplifier is less than that of the hysteresis-based one [5] with the constant ripple current on the assumption that the switching frequency of the former is equal to the maximum switching frequency of the latter. This is because the relation between the switching frequency and the peak-to-peak ripple current Δi_r is expressed as follows for both cases:

$$f_s \cdot \Delta i_r = (V_{\rm dd}/L) \cdot D \cdot (1-D) \tag{2}$$

where D is the duty ratio, $\mathrm{V_{dd}}$ is the supply voltage, and L is the inductance.

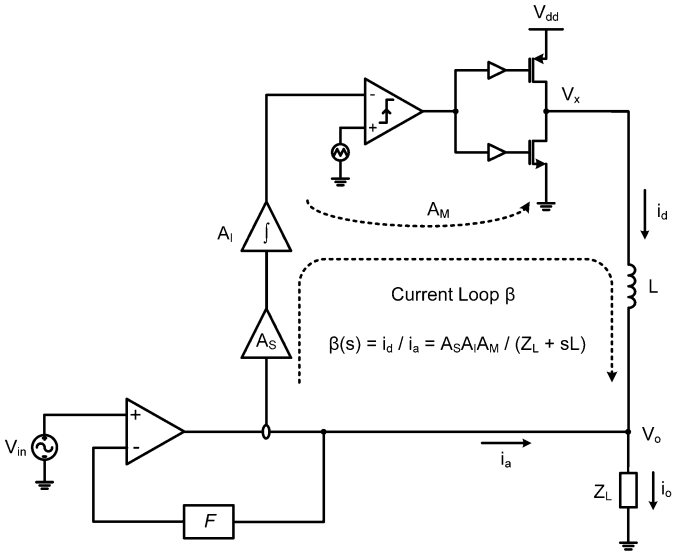
However, when we use the PWM control, we must consider the loop stability. From Fig. 3(a), the current loop gain β can be found by

$$\beta(s) = A_s A_I A_M/(Z_L + sL) \tag{3}$$

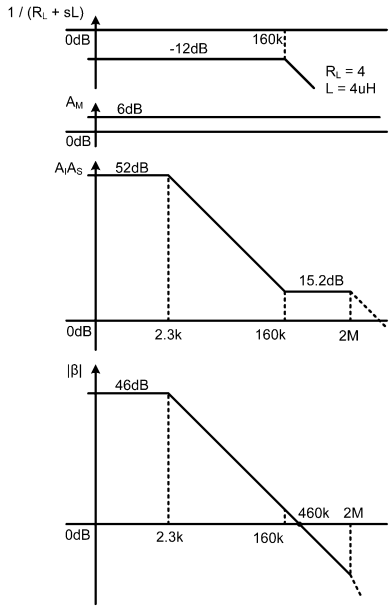
where A_S, A_I, and A_M are the current sense gain, integrator gain, and modulation gain, respectively, and $(Z_L + sL)$ is the impedance from a switching node V_x. The modulation gain A_M is the ratio of $V_{\rm dd}$ to a peak-to-peak magnitude of a triangular wave. For loop compensation, as shown in Fig. 3(b), one zero at about 160 kHz is inserted into the integrator since two poles result from the integrator and the inductor in the current loop.

C. Third-Order Ripple Filter and Current Feedback

Although the linear amplifier has low output impedance, the switching ripple current should be reduced to decrease both the output ripple voltage and the power consumption of the linear amplifier. For this purpose, as shown in Fig. 4, a third-order filter with L_1, L_2, and C_F is used in the current loop.



(a)



(b)

Fig. 3. (a) Simplified block diagram of the hybrid switching amplifier. (b) Bode plots for the current loop design.

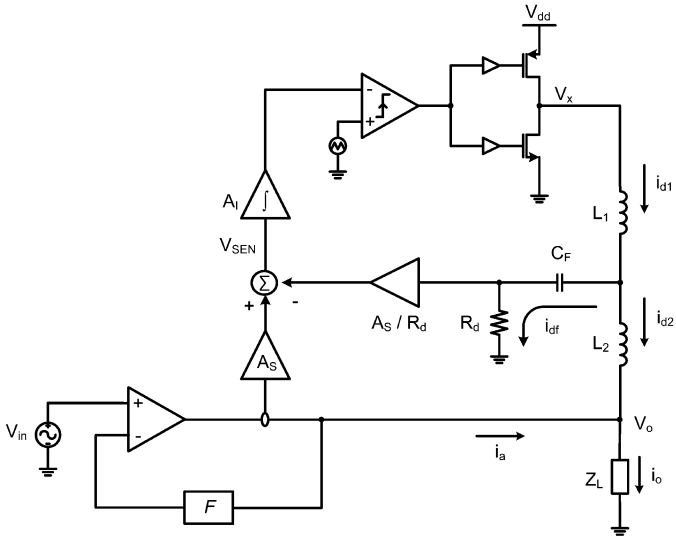


Fig. 4. Hybrid switching amplifier with the third-order ripple filter and the current feedback.

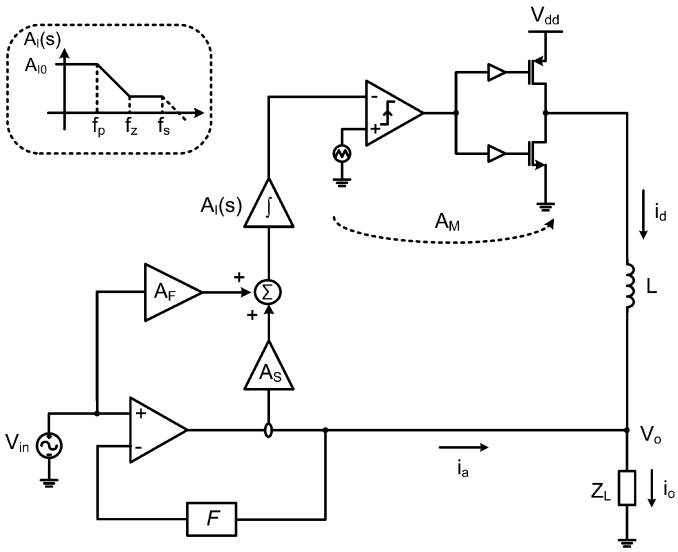


Fig. 5. Hybrid switching amplifier with the feedforward path.

In spite of the desirability of lowering the resonant frequency for greater reduction of the ripple current, two additional poles should have little impact on the current loop. Accordingly, the resonant frequency is chosen between the unity-gain frequency of the current loop and the switching frequency. Additionally, a damping resistor R_d is inserted, taking a quality factor into account, because an excessively small R_d can generate an unwanted resonance.

To stabilize the current loop in spite of the relatively small R_d, the current feedback suggested in [7] is introduced. The ripple information is used for the hysteretic control in the reference, whereas only a high-frequency signal current passing through the capacitor C_F is used for the PWM control with the same but negative gain as the current sense gain A_S, because the sensed ripple information is attenuated at the output of the integrator. The current loop therefore remains stable because the same voltage $V_{\rm SEN}$, as in the case of a single inductor, is recovered without losing the high-frequency current component.

D. Feedforward Path

As given in (1), the linear amplifier should provide some compensation current to prevent the output voltage from being distorted by the delay of the current loop at the high frequency. The higher the frequency, the more the compensation current flows. There are higher frequency components than the EDGE baseband signal of about 270 kHz in the amplitude path of the polar transmitter. Hence, an auxiliary circuit is necessary to alleviate the burden of the linear amplifier.

If we add a feedforward path, like the one shown in Fig. 5, the input signal can directly control the switching amplifier. Such a

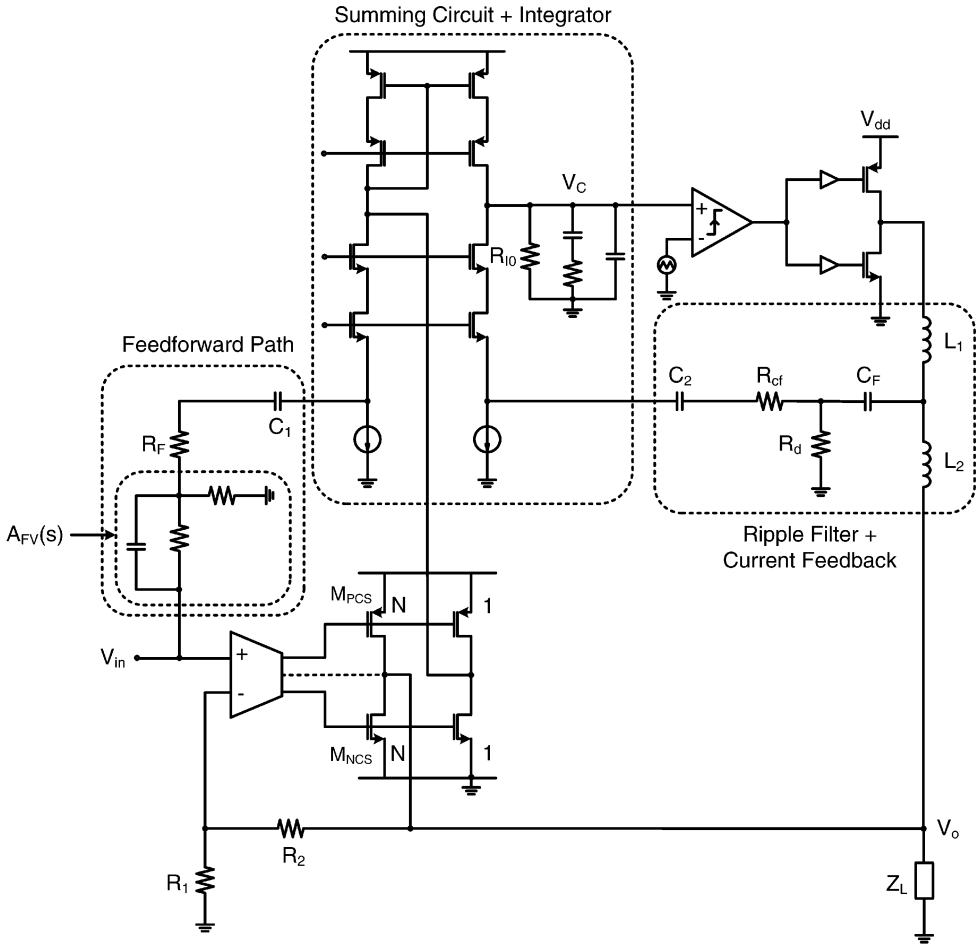


Fig. 6. Detailed block diagram of the hybrid switching amplifier.

path is faster than the feedback current path formed by sensing the output current of the linear amplifier. Although the feedforward signal can be injected after the integrator, it is added before the integrator in Fig. 5 considering the implementation of the summing circuit and integrator as will be explained in the next section. With this feedforward path, we can express the output current as follows:

$$i_o = \frac{A_{vf} \cdot v_{\text{in}}}{Z_L} = i_a + (A_S \cdot i_a + A_F \cdot v_{\text{in}}) \cdot A_I \cdot A_M \cdot \frac{1}{Z_L + sL} \tag{4}$$

where A_{vf} is the overall closed-loop gain of $1/F$. Since the output current of the linear amplifier i_a ideally has to be equal to zero, the gain of the feedforward path $A_F(s)$ is given as

$$\begin{aligned} A_F(s) &= \frac{A_{vf}}{A_M} \cdot \frac{1}{A_{I0}} \cdot \frac{1 + s/\omega_p}{1 + s/\omega_z} \cdot \frac{Z_L + sL}{Z_L} \\ &\approx \frac{A_{vf}}{A_M} \cdot \frac{1}{A_{I0}} \cdot \frac{1 + s/\omega_p}{1 + s/\omega_z} \end{aligned} \tag{5}$$

where the integrator gain $A_I(s)$ is $A_{I0} \cdot ((1+s/\omega_z)/(1+s/\omega_p))$. Notice that the gain of the feedforward path has the reciprocal characteristic of the integrator and the inductor to compensate for their delays.

E. Implementation of a Hybrid Switching Amplifier

Fig. 6 shows the detailed circuit of the hybrid switching amplifier. In CMOS design, although three voltage signals can be added and then integrated as shown in Figs. 4 and 5, the simultaneous summation and integration of the signals at the node V_c, after the conversion of the three voltage signals into current ones, is advantageous, that is, the sensed output current of the linear amplifier, the feedforward current, and the high-frequency current through the ripple filter are added together and integrated at the node with the inverted polarity of the last one.

In this case, the dc gain of the integrator A_{I0} is replaced by R_{I0} and the sensing ratio of the output current of the linear amplifier is 1 to N so that the current sense gain A_S is $1/N$. The feedforward path gain $A_F(s)$ given in (5) can be expressed as $A_{FV}(s)/R_F$ because the input voltage V_{in} is converted into the current by R_F after passing through the lead compensator $A_{FV}(s)$. As mentioned before, the zero and the pole of $A_{FV}(s)$ should be located at the pole and the zero of the integrator, respectively. If the transfer functions of the integrator and $A_{FV}(s)$ are given, the value of R_F can be found to set the dc gain of $A_F(s)$. The capacitor in the feedforward path C_1 is a coupling capacitor with a large capacitance.

After the high-frequency current that passes through the ripple filter is sensed as a voltage by the damping resistor R_d, the voltage is converted into the current by R_{cf}. Since the

high-frequency current should be transferred to the integrator with the same gain of $1/N$ as the output current of the linear amplifier, the value of $R_{\rm cf}$ is set equal to $N \cdot R_d$. The capacitor C_2 is also a coupling capacitor like C_1.

F. Design for the Class-E2 EDGE

The Class-E2 EDGE specifications require an average output power of 26 dBm and a peak-to-average power ratio of 3.2 dB. Accordingly, the amplitude modulator should be able to supply more than about 2.2 W, assuming that the RF power amplifier has a maximum efficiency of 40%. This means that the equivalent dc load resistance is approximately 4 Ω when the maximum output voltage of the amplitude modulator is 3 V at $V_{\rm dd} = 3.5$ V [2]. Hence, the hybrid switching amplifier is designed to drive a power amplifier with an equivalent impedance of 4 Ω while its output voltage varies from 0.4 to 3 V.

Despite the EDGE signal bandwidth of about 270 kHz, the amplitude modulator should have a bandwidth wider than 2 MHz to satisfy the error vector magnitude (EVM) and the spectral mask requirements because, as mentioned before, the amplitude component for the polar modulator becomes much wider than that of the original EDGE signal in the process of extracting it [1], [2]. Fortunately, however, the low-speed switching amplifier can efficiently supply most of the output current because most of the EDGE amplitude signal power is concentrated on the low-frequency band of less than 50 kHz, as shown in [1]. This is why the current loop β is designed to have a unity-gain frequency of about 460 kHz using a 2 MHz switching frequency with a 4 μH inductance, as shown in Fig. 3(b). As a result, a switching ripple current of about 110 $\rm mA_{pp}$ is generated without the use of the third-order ripple filter at a duty ratio of 0.5. However, it is reduced up to about 40 $\rm mA_{pp}$ with the third-order ripple filter and the current feedback. The values of the used components are as follows: $L_1 = 3\,\mu$H, $L_2 = 1\,\mu$H, $C_f = 100$ nF, $R_d = 2\,\Omega$, and $R_{\rm cf} = 390\,\Omega$.

On the other hand, the linear amplifier should have a bandwidth that is much wider than 2 MHz to compensate for the fast varying amplitude components that the switching amplifier cannot follow. The driving capability of the linear amplifier should also be more than at least 80 mA, including a switching ripple current and a high-frequency signal current, because, according to (1) and Fig. 3(b), the required output current of the linear amplifier is approximately 34 mA on the condition that the maximum output voltage at 50 kHz, $V_o = 1.25 \cdot \sin(2\pi \cdot 50\ k \cdot t) + 1.75\ V_{\rm dc}$, is applied to a 4 Ω load. To put it concretely, $|\beta| = 9.2$, $\theta = 90^\circ$ at 50 kHz from Fig. 3(b), and the output current from the switching stage is slower than the output current by $\alpha = 6.2^\circ$.

III. Linear Amplifier With a Novel Class-AB Buffer

A. Critical Design Parameters for the Linear Amplifier

If the amplitude modulator has an input signal of $a(t)$ and an output signal of $a'(t)$ with a closed-loop gain of 1, $a'(t)$ is expressed as the summation of $a(t)$ and the switching ripple voltage of $\alpha_R \cdot \cos(\omega_R t + \phi)$, where ω_R is the switching frequency. By assuming the phase-modulated signal of $\cos(\omega_c t + \theta(t))$ is applied at the input of the RF power amplifier, we can express the output of the power amplifier $s'_C(t)$ by the amplitude modulation of $a'(t)$ and $\cos(\omega_c t + \theta(t))$ as follows:

$$\begin{aligned} s'_C(t) =& a(t) \cdot \cos(\omega_c t + \theta(t)) + \alpha_R \cdot \cos(\omega_R t + \phi) \\ & \cdot \cos(\omega_c t + \theta(t)) \end{aligned} \tag{6}$$

The last term is caused by the output ripple voltage of the amplitude modulator, that is, the ripple voltage from the switching amplifier results in unwanted interference with the phase-modulated carrier at the offset frequency of ω_R away from the carrier frequency ω_c. Consequently, the fundamental component of the output ripple voltage should be a factor of approximately 700 less than the output voltage of the amplitude modulator to satisfy the spectral requirement of about -63 dBc for the maximum output power of 29.2 dBm at the switching frequency [13].

Because the switching ripple voltage at the output of the hybrid switching amplifier is generated by the multiplication of the ripple current and the output impedance of the linear amplifier, it is crucial to design the linear amplifier with low output impedance. In this design, when we consider the ripple current of about 40 $\rm mA_{pp}$, the output impedance should be less than about 200 mΩ at a switching frequency of 2 MHz.

In addition, the linear amplifier should be able to sink or source the ripple current at any level of the output voltage varying in the positive range during operation. In other words, the ripple current should be absorbed as well as supplied at a high output voltage and supplied as well as absorbed at a low output voltage. For a dual-supply voltage, this type of operation is called a four-quadrant operation with respect to the relation between the output current and the output voltage of the linear amplifier. We based our definition of the four-quadrant operation on the assumption that the output voltage at the center is half $V_{\rm dd}$ because of using a single supply voltage.

B. Conventional Class-AB Output Stages

A complementary common-source (CS) configuration [8], [9] used in most class-AB output stages has inherently high output impedance, and a source-follower (SF) configuration with a relatively low output impedance has a limited output swing that is unsuitable for low-voltage applications. With relatively small transconductance, these are why few output stages have been suggested for the low output impedance in the CMOS process while many class-AB output stages have been suggested for a low-voltage rail-to-rail operation, a wide bandwidth, and a high slew rate.

A local negative feedback using an operational transconductance amplifier (OTA) has often been applied to reduce the output impedance in a CS output stage [9]. The loop gain of the local feedback loop effectively reduces the output impedance together with that of a global feedback loop. The higher the loop gain of the OTA, the greater the decrease of the output impedance. However, the output impedance increases at a high frequency because the gains of both feedback loops decrease due to the bandwidth limitation. While increasing the transconductance of the output transistor in a CS output stage helps to reduce the output impedance with a Miller compensation capacitor at a high frequency, it requires much power consumption and large area to obtain the desired output impedance.

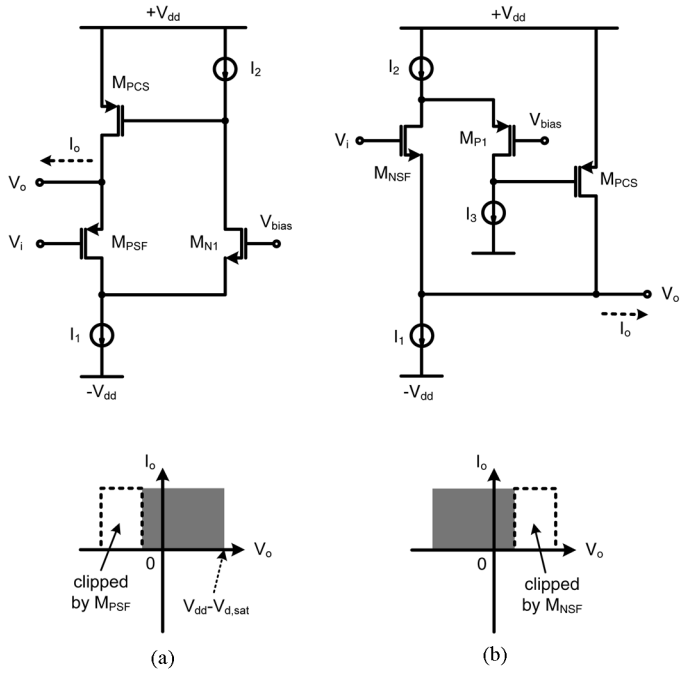


Fig. 7. Composite output stages advantageous to sourcing the output current.

The output stages, which are a combination of the CS and SF stages, have sometimes been suggested as a solution for both rail-to-rail operation and low output impedance [10], [11]. The output impedance of the composite output stage in [10] depends solely on the transconductance of the SF stage, so that it is not easy to implement the desired impedance through reasonable power consumption at a high frequency where the loop gain of the global feedback becomes small, that is, the enormous transconductance of the SF transistor required for the desired impedance brings about inefficiency in aspects of power and area, as mentioned above. On the other hand, the composite output stage in [11] can make the output impedance very low with relatively low power dissipation because of reducing the output impedance of the SF by a factor of the loop gain of the local feedback loop. The local loop operates as the same manner as the current loop β of the hybrid switching amplifier in that the SF and CS stages correspond to a voltage source and a dependent current source, respectively. Therefore, by widening the local loop, it is possible to implement the output stage with a wide bandwidth, a high current-driving capability, and a very low output impedance even at a high frequency. However, the composite output stage in [11] cannot complete the four-quadrant operation in itself without the help of a feedback class-AB biasing circuit [8], [12]. To facilitate the understanding, Fig. 7 shows two composite output stages advantageous to sourcing the output current. The composite output stage shown in Fig. 7(a) cannot obtain large negative output swing because of the source follower $M_{\rm PSF}$. As a result, there is a region unable to operate in the second quadrant. In contrast, the output stage in Fig. 7(b) has this type of region in the first quadrant because of the source follower $M_{\rm NSF}$. Because the complementary counterpart of Fig. 7(a) has a region unable to operate in the fourth quadrant, the composite push–pull output stage in [11] needs a feedback class-AB biasing circuit to achieve the four-quadrant operation required for the hybrid switching amplifier.

C. Proposed Class-AB Output Stage With Low Output Impedance and Four-Quadrant Operation

As shown in Fig. 8, a low output impedance and a four-quadrant operation can be achieved by combining the two structures shown in Fig. 7(a) and (b). Because the nMOS CS transistor $M_{\rm NCS}$ is added for the push-pull operation, four local loops can be found in the middle range of the output voltage. In addition, the switches $M_{\rm PR}$ and $M_{\rm NR}$ are inserted to prevent the output voltage from being clipped by the SF transistor, namely $M_{\rm NSF}$ or $M_{\rm PSF}$, near the positive or negative supply rail, respectively. In the concrete, during positive output swings, $M_{\rm NSF}$ is turned off by $M_{\rm PR}$, and the two loops ($M_{\rm PSF} - M_{N1} - M_{N3} - M_{\rm PCS}$ and $M_{\rm PSF} - M_{N1} - M_{N3} - M_{\rm NCS}$) source or sink the ripple current to eliminate the output ripple voltage. During negative output swings, $M_{\rm PSF}$ is turned off by $M_{\rm NR}$, and the two loops ($M_{\rm NSF} - M_{P1} - M_{P3} - M_{\rm PCS}$ and $M_{\rm NSF} - M_{P1} - M_{P3} - M_{\rm NCS}$) perform the same function.

This kind of push–pull output stage requires a bias control circuit that can reduce the distortion of the output transistors by guaranteeing that a certain minimum current flows. The composite output stage suggested in [11] can function in four quadrants solely with a feedback class-AB biasing circuit as mentioned before, whereas the proposed output stage can operate in four quadrants with any class-AB biasing circuit [8], [12], though, in our design, as shown in Fig. 9, a feedback class-AB biasing circuit is used for future low-voltage applications. The branch of the cascode transistors ($M_{P1} - M_{P3} - M_{N3} - M_{N1}$) in Fig. 8 is separated into two branches ($M_{P1} - M_{P3} - M_{N4} - M_{N2}$ and $M_{P2} - M_{P4} - M_{N3} - M_{N1}$) for biasing of the output transistors. In particular, the selected minimum current is inserted into the source node of the cascode transistor (M_{P3} and M_{N3}) and not into the gate node, as suggested elsewhere [8]. This helps increase the phase margin of the class-AB feedback loop by avoiding a nondominant pole at the gate of the cascode transistor.

The compensation capacitors and resistors should be determined in order to obtain as wide a bandwidth as possible and to stabilize each local loop under any output voltage and load conditions. Because the loop composed of $M_{\rm PSF}$ and $M_{\rm PCS}$ is the slowest at the maximum output voltage and the heaviest load, the bandwidth of the linear amplifier depends on this loop. In spite of the desirability of using large compensation capacitors to achieve a sufficient phase margin of each loop at the open load, the optimum values of these capacitors should be found to achieve a wide bandwidth. In other words, the compensation capacitor in a two-stage OTA is determined to locate the unity-gain frequency of the global feedback loop inside the -3 dB frequency of the buffer stage and the compensation capacitors, C_{C1} and C_{C2}, in the buffer stage are set to guarantee the stability of the local loops at the open load with the zero frequencies by R_{Z1} and R_{Z2} located near the unity-gain frequencies of the local loops. To get a unity-gain frequency of more than 10 MHz in this design, we assigned a capacitance of 710 fF for both C_{C1} and C_{C2} and 1.6 pF for the compensation capacitor of a two-stage OTA. The bias currents of the

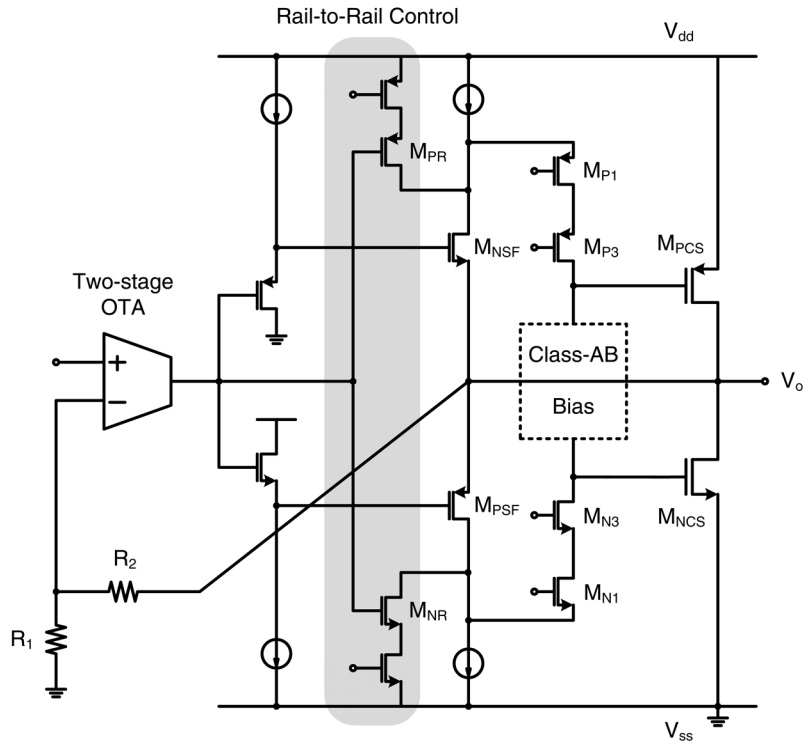


Fig. 8. Rail-to-rail four-quadrant output stage with low output impedance.

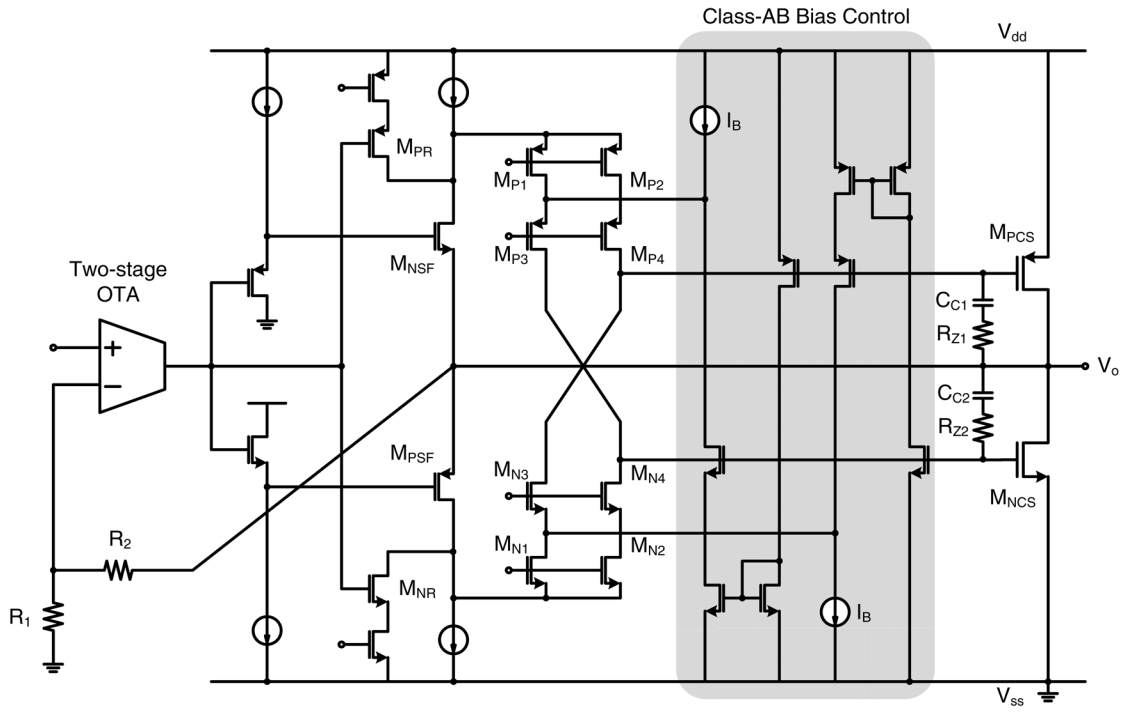


Fig. 9. Linear amplifier with a class-AB low-output-impedance buffer.

source followers are set to about 300 μA to prevent the nondominant pole at the output caused by the impedances of them from affecting the phase margin. The common-source transistors $M_{\rm PCS}$ and $M_{\rm NCS}$ have the aspect ratios of 1500μm/0.35μm and 600μm/0.35μm, respectively, and are biased at about 2 mA.

IV. Experimental Results

Fig. 10 shows a micrograph of the prototype fabricated in a 0.35-μm CMOS process with an area of 4.7 mm^2. The size of the power transistor is 72,000 μm for the pMOS and 20,160 μm

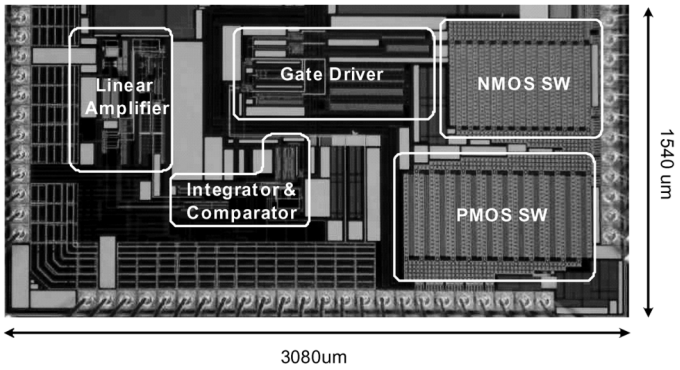


Fig. 10. Chip micrograph of the hybrid switching amplifier.

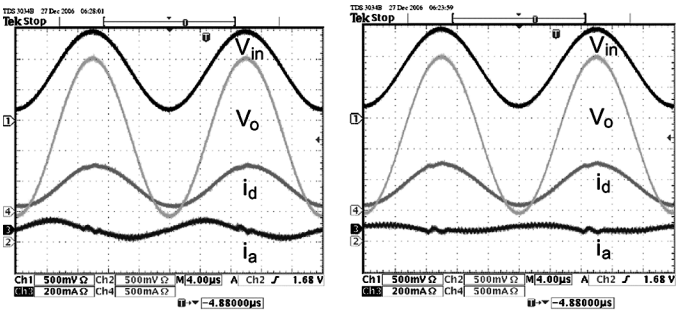


Fig. 11. Measured waveforms (a) without the feedforward path and (b) with the feedforward path ($\mathrm{Ch1}: V_{\mathrm{in}}$, $\mathrm{Ch2}: V_o$, $\mathrm{Ch3}: i_a$, $\mathrm{Ch4}: i_d$).

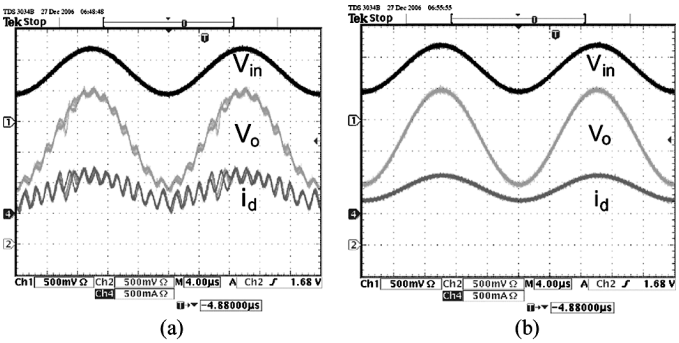


Fig. 12. Measured waveforms with the third-order ripple filter (a) without the current feedback and (b) with the current feedback ($\mathrm{Ch1}: V_{\mathrm{in}}$, $\mathrm{Ch2}: V_o$, $\mathrm{Ch4}: i_d$).

for the NMOS. The closed-loop gain of the hybrid switching amplifier is 2, and the feedback resistors R_1 and R_2 in Fig. 6 are integrated.

The chip is powered from a 3.5 V supply. To prevent the high-frequency switching noise caused by parasitic components at the switching stage from being coupled to the output, the supply voltage of the gate driver and the output switches was separated from that of the other circuits and the bare chip was directly bonded to the PCB.

Fig. 11 shows the effect of the feedforward path. Without the feedforward path, as shown in Fig. 11(a), the output current of the linear amplifier is approximately 120 $\mathrm{mA_{pp}}$. In contrast, as shown in Fig. 11(b), this value is reduced to about half when the feedforward path is used.

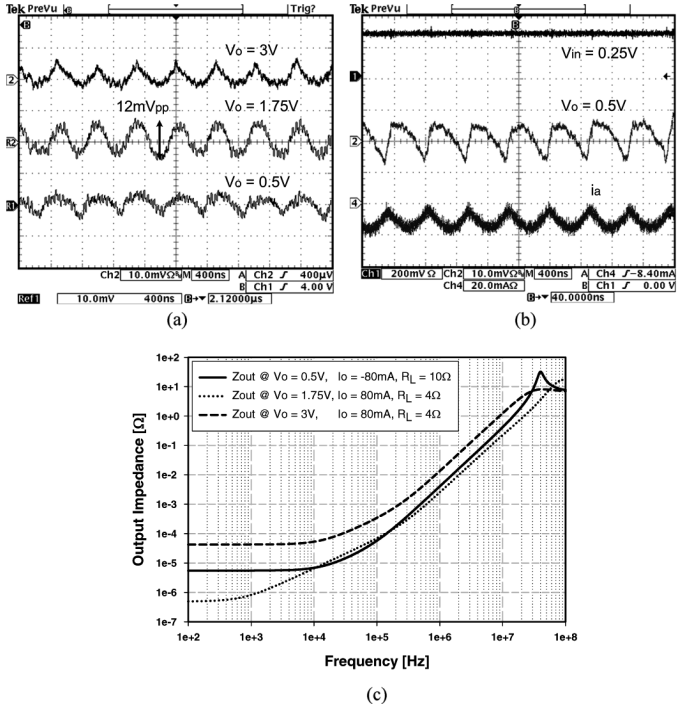


Fig. 13. (a) Measured ac-coupled output ripple voltages according to the output voltage. (b) Output current of the linear amplifier at $V_o = 0.5$ V. (c) Simulated frequency response of the output impedance of the linear amplifier.

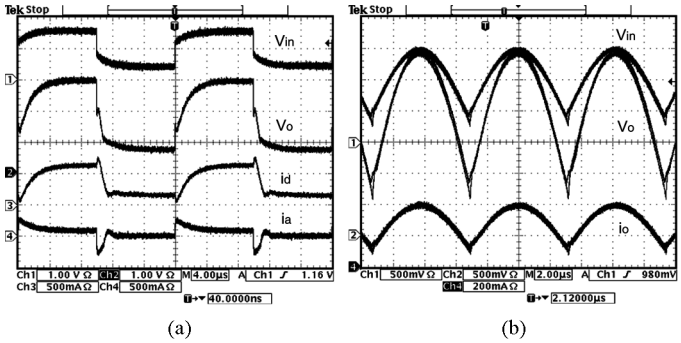


Fig. 14. Measured waveforms for (a) 50 kHz square-wave signal at 4 Ω load and (b) 160 kHz full-wave rectified signal at 8 Ω load.

Fig. 12 demonstrates how well the current feedback operates with the third-order ripple filter. Because the resonant frequency of 580 kHz with a Q-factor of 1.37 is approximately obtained from the components given in Section II, the unwanted oscillation of about 600 kHz occurs as shown in Fig. 12(a) when the current feedback is not used. However, there is no resonance after the current feedback is applied, as shown in Fig. 12(b).

Fig. 13(a) shows the output ripple voltage in relation to the output voltage. A maximum ripple voltage of about 12 $\mathrm{mV_{pp}}$ occurs in the middle of the output voltage because of the PWM control. As shown in Fig. 13(b), the output current of the linear amplifier was measured at $V_o = 0.5$ V to indirectly guess the output impedance of the linear amplifier. The output impedance of about 500 mΩ is obtained since the peak-to-peak ripple voltage and ripple current are approximately 8 $\mathrm{mV_{pp}}$ and 16 $\mathrm{mA_{pp}}$, respectively. The value of the peak-to-peak ripple voltage shown in Fig. 13(a) should be used because the parasitic

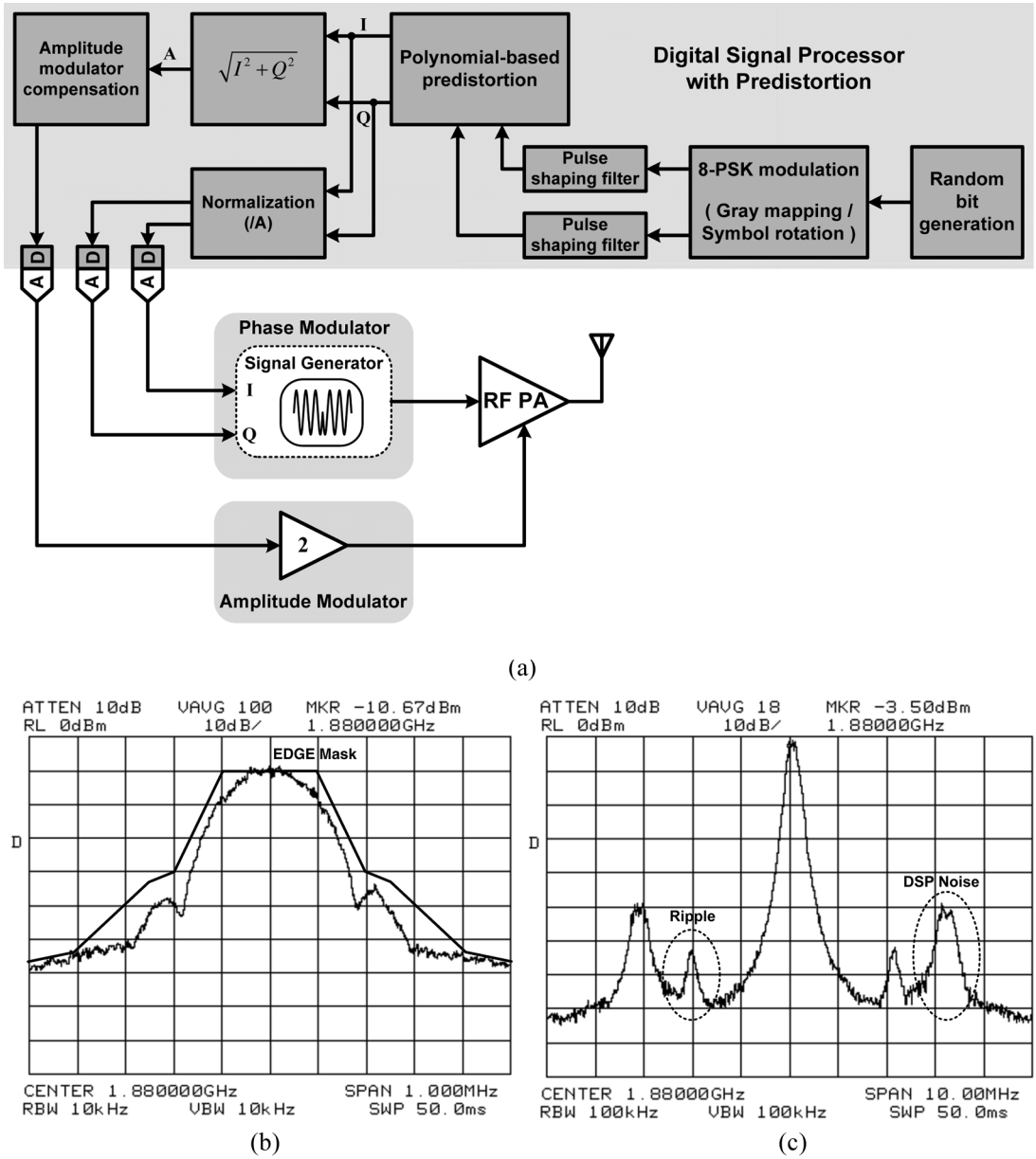


Fig. 15. (a) Block diagram of the measurement setup. Output spectrum at instantaneous output power ranging from 8.5 dBm to 28 dBm with (b) 1 MHz span and (c) 10 MHz span.

impedance added in the course of measuring the output current of the linear amplifier increased the output ripple voltage. Similarly, taking the negative feedback from the slightly wrong place resulted in the larger output impedance than the simulation result shown in Fig. 13(c), that is, the impedances of bond wire and PCB trace from the linear amplifier output to the output had dominant influence upon the output impedance because the feedback resistors R_1 and R_2 are integrated in the chip as mentioned before.

Fig. 14(a) shows the waveforms for a 50 kHz square-wave signal with a 4 Ω load. The linear amplifier has a current-driving capability of approximately 300 mA at the rising and falling edges, respectively. In addition, the hybrid switching amplifier has a rising time of less than 4 μs. Fig. 14(b) shows the input and output voltage waveforms for a 160 kHz full-wave rectified signal with an 8 Ω load. The waveforms have some distortions near the zero-crossing points because the rectified input signal is generated on the PCB using a commercial opamp with a narrow bandwidth. Nevertheless, the output follows the input very well.

Fig. 15 shows the spectral responses for the EDGE signal generated from a DSP. To demonstrate the performance of this amplitude modulator, we made a prototype of a polar transmitter by using a commercial RF power amplifier and a DSP for the function of predistortion, as shown in Fig. 15(a). In spite of a relatively high noise level of the baseband signal from the DSP, as shown in Fig. 15(b), the prototype satisfies the EDGE spectral requirement with negligible margin at the critical frequency of 400 kHz. As a result, it is demonstrated that the proposed hybrid switching amplifier can become a good candidate for class-E2 EDGE polar transmitters considering the increase of the output impedance and the high noise level of the baseband signal, even though there are little margins at 400 kHz and 2 MHz, as shown

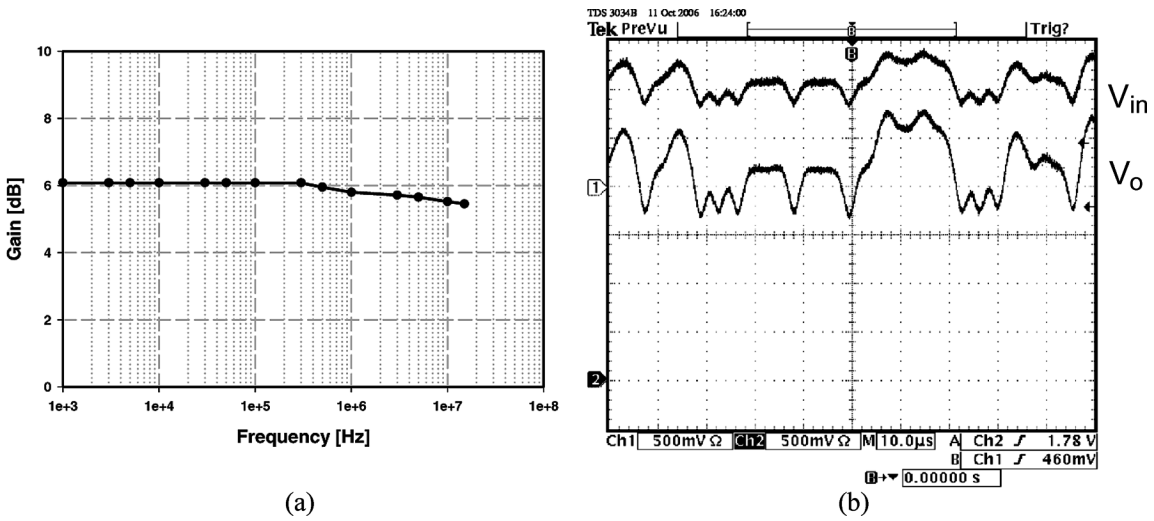


Fig. 16. (a) Measured small-signal bandwidth of the hybrid switching amplifier for a 39 Ω load at $V_{o,\mathrm{dc}} = 1.72$ V. (b) Response to the amplitude component of EDGE signal.

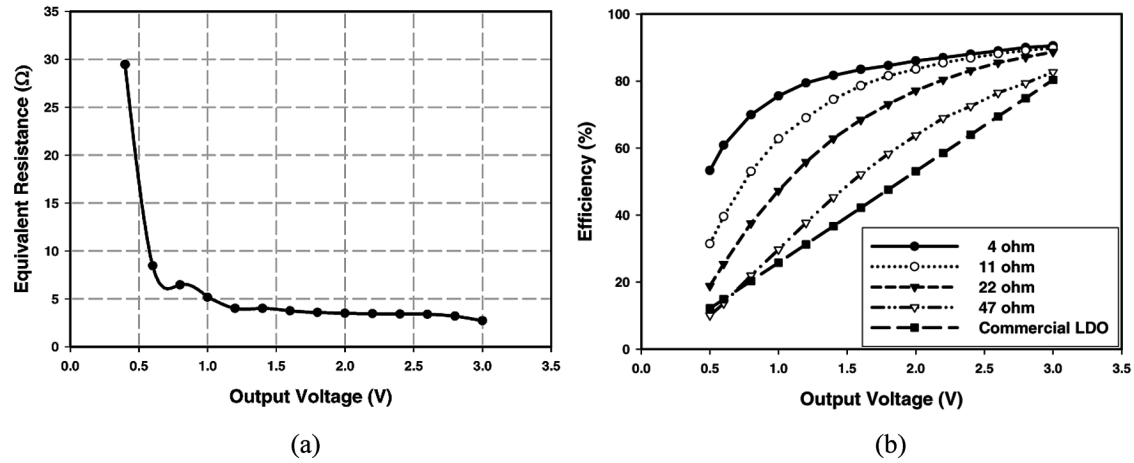


Fig. 17. (a) Measured equivalent resistance of a commercial RF power amplifier. (b) Measured efficiency of the hybrid switching amplifier at various loads.

in Fig. 15(b) and (c). The unwanted spur shown in Fig. 15(c) at about 3 MHz results from the clock frequency of the DAC on the DSP board, which is not related to the amplitude modulator.

Fig. 16(a) shows that the small-signal closed-loop bandwidth of the hybrid switching amplifier measured under 39 Ω load condition at the output dc voltage of 1.72 V is larger than about 10 MHz. Fig. 16(b) is the response of the amplitude modulator for the amplitude component of the EDGE signal generated from a DSP in the prototype of polar transmitter. The output waveform follows the input signal very faithfully.

Fig. 17(b) shows the efficiency of the hybrid switching amplifier in relation to the load condition. The amplifier can provide a maximum power of 2.25 W to a 4 Ω load with the maximum efficiency of 88.3%. Except for small currents, the efficiency of the hybrid switching amplifier is superior to that of a commercial LDO measured at a 4 Ω load. Actually, the inefficiency for the small currents shown in Fig. 17(b) is not serious, because the equivalent dc resistance of the commercial RF power amplifier as a load of the amplitude modulator ranges from 2.7 to 29.4 Ω, as shown in Fig. 17(a).

TABLE I
MEASURED PERFORMANCE PARAMETERS

Supply voltage	3.5 V
Output voltage range	0.4 V ~ 3 V
Maximum output power	2.25 W @ 4Ω
Switching frequency	2 MHz
Closed-loop bandwidth (small-signal)	> 10 MHz
Output ripple voltage	< 12 mV_{pp}
Current-driving capability of the linear amp	~ 300 mA
Typical power dissipation of the linear amp	20 mW @ idle condition
Maximum efficiency	88.3 % @ 4Ω

Table I summarizes the measured performance. The switching ripple current causes the linear amplifier to dissipate the power of about 20 mW even under a condition of no input.

V. Conclusion

We propose a CMOS hybrid switching amplitude modulator for class-E2 EDGE polar transmitters. The proposed modulator, which is based on a hybrid switching technique, can achieve both high efficiency and high speed. For better performance, we introduced a PWM control, a feedforward path, and a third-order ripple filter with current feedback into the switching stage. We also propose a novel class-AB buffer amplifier with the following characteristics: a wide bandwidth, a low output impedance, four-quadrant operation, and a high current-driving capability. In conclusion, the hybrid switching amplitude modulator satisfies the requirements of the output power, the EVM, and the spectral mask margin.

Acknowledgment

The authors would like to thank D.-H. Lee, W.-S. Nam, and J.-S. Paek for their assistance with the measurements.

References

[1] M. R. Elliott *et al.*, "A polar modulator transmitter for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2190–2199, Dec. 2004.

[2] P. Reynaert and M. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.

[3] P. J. Nagle *et al.*, "A wideband linear amplitude modulator for polar transmitters based on the concept of interleaving delta modulation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2002, pp. 234–488.

[4] N. S. Jung, J. H. Jeong, and G. H. Cho, "High efficiency and high fidelity analogue/digital switching mixed mode amplifier," *Electron. Lett.*, vol. 34, pp. 828–829, Apr. 1998.

[5] H. Ertl *et al.*, "Basic considerations and topologies of switched-mode assisted linear power amplifiers," *IEEE Trans. Ind. Electron.*, vol. 44, pp. 116–123, Feb. 1997.

[6] F. Wang *et al.*, "Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2005, pp. 645–648.

[7] N. I. Kim, S. H. Jung, J. Y. Ryoo, and G. H. Cho, "Ripple feedback filter suitable for analog/digital mixed-mode audio amplifier for improved efficiency and stability," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 2002, pp. 45–49.

[8] K.-J. de Langen and J. H. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1482–1496, Oct. 1998.

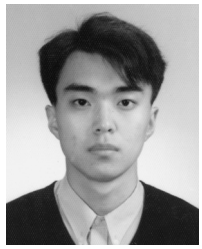
[9] K. E. Brehmer and J. B. Wieser, "Large swing CMOS power amplifier," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 12, pp. 624–629, Dec. 1983.

[10] J. N. Babanezhad, "A low-output-impedance fully differential op amp with large output swing and continuous-time common-mode feedback," *IEEE J. Solid-State Circuits*, vol. 26, no. 12, pp. 1825–1833, Dec. 1991.

[11] G. A. Rincon-Mora and R. Stair, "A low voltage, rail-to-rail, class AB CMOS amplifier with high drive and low output impedance characteristics," *IEEE Trans. Circuits Syst. II*, vol. 48, no. 8, pp. 753–761, Aug. 2001.

[12] J. Huijsing, *Operational Amplifiers—Theory and Design*, 1st ed. Boston, MA: Kluwer, 2001.

[13] *Digital cellular telecommunications system (Phase 2+); Radio transmission and reception*, ETSI TS 145 005. 3GPP TS 45.005, 2007.



Tae-Woo Kwak (S'04) received the B.S. degree from Kyungpook National University, Daegu, Korea, in 2000, and the M.S. degree from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 2002, both in electrical engineering. He is currently working toward the Ph.D. degree in electrical engineering at KAIST. His doctoral work concerns the switching amplitude modulator for polar transmitters.

His research interests are analog integrated circuits and smart power ICs such as power management ICs and audio power amplifiers.

Mr. Kwak was the corecipient of the Gold Prize in the Human-Tech Thesis Prize from Samsung Electronics and the Best Design Award of the Korean Conference on Semiconductors in 2006, respectively. He was also the recipient of the ISSCC 2007 Silkroad Award as well as the Best Design Award from Dongbu HiTek in 2007.

Min-Chul Lee (S'04) received the B.S. and M.S. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 1999 and 2001, respectively. He is currently working toward the Ph.D. degree in electrical engineering at KAIST.

His research interests include high performance dc–dc converter design and low-power analog integrated circuit design. In particular, he is currently involved with the design of the amplitude modulator for EDGE polar transmitters.

Gyu-Hyeong Cho (S'76–M'80) received the B.S. degree from Hanyang University, Seoul, Korea, in 1975, and the M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Seoul, in 1977 and 1981, respectively.

During 1982-1983, he was with Westinghouse R&D Center, and he joined the Department of Electrical Engineering at KAIST in 1984. He has been a full Professor since 1991 and was a Visiting Professor with the University of Wisconsin, Madison, in 1989. His research focused on the area of power electronics until the late 1990s, and he has been involved with soft switching converters, high-power and high-voltage inverters, and Static Var Compensators. Later, he shifted to another area of Analog Integrated Circuit Design. His recent research is focused on two areas: one is the combined area of analog integrated circuits and power electronics, including smart power ICs such as single-chip power management ICs and Class-D audio power amplifiers, and the other is display driver ICs for LED, OLED, and LCD flat-panel displays.