7.7 A Column Driver with Low-Power Area-Efficient Push-Pull Buffer Amplifiers for Active-Matrix LCDs

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In high-image-quality large-sized AMLCD applications, dot inversion for polarity reversal has been applied [1]. To reduce current consumption, vertical N-dot inversion data driving can be applied in large-sized AMLCD applications. In order to implement vertical N-dot inversion data driving, buffer amplifiers in a column driver should provide a push-pull function due to the long time constants of column lines in an AMLCD panel. As the display resolution increases, hundreds of buffer amplifiers should be integrated into one driver IC. Therefore, the layout area and current consumption of buffer amplifiers are important parameters for column drivers. For AMLCD driving applications, various buffer amplifier circuits have been proposed [2-5]. Existing buffer amplifiers, however, have large layout areas and high current consumption because they include numerous transistors and circuit branches. For a number of cases, even vertical N-dot inversion applications are not appropriate due to the lack of a push-pull function for all output channels [3]. In this paper, a column driver with 720 transient-operating push-pull buffer amplifiers is presented. It consumes low static current and occupies a smaller layout area because it minimizes the number of transistors and circuit branches used to implement the push-pull function.

Figure 7.7.1 shows the full function column driver with the 720 transient-operating push-pull buffer amplifiers. Each channel of the column driver can provide 512 distinct voltage levels between 0.1V and the nearest supply voltage (V_{DD} - 0.1V) by the synchronized operation of an input data selection pass-transistor logic block and an output switching block. For the polarity inversion operation, these voltage levels are divided into two groups. The first is for a negative gamma curve and is composed of 256 voltage levels between 0.1V and half of V_{DD}. The second is for a positive gamma curve composed of 256 voltage levels between half of V_{DD} and V_{DD} – 0.1V. The outputs of the chip are automatically assigned their column inversion mode, as the chip provides the outputs of A_H and A_L simultaneously. A_H and A_L must have a push-pull function in vertical N-dot inversion applications, as each channel must charge and discharge an AMLCD panel irrespective of the initial voltage of the column line.

Figure 7.7.2 shows a conceptual schematic of the two proposed complementary buffer amplifiers. The first is a push amplifier with a pull function (A_H) and the second is a pull amplifier with a push function (A_L). In large-area AMLCD applications, the reference voltage is nearly half of the supply voltage for polarity reversals. Rail-to-rail buffer amplifiers can be used in this application, but they lead to larger area and greater power consumption because the charging (discharging) parts of the amplifiers are of no use during the discharging (charging) operation. The buffer amplifiers used here minimize the number of circuit branches operating in steady-state, as one of the power and area-efficient buffer amplifier design approaches was to minimize the number of circuit branches. By combining AMPH (AMPL), CMPH (CMPL) and MH (ML) in the A_H (A_L) buffer amplifier (Fig. 7.7.2), the push-pull function is implemented. In this case, MH and ML are turned off in steady state by the bleeding currents I_{BH} and I_{BL}, respectively. MH (ML) pulls (pushes) the current from (to) the load only during transient operation according to the voltage difference between the input (V_{IN+}) and the output (V_{OH} or V_{OL}) terminals. Figure 7.7.3 shows schematics of the buffer amplifiers. The intended 7% W/L mismatch between M10H (M10L) and M11H (M11L) produces the bleeding currents I_{BH} and I_{BL} without the need for additional transistors.

Figure 7.7.4 shows the output voltage waveforms of the 2 fixed channels for a vertical 2-dot inversion operation. The driving voltage waveforms for each channel define 2 periods: direct-drive and shift-drive. In the direct-drive period, the odd-numbered outputs are from the A_H factors and the even-numbered outputs are from A_L factors, while in the shift-drive period, the odd-numbered outputs are from the A_L factors and the even-numbered outputs are from the A_H factors. In addition, each drive period is composed of a first drive period and a second drive period. All of the column lines of the panel should be forced to half the level of the supply voltage during the equalization period. However, the circuits could not set all column line voltages to a fixed voltage due to the long time constants of the column lines. According to the voltage difference between the first and second drive periods, each channel requires charging or discharging and should have a push or pull function peformed. This situation occurs when vertical N-dot inversion is used in the application. In region A1 (B1), the output of channel 1 (2) is from an A_H (A_L) buffer, and this A_H (A_L) buffer has to discharge (charge) the panel by performing a transient pull (push) operation. In region A2 (B2), the output of channel 1 (2) is from an A_L (A_H) buffer, and this A_L (A_H) buffer has to charge (discharge) the panel by performing a transient push (pull) operation.

Output DC offsets should be controlled within ±25mV because DC offsets generate various display quality problems as a result of transmittance errors in an AMLCDs [4]. To compensate for the DC offset of each amplifier, an offset averaging method is applied [4]. The offset averaging circuit can be implemented by a switching operation for all differential input stages, as explained in [6]. Figure 7.7.5 shows the relative output DC offset distributions for 360 A_H and 360 A_L amplifiers in the column driver for typical input data with or without a DC offset averaging method.

Figure 7.7.6 summarizes the performance of the column driver. The 3.8μA of static current is equivalent to a sub-μA static current for a design with a low-voltage process, as the μC_{OX} values of low-voltage processes are generally 3 to 4 times larger than those of high-voltage processes.

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References:
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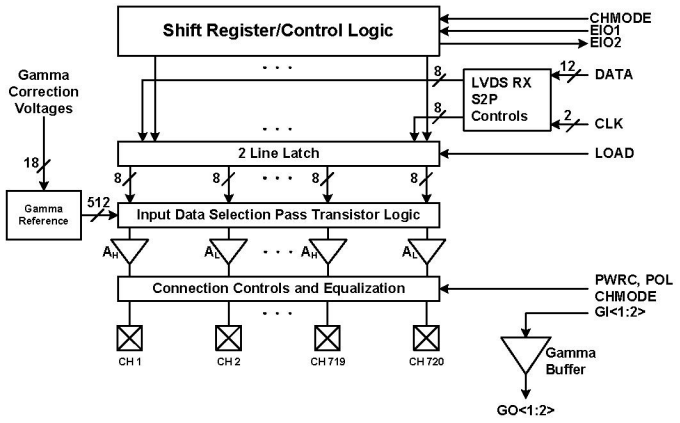

Figure 7.7.1: Column driver architecture.

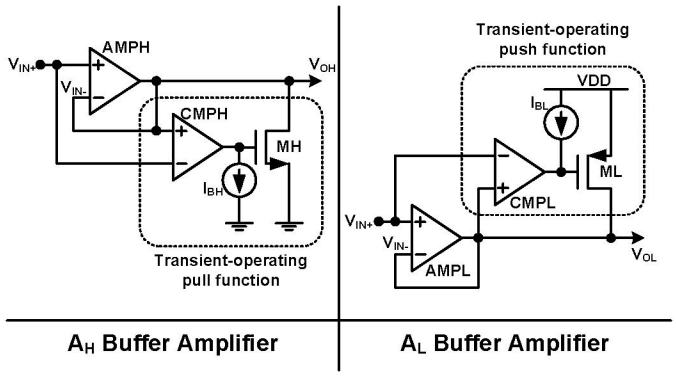

Figure 7.7.2: Conceptual schematic of the transient-operating push-pull amplifiers.

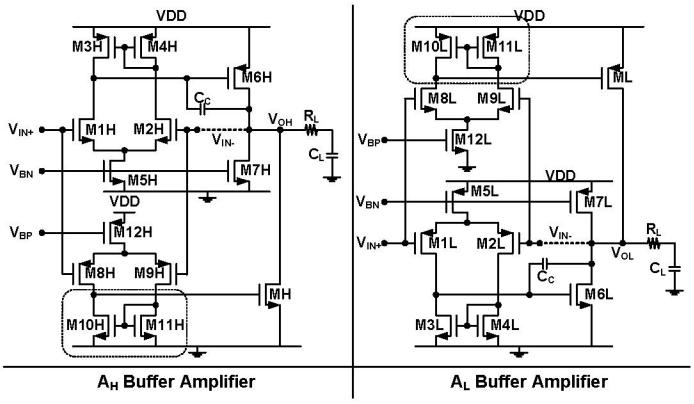

Figure 7.7.3: Schematics of the A_H and A_L buffer amplifiers.

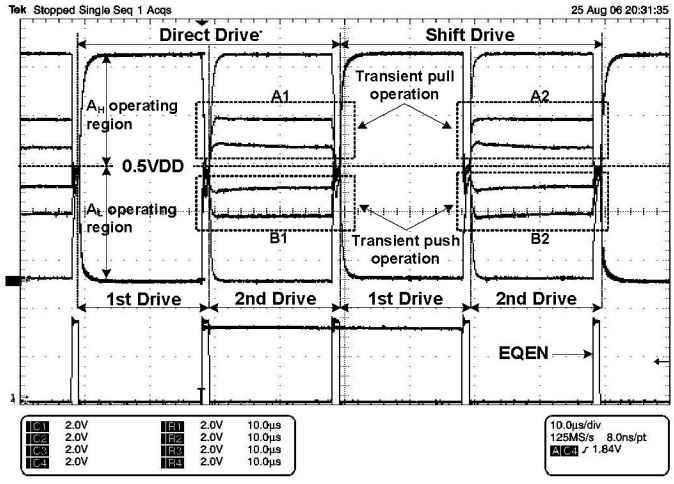

Figure 7.7.4: Output waveforms for the vertical 2-dot inversion operation.

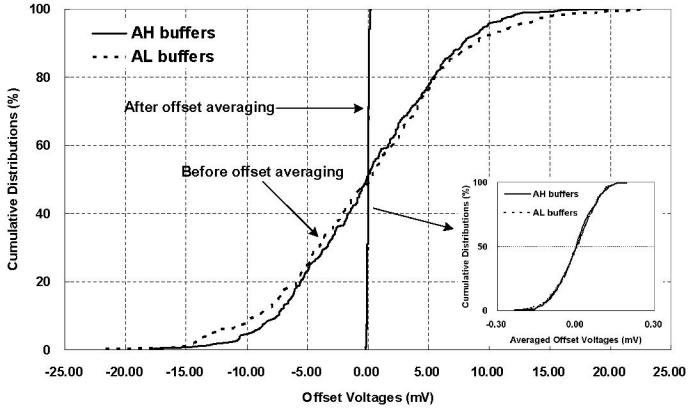

Figure 7.7.5: DC offset voltage distributions before and after offset averaging.

Technology	0.35μm CMOS (3M, 1P)
Operating voltage	13.5V (Analog), 3.3V (Logic)
Output dynamic range	13.3V (VDD-0.2V)
Static current	3.8 μA/Channel
|DC offset| (Before averaging)	< 22mV (for 720 outputs)
|DC offset| (After averaging)	< 220μV (for 720 outputs)
Buffer area portion in a chip	14.8%
Chip size	17200μm x 1350μm
Application	17.1" WXGA+ (1440RGB×900)
Color resolution	16M colors

Figure 7.7.6: Performance summary.