A NEW ZERO VOLTAGE SWITCHING RESONANT DC-LINK INVERTER WITH LOW VOLTAGE STRESS

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ABSTRACT

In this paper, a new zero voltage switching[ZVS] voltage source inverter is presented to overcome the main problems of the resonant dc-link type inverter with discrete pulse modulation[DPM] such as subharmonic problem and high voltage stress(1.3 ~ 1.8p.u.). The proposed ZVS inverter adopts a new parallel resonant dc-link and has pulsewidth modulation capability with minimum device voltage stress(1.0p.u.). In addition, the design and control of the proposed inverter are fairly simple. Operational principle, detailed analysis and design procedures are described. A 7.5kVA prototype inverter is implemented and tested with 20kHz switching frequency. Experimental results verifying the principle of operation are shown.

I. INTRODUCTION

Recently the resonant dc-link(RDCL) inverter for improvement in such demands have been studied much to reduce the switching loss and to increase the switching frequency[1-3]. Each switching in the inverter is carried out when the dc-link voltage becomes zero, resulting in many advantages such as high switching frequency, low switching loss, reduced acoustic noise and EMI and so forth. But the voltage stress problem in the inverter switches and subharmonic problem due to discrete pulse modulation(DPM) should be improved further[4-6].

A new resonant dc-link inverter topology is proposed to solve such a problems of RDCL type inverter with DPM, which is simple and suitable for high power application. This topology has most of the advantages of the conventional RDCL inverter. Moreover, the voltage stress on the inverter switches is limited to the dc supply voltage V_s. Another significant advantage of the proposed topology is that the inverter can be controlled by the conventional PWM strategy. In particular, the space vector PWM strategy is very suitable. In addition, the design and control of the resonant dc-link part are very simple. In this paper, operation principle and design procedure of the proposed topology are described in detail. The proposed RDCL inverter is implemented and tested to verify the principle of operation.

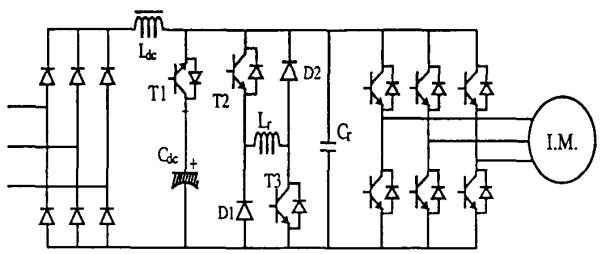

Fig. 1 The proposed ZVS resonant dc-link inverter with low voltage stress.

II. OPERATIONAL PRINCIPLES AND ANALYSES

Fig. 1 shows the proposed ZVS RDCL inverter with low voltage stress. The operational principles and analyses of the proposed inverter are explained in detail. For simplicity of explanation, the following assumptions are given :

(1) Since the switching time is short, the inverter load is regarded as current source, that is, $I_o = S_a I_a + S_b I_b + S_c I_c$ where S_a, S_b and S_c are pole switching statuses and I_a, I_b and I_c are phase currents. For example, if upper switch is on at a-phase, $S_a = 1$ otherwise $S_a = 0$.

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(2) Switching devices and resonant components are ideal.

(3) Dc-link filter inductor L_{dc} is much greater than the resonant inductor Lr, that is, $L_{dc} \gg Lr$.

Under these assumptions, the six mode diagrams of resonant dc-link operation are shown in Fig. 2, which will be explained below.

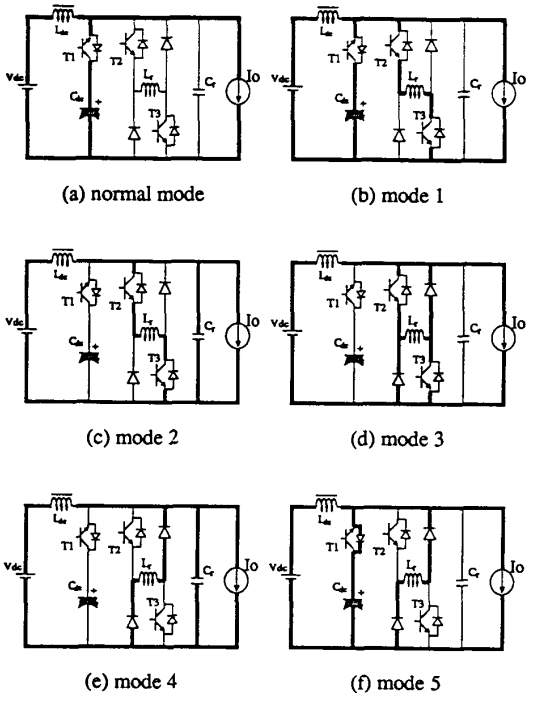


Fig. 2 Mode diagrams of resonant dc-link operation.

(1) Normal Mode

This mode has the same operation with the conventional PWM inverter. Thus each line current increases or decreases in this interval. In this mode, the resonant inductor current $i_{Lr}(t)$ and the resonant capacitor voltage $v_{Cr}(t)$ are given by

$$i_{Lr}(t) = 0 \tag{1}$$

$$v_{Cr}(t) = V_s \tag{2}$$

where V_s is the dc-link capacitor voltage.

(2) Mode 1 (Initializing Mode) : $(t_0 \sim t_1)$

At t_0, mode 1 starts by turning on T_2 and T_3 with zero current. The resonant inductor current $i_{Lr}(t)$ increases linearly with the slope of V_s/Lr. If $i_{Lr}(t)$ becomes equal to the initialized current I_i, then T_1 is turned off with zero voltage condition. If $(I_s - I_o) > I_i$, then this mode continues until $i_{Lr}(t)$ equals to $(I_s - I_o)$, where I_s is the current flowing out through the dc-link filter inductor. If $(I_s - I_o) < I_i$, then the initialization is ended when $i_{Lr}(t)$ equals to I_i. During this interval, we can write

$$i_{Lr}(t) = \frac{V_s}{Lr}t \tag{3}$$

$$v_{Cr}(t) = V_s \tag{4}$$

$$i_{Lr}(t_1) = \frac{V_s}{Lr}t_1 = I_1 . \tag{5}$$

(3) Mode 2 (Resonant Mode) : $(t_1 \sim t_2)$

After T_1 being turned off with zero voltage condition, the resonance between Lr and Cr starts. Resonant capacitor voltage $v_{Cr}(t)$ decreases resonantly from V_s to 0. At t_2, the resonant inductor current reaches the peak value in this period. The current and voltage equations are given by

$$i_{Lr}(t) = \frac{V_s}{Zr}\sin(\omega_r t) + [I_1 + (I_o - I_s)]\cos(\omega_r t) - (I_o - I_s) \tag{6}$$

$$v_{Cr}(t) = -V_s\cos(\omega_r t) - [I_1 + (I_o - I_s)]Zr\sin(\omega_r t) \tag{7}$$

$$i_{Lr}(t_2) = I_2 = I_{Lr,peak} \tag{8}$$

$$v_{Cr}(t_2) = 0 \tag{9}$$

where $Zr = \sqrt{\frac{Lr}{Cr}}$

$$\omega_r = \frac{1}{\sqrt{LrCr}}$$

(4) Mode 3 (Freewheeling Mode) : $(t_2 \sim t_3)$

In this mode, the resonant inductor current flows through the two freewheeling pathes, $T_2 - Lr - D_2$ and $T_3 - D_1 - Lr$ while the resonant capacitor voltage holds the zero value. This duration is called zero voltage period and should be long enough to satisfy the ZVS condition of the main switches in the worst case. Since the inverter switching status is changed in this mode, the zero voltage switching condition is satisfied. The PWM capability can be achieved by the control of t_3.

$$i_{Lr}(t) = I_2 \tag{10}$$

$$v_{Cr}(t) = 0 . \tag{11}$$

(5) Mode 4 (Resonant Mode) : $(t_3 \sim t_4)$

This mode starts when the switches T_2 and T_3 are turned off with zero voltage condition. The resonance between Lr and Cr is restarted. The capacitor voltage $v_{Cr}(t)$ increases resonantly from 0 to V_s and is clamped to V_s. The equations are given by

$$i_{Lr}(t) = [I_2 - (I_{on} - I_s)]\cos(\omega_r t) + (I_{on} - I_s) \tag{12}$$

$$v_{Cr}(t) = [I_2 - (I_{on} - I_s)]Zr\sin(\omega_r t) \tag{13}$$

$$i_{Lr}(t_4) = I_3 \tag{14}$$

$$v_{Cr}(t_4) = V_s \tag{15}$$

where I_{on} is the load current after the switching status changed.

(6) Mode 5 (Discharge Mode) : $(t_4 \sim t_5)$

In this mode, T_1 is turned on with zero condition when $V_{cr}(t) = V_s$. voltage. As dc-link voltage is applied back to resonant inductor, the inductor current decreases linearly by the slope V_s/Lr like the first mode. The current and voltage equations are as follows.

$$i_{Lr}(t) = -\frac{V_s}{Lr}t + I_3 \tag{16}$$

$$v_{Cr}(t) = V_s \tag{17}$$

$$i_{Lr}(t_5) = 0 \tag{18}$$

This mode ends when $i_{Lr}(t)$ becomes zero at $t = t_5$. After returning mode 0, next switching requirement is waited and the interval time can be long or short. Fig. 3 shows the typical operational waveforms of RDCL circuit.

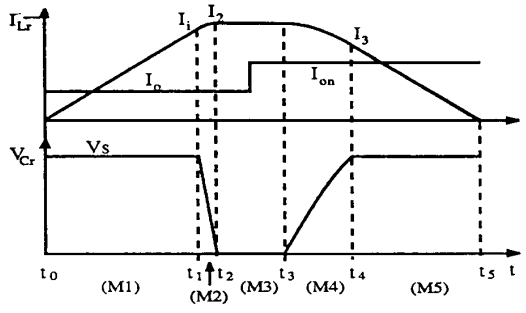


Fig. 3 The typical operational waveforms of RDCL circuit.

III. DESIGN PROCEDURE

For determining the values of resonant inductance and capacitance, the important parameters are as follows :

(1) the time between t_0 and t_2 : $(t_2 - t_0) = t_d$

(2) the time between t_2 and t_3 : zero voltage period = t_z

(3) the off time of BJT (= t_{off}) = storage time + fall time + delay time of base driver

(4) the range of $I_s = (0.2 \sim 0.5)I_{omax}$ where I_{omax} is the maximum dc-link current flowing into the inverter.

The t_d is the addition of initializing time and the first resonant time. The maximum value of this time must be determined according to t_{off}. Also, t_z must be determined so that the devices of inverter can precisely switch with zero voltage. Once switching device is fixed, t_{off} is determined. In general, t_d and t_z can be approximated as follows.

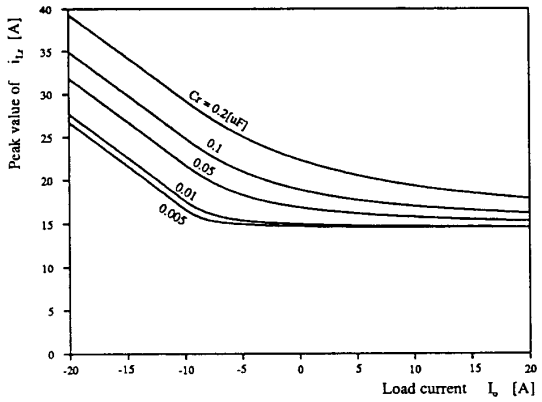
$$t_d \approx 0.8\,t_{off} \tag{19}$$

$$t_z \approx 0.2\,t_{off} \tag{20}$$

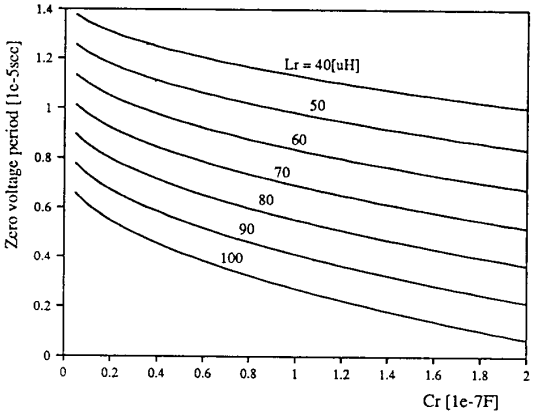
The resonant inductor current must build up enough that the resonant capacitor voltage $v_{Cr}(t)$ reaches from zero to V_s. The next condition can be obtained from eq. (15) as

$$I_{Lr,peak} \geq \frac{V_s}{Z_r} + (I_{on} - I_s). \tag{21}$$

The t_z and the total transition time $(t_5 - t_0)$ should be small enough compared to the switching interval time T_s of the inverter. In addition, $I_{Lr,peak}$ needs to be minimized. However, it is not easy to satisfy these



(a)



(b)

Fig. 4 (a) The maximum current of the resonant inductor according to the output load current for each resonant capacitor.
(b) The variation of zero voltage period according to the resonant components.

objectives simultaneously. The proper value of the resonant components can be obtained by computer simulations. Fig. 4(a) shows the maximum current of the resonant inductor according to the output load current for each resonant capacitor. Fig. 4(b) shows the variation of zero voltage period according to the resonant components in the proposed RDCL inverter. This period should be determined considering the variation of device storage time according to the output current. The voltage and current RMS stresses of the switching devices in the resonant dc-link are shown in Table I in per unit. Thus, the switching devices in the resonant dc-link is selected having the same capacity as those of the inverter.

Table. I Voltage and current stresses of switching devices in RDCL circuit.

	Peak Voltage Stress	Peak Current Stress	RMS Current Stress
T_1	1.0 p.u.	2.0 p.u.	0.7 p.u.
T_2	1.0 p.u.	2.0 p.u.	0.7 p.u.
T_3	1.0 p.u.	2.0 p.u.	0.7 p.u.

IV. CONTROL STRATEGY OF THE PROPOSED INVERTER

To avoid the complexity, a simple control method of the resonant dc-link circuit is selected. Fig. 5 shows the variation of inductor current and capacitor voltage according to the load current I_o. If the initializing

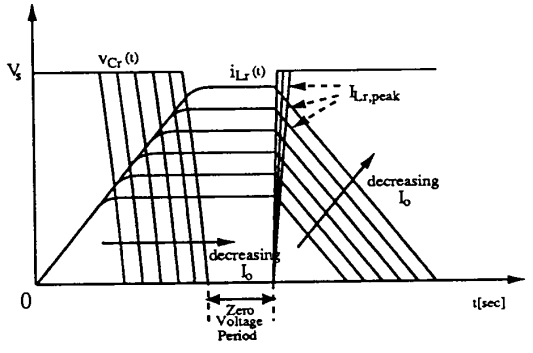


Fig. 5 The variation of inductor current and capacitor voltage according to the load current I_o.

current I_i is determined as in the previous section, then the RDCL circuit is automatically controlled by the following sequences.

(1) If $(I_s - I_o) < I_i$, the initialization is ended when $i_{Lr}(t)$ equals to I_i.

(2) If $(I_s - I_o) > I_i$, T_1 is turned off. Then, the initialization continues until $i_{Lr}(t)$ equals to $I_s - I_o$ because the remaining current flows the antiparallel diode of the switch T_1.

If T_1 is turned off when $i_{Lr}(t) = I_i$, then the freewheeling mode is determined automatically. After the switching status is changed when the inverter demands the dc-link voltage for PWM strategy, the resonant capacitor voltage raises to V_s by the resonance. The block diagram of the proposed inverter control method is shown in Fig. 6. In this case, the current control method is used for testing the proposed topology[7]. Due to the PWM capability of the proposed inverter, the space vector PWM strategy ,which is mostly preferred control method for the most of RDCL type inverter, can be applied to the proposed inverter.

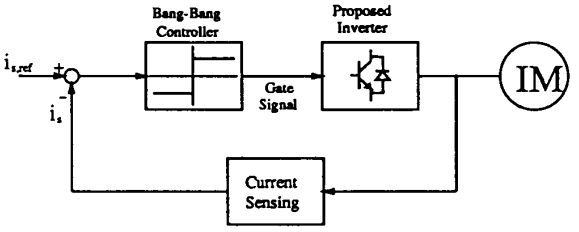


Fig. 6 Block diagram of the proposed inverter control method.

V. SIMULATION AND EXPERIMENTAL RESULTS

The proposed inverter is simulated and experimented to verify the operational principles. The inverter control method of Fig. 6 is used. The parameters used for simulations are as follows:

Resonant inductor Lr = 80 [μH]
Resonant capacitor Cr = 0.1 [μF]
Dc-link voltage V_s = 300 [V]
Motor load : 220 [Vrms] 5 [HP] motor

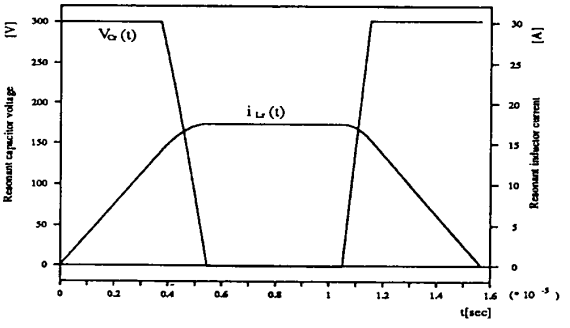
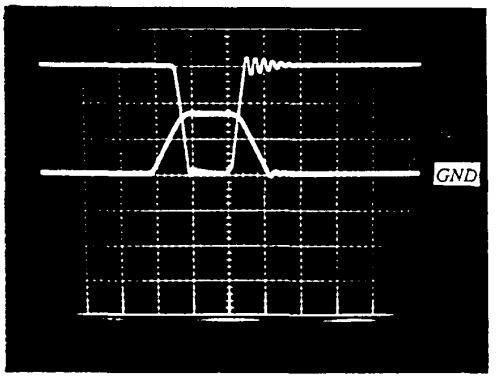


Fig. 7 The simulation voltage and current waveforms of the dc-link operation at about 20 KHz.



5 μscc/div

Fig. 8 The experimental voltage and current waveforms of the dc-link operation for verifying operational principles. (resonant capacitor voltage : 100V/div, resonant inductor current : 10A/div)

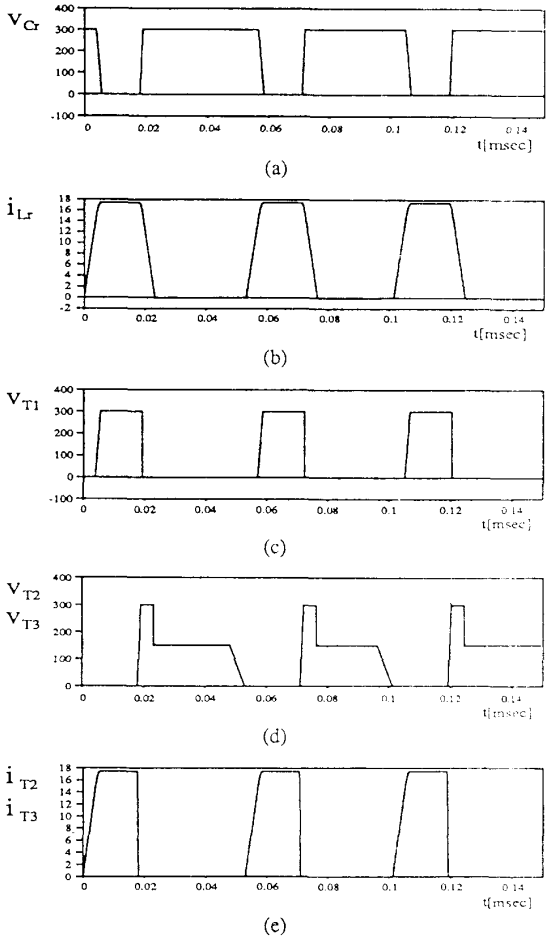
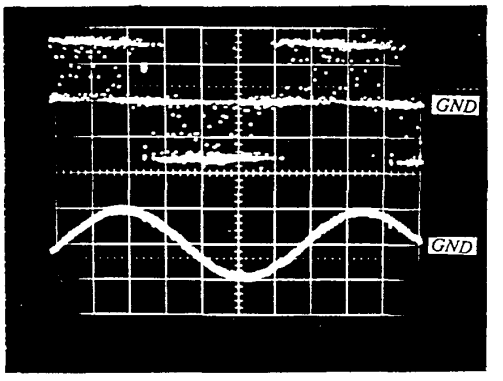
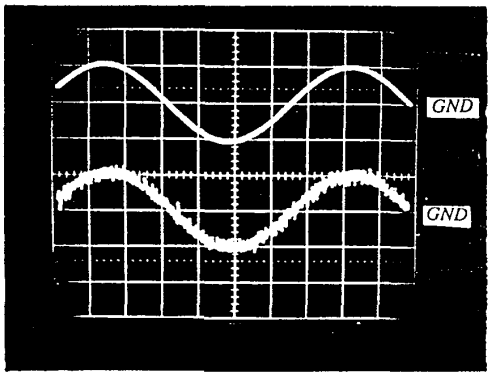


Fig. 9 Simulation results for voltage and current waveforms of the switching devices and resonant components in the resonant dc-link circuit.



5 msec/div

Fig 10 The experimental output waveforms of the prototype inverter with 5hp induction motor. (line-to-line voltage : 100V/div, line current : 10A/div)



5 msec/div

Fig. 11 Reference current(10A/div) and line current (10A/div) waveforms for comparison.

The current and voltage waveforms of the dc-link operation at about 20 KHz are shown in Fig. 7. A 7.5kVA prototype inverter is implemented and tested with 20kHz switching frequency. Fig. 8 shows the experimental current and voltage waveforms of the dc-link operation for verifying operational principles. All of the waveforms are very well matched with the analysis of the previous section. Fig. 9 shows the voltage and current waveforms of the devices in the resonant dc-link circuit. Fig. 9(a) shows that all of the inverter switching devices are clamped to source voltage V_s. Fig. 9(c) and (d) show the collector-emitter voltage waveforms of the switch T_1, T_2, and T_3, respectively. Fig. 9(e) shows the current waveforms of each switch. These waveforms give the appropriateness of Table. I. Though the current stress of each switching device can be raised to 2.0 p.u. in the worst case, the rms current stress is about 0.7 p.u.. The simulation and experimental results show that the voltage stresses on all of the

deviees are equal to the dc-link voltage V_s and the rms current stresses are small. The experimental output waveforms of the prototype inverter are shown in Fig. 10. Since the switching frequency is high, the line current is near sine wave. Fig. 11 shows that the line current coincides with the reference current.

VI. CONCLUSION

A new ZVS resonant dc-link inverter with low voltage stress is presented. The proposed inverter has not only the advantages of the conventional RDCL inverter but also low voltage stress(1.0p.u.) and low current stress. Moreover, the conventional PWM strategy is applicable to the proposed inverter. In particular, the space vector PWM technique is thought to be proper. The design and control of the proposed inverter are very simple. Operation principle and design procedure of the proposed topology are explained in detail. The proposed RDCL 7.5kVA prototype inverter is implemented and the simulation and experimental results verifying the principle of operation are presented.

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