A Fully-Integrated Low Power Direct Conversion Transmitter with Fractional-N PLL using a fast AFC Technique for CDMA Applications

Myung-Woon Hwang[†, ††], Jeong-Cheol Lee[†], Sungho Beck[†], Seungyup Yoo[†], Kyoohyun Lim[†], Hyosun Jung[†], Tschang-Hi Lee[†], Kyung-lok Kim[†], Gyu-Hyeong Cho[††], and Sangwoo Han[†]

[†] Future Communications IC (FCI) Inc., Sungnam City, Kyunggi Do, 463-020, Korea
[††] Korea Advanced Institute of Science and Technology (KAIST), Daejon City, 305-701, Korea

Abstract — **This paper presents a fully integrated low power direct conversion transmitter IC for CDMA applications. To reduce the power consumption and reduce switching time, fractional-N frequency synthesizer with an internal VCO is integrated into transmitter IC and N-target algorithm is proposed to implement Automatic Frequency Calibration(AFC). Total locking time is approximately 200μs including 80μs AFC lock time. Total current consumption for -80dBm, -10dBm, and 8dBm output power are 27mA, 33mA, and 60mA, respectively. This chip is housed in a small 5mm x 5mm 32pin MLF package.**

Index Terms — BiCMOS, Fractional-N, SDM, CDMA, transmitter.

I. Introduction

Low cost and low power consumption are the most important transmitter IC specifications, since the other performances meet the standard requirements. Direct conversion architecture is a proper solution to meet these requirements, which eliminate many external components and internal blocks [1]. Also, it is appropriate to integrate PLL and a VCO block into the transmitter IC as this provides additional advantages for lower power consumption due to the elimination of LO external driving buffers as well as low cost owing to the reduction of external components.

Fractional-N frequency synthesizer with fast automatic frequency calibration (AFC) is chosen over integer-N to achieve fast switching time, which reduces the total transmitter power consumption required during switching time. Fractional-N frequency synthesizer also allows use of smaller charge pump current than integer-N to meet switching time required to support inter-frequency hard handoff and quick paging [2].

This paper presents a 0.35um BiCMOS direct conversion transmitter IC with a fractional-N frequency synthesizer using a wideband VCO and a fast automatic frequency calibration (AFC) technique for CDMA applications. The developed transmitter IC achieves the lowest power consumption compared with other published and commercial products by fully integrating fractional-N frequency synthesizer and VCO, optimizing the signal processing block current over full dynamic range, and reducing the switching time using the proposed N-target algorithm.

II. Circuit Design and Implementation

In CDMA transmitter design, the major requirements are dynamic range, spectral mask and receive band noise, and fast switching time [2]-[3] in addition to cost and power consumption. To meet all of these requirements, the transmitter is designed using the architecture shown in Fig. 1. This transmitter IC is composed of a signal processing block, a Tx PLL with an internal VCO block, and a digital interface block.

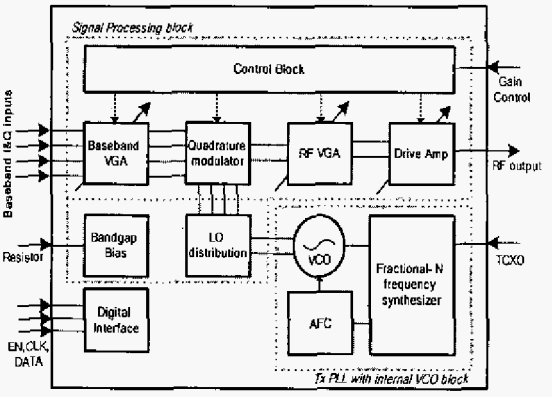

Fig. 1. Total transmitter architecture

A. Signal Processing Block

The signal processing block modulates the incoming baseband signal to the desired frequency for CDMA applications, while maintaining desired power with proper amplification. The block consists of a baseband VGA, a quadrature modulator, RF VGA, and a drive amplifier, as shown in Fig. 1.

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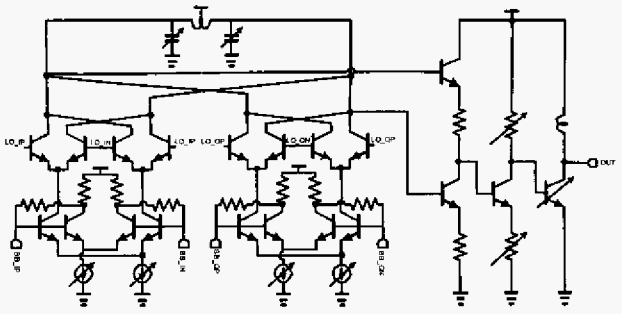

Fig. 2. Simplified signal processing block schematic

To reduce the power consumption, total dynamic range is distributed over the baseband VGA, RF VGA, and drive amplifier. Also the block current is reused and optimized according to the output power. The baseband VGA controls the input signal level to the modulator in order to expand dynamic range. The quadrature modulator consists of two Gilbert mixer cores and internal LC load used to minimize power consumption while achieving maximum gain as shown in Fig. 2. The RF VGA and drive amplifier are adopted to expand the dynamic range of the transmitter and achieve high linearity with low power consumption by optimizing device size and bias level according to output power level.

To reduce the process and temperature variation, a digitized capacitor bank is incorporated to internal LC tuned load of quadrature modulator, which insures gain flatness at each operating band. Process and temperature insensitive gain and bias current control blocks are designed for each block to achieve required performance while consuming smallest current. LO distribution circuitry using divided-by-2 and limiting amplifiers make RF performances of signal path insensitive to LO power generated from internal VCO.

To reduce the cost by minimizing external matching components, internal inductor is used as a load for maximum power transfer to the external power amplifier, so only one external capacitor is required for 50 ohm matching at the output port.

B. Tx PLL with interanl VCO

The fractional-N frequency synthesizer with fully integrated VCO is designed to obtain fast switching time required for CDMA applications. This block is optimized to consume the low current while satisfying the constraints for phase noise, channel spacing, and reference spur. The block diagram of fractional-N frequency synthesizer is shown in Fig. 3. The synthesizer consists of PFD, a charge pump, a programmable divider, a Δ-Σ modulator, a voltage controlled oscillator (VCO), and an automatic frequency control block (AFC) using the proposed N-target algorithm.

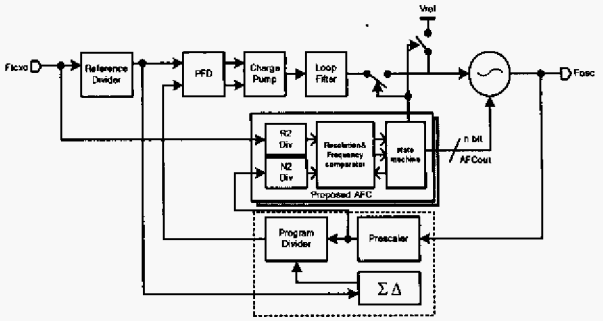

Fig. 3. Proposed Δ-Σ fractional-N frequency synthesizer block diagram

The charge pump block uses a feedback error amplifier to reduce the mismatch between up and down current for lower spurious level and noise. The Δ-Σ modulator is designed with a 4th order multistage-noise-shaping (MASH) structure having 20bit resolution, because MASH has no stability problem and good noise shape performance. VCO is based on a standard negative gm topology coupled to an LC tank. Cross-coupled NMOS and PMOS core is used for negative gm to reduce the phase noise. To overcome the process variation, digital capacitor banks are included, which are calibrated by the AFC using the proposed N-target algorithm.

Frequency resolution and AFC lock time are key parameters to design the AFC [4]. There is a trade-off between these two parameters because the AFC lock time is increased when the frequency resolution is reduced. The proposed AFC architecture shown in Fig. 3 provides the proper VCO bank bits, which consists of a R2 divider, a N2 divider, a frequency comparator and a state machine. For proper frequency resolution and AFC locking time, the R2 divider number is determined by

$$R2 = F_{tcxo} \cdot T_{comp}$$
$$N2 = R2 \cdot F_{res} / F_{tcxo} \quad (1)$$

where F_{TCXO} is TCXO frequency, and T_{comp} is one unit digital calibration time, which is determined by the frequency resolution. Hence, the total AFC lock time is

$$\begin{aligned} T_{AFC} &= T_{comp} \cdot 2^{N_{VCObank}} && \text{for linear search algorithm} \\ &= T_{comp} \cdot N_{VCObank} && \text{for binary search algorithm} \\ &= T_{comp} \cdot K && \text{for proposed N - target algorithm} \end{aligned} \quad (2)$$

where $N_{VCObank}$ is the number of VCO bank bits and K is the number of calibration iterations at the N-target algorithm. The N-target value is pre-defined by

$$N_{target} = \frac{F_{channel} \cdot R2}{F_{tcxo} \cdot N2 \cdot P} \quad (3)$$

where $F_{channel}$ is the desired output channel frequency and P is the prescaler divider number.

The N-target algorithm has two operation modes: coarse mode and fine mode. At coarse mode, the state machine sets the center bank number to the VCO bank and the divided VCO output signal is counted during T_{comp} period, which is defined as N_{gen}. Hence, the VCO bank difference ($Bank_{diff}$) from the center bank is simply calculated by

$$Bank_{diff} = \frac{F_{res}}{F_{step}} \times (N_{gen} - N_{target}) \quad (4)$$

and the coarse VCO bank number is determined by adding the VCO bank difference to the center bank number. At fine mode, the desired VCO bank number is finally defined using a linear search algorithm to reduce the bank error due to the variation of the VCO gain slope and the frequency step of the bank. The K value is the calibration number of linear search, which is about 1~3. Thus, the proposed N-target algorithm has fast AFC lock time when the VCO has many banks, because this algorithm is insensitive to bank number. This proposed AFC architecture is designed to use the TCXO input and prescaler output for low power consumption and reduction of layout area.

C. Implementation

A microphotograph of the direct conversion transmitter IC for CDMA applications is shown in Fig. 4. The designed chip is fabricated using 0.35um SiGe BiCMOS process. This chip is packaged in a small 5mm × 5mm MLF 32-pin chip-scale package.

Block floor planning and layout technique also play a significant role in a mixed/analog IC implementation. Several guard rings using n-well and p-well are used for isolation between the signal processing block and TxPLL block. Symmetric layout for the modulator, LO, and VCO is also important to reduce LO leakage to RF output port to get high waveform qualify factor.

III. Measured Results

The device operates over a 2.7V to 3.0V supply voltage and an ambient temperature range of -30°C to 85°C. The transmitter performance is summarized in Table I and is measured at 2.7V supply voltage and room temperature. The CDMA modulation spectrum in the CDMA band is shown in Fig. 5 and the output spectrum satisfies the spectrum mask specification with sufficient margin. Fig. 6 shows the total current consumption, ACPR1, and ACPR2 over the full output dynamic range and Fig. 7 shows the output power and gain slope versus the control voltage percentage of supply voltage. Fig. 8 shows the total PLL locking time including AFC lock time. Period (a) is AFC lock time, about 80us, and period (b) is the closed loop PLL locking time, about 120us, where the PLL loop bandwidth is about 30kHz and F_{res} is 4.8MHz. Fig. 9 shows the close loop phase noise performance of the internal VCO and Fractional-N PLL. There is no degradation of phase noise due to fractional-N noise.

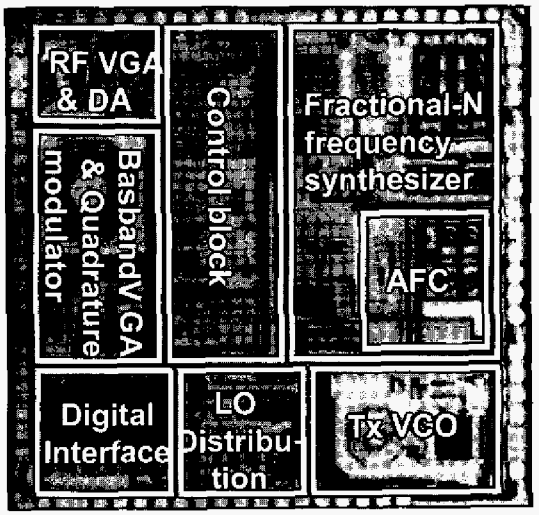

Fig. 4. Chip microphotograph of transmitter IC.

IV. Conclusion

A direct conversion transmitter IC compliant with the TIA-EIA 98D specifications is fully integrated with a fractional-N frequency synthesizer using a wideband VCO and a proposed fast AFC technique for CDMA applications. This transmitter achieves the lowest current consumption, fast switching time, and high linearity

Acknowledgement

The authors wish to acknowledge FCI Quality & Product Engineering team for measurement support and FCI ZS team for software programming and measurement automation setup.

References

[1] Kevin Card, et al., "Direct Conversion Dual-Band SiGe BiCMOS Transmitter and Receive PLL IC for CDMA/WCDMA/AMPS/GPS applications", *IEEE International Solid-State Circuit Conference,* Digest of Technical Papers, pp.,272-273.

[2] TR-45, "Introduction to CDMA 2000 Standards for Spread Spectrum Systems", *TIA/EIA/IS-2000.1-A,Ballot resolution Version*, March 2000.

[3] Madhukar Reddy, et al., "Highly Integrated Dual Band/Tri-mode SiGe BiCMOS transmitter IC for CDMA Wireless

Applications ", 2002 *IEEE Radio Frequency Integrated Circuits Symposium Digest*, pp.35-38.

[4] Han-il Lee, et al., "Sigma- Delta Fractional-N Frequency Synthesizer using a wideband integrated VCO and a fast AFC technique for GSM/GPRS/WCDMA Applications", IEEE 29th European Solid-State Circuits Conference, Sep.2003, pp. 97-100.

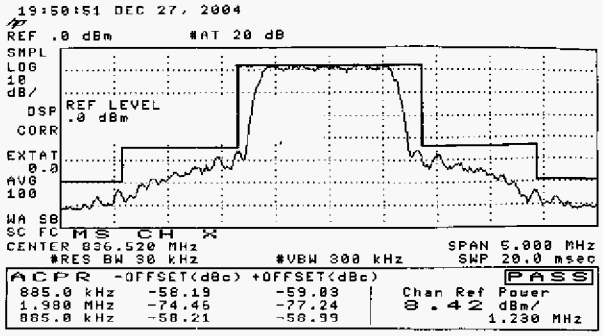

Fig. 5. Measured output modulation spectrum in CDMA band

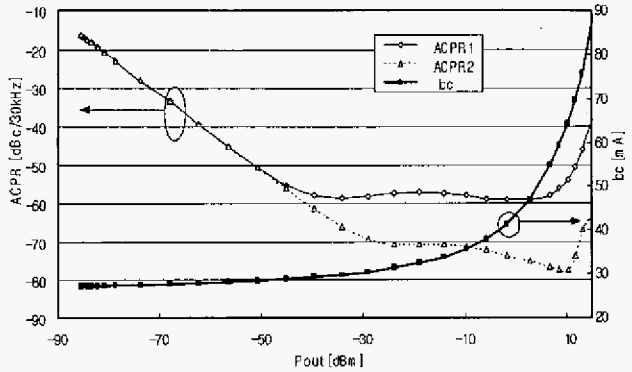

Fig. 6. Measured current consumption and ACPR1/ACPR2 versus output power

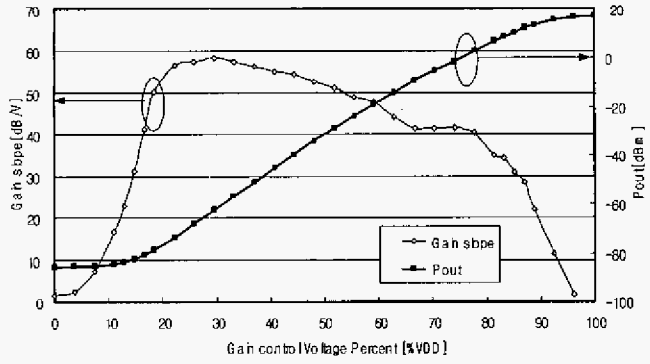

Fig. 7. Measured output power and gain slope versus gain control voltage percentage of supply voltage

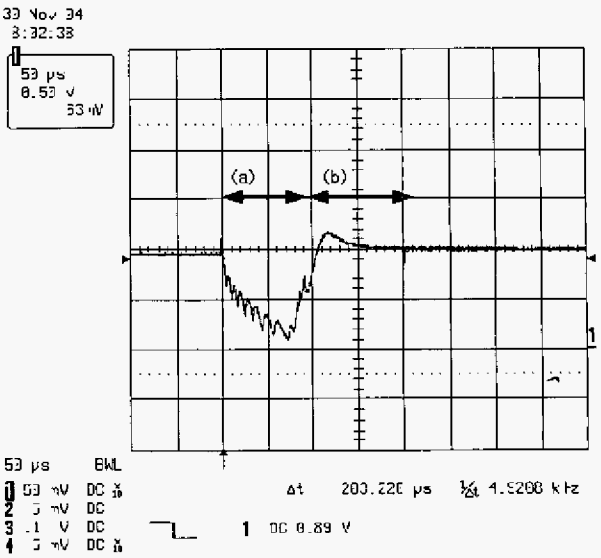

Fig. 8. Measured PLL locking feature including AFC locking operation at charge pump output node

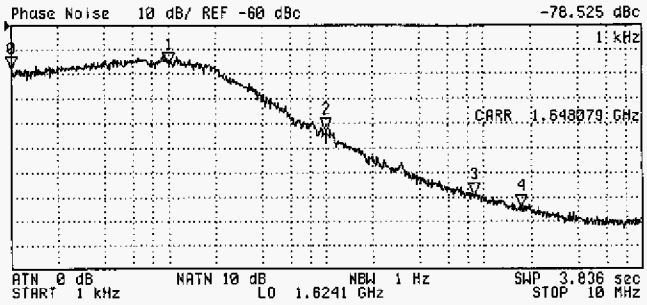

Fig. 9. VCO and Fractional-N PLL closed loop phase noise

TABLE I

SUMMARY OF MEASUREMENTS AT 2.7V, 27C

		Measured Results
Frequency range		824 ~925 MHz
Maximum output power		8 dBm
Minimum output power		-80 dBm
ACPR1 @ max power (+ 885kHz)		-58 dBc / 30kHz
ACPR2 @ max power (+ 1980kHz)		-74 dBc / 30kHz
LO leakage @ max power		25 dBc
@ min power		9 dBc
Image rejection @ max power		25 dBc
Rx band noise (+45MHz) @ max power		-136dBm/Hz
VCO phase noise @ 900kHz offset		-130 dBc
AFC time		~ 80 us
Total PLL locking time		~ 200us
Current consumption	@ 8dBm	60 mA
	@ -10 dBm	33 mA
	@ -80 dBm	27 mA
	@ power off	10 uA