Program-Controlled Soft Switching PRDCL Inverter with New Space Vector PWM Algorithm

Wan Yi, Hyo L. Liu, Yong C. Jung, Jung G. Cho, and Gyu H. Cho

Dept. of Electrical Engineering,
Korea Advanced Institute of Science and Technology(KAIST)
#373-1 Kusong-dong Yusong-gu, Taejon 305-701 Korea (Fax:82-42-869-3410)

Abstract

A soft switched space vector PWM inverter is developed using new parallel resonant dc-link (PRDCL) [7,8]. This PRDCL can operate on variable dc-link pulse position and width resulting in enhanced PWM capability, which is superior to other resonant dc-links. A new space vector algorithm is presented suitable for this PRDCL inverter. The suggested algorithm is able to eliminate narrow PWM pulse which impede dc-link operation. This PWM control, however, requires complex and precise timing sequences in relation to PRDCL operation, which is nicely solved by adoping new programed controller with a buffer and a programmable timer.

I. Introduction

The soft switching has been regard as the considerable technique to overcome many problems encountered in power inverter design, particularly considering switching loss and limited switching frequency. It takes many advantages over the hard switching inverters such as high power density, low EMI, low acoustic noise and high dynamic performance resulting from high switching frequency.

Many inverter circuits exploiting a soft switching technique has been proposed and studied extensively [1-6]. Among them, especially the voltage source type, actively clamped resonant dc-link (ACRDCL) inverter [1] is considered to be successful topology. It has, however, several disadvantages that come from discrete pulse modulation (DPM) which causes a subharmonic problem, higher device voltage stress (1.3-1.5 p.u.) and conduction loss in resonant operation. To overcome these problems, several approachs were tried, but they still exposed other kinds of problems.

Another approach for soft switching PWM inverter was suggested using parallel resonant dc-link (PRDCL) which also provided variable dc-link pulse width [3,4]. It had some merits, however, it also showed several disadvantages such as many excessive devices (4 devices) including fast and high voltage (2.0 p.u.) devices and restricted PWM capability.

New topology of PRDCL inverter is presented recently and illustraited in Fig. 1 [7,8]. This PRDCL allows variable off-pulse width and on-pulse width of dc-link voltage which greatly raises the PWM capability. Minimum voltage stress (all 1.0 p.u.), low device current stress and reasonable additional device count enable the new PRDCL inverter to be able to implement for wider power range.

Also new space vector algorithm which is convenient for this PRDCL inverter is suggested and explored in this work. This algorithm makes it possible to eliminate narrow PWM pulse which impede dc-link operation. Finally, this PRDCL inverter is realized using programmed controller with external circuits which guarantee the precise timing sequences and the experimental results are demonstrated.

II. Reviews of PRDCL Operation

To understand the requirement of PRDCL inverter control , the operation are briefly reviewed.

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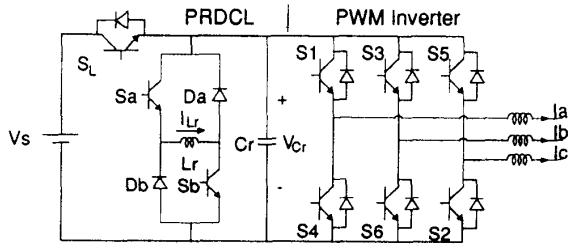


Fig. 1 Proposed PRDCL Inverter

Since the resonant inductor Lr is sufficiently smaller than the load inductance, the inverter with three phase load can be replaced by current source during the switching period. The PRDCL operation is divided into six operational modes which are illustrated in Fig. 2. The Fig. 3 is the waveform of the dc-link operation as for each mode.

Mode 0 : (SL:on, Sa & Sb:off)
This mode is normal operation mode in which the load current Io is flowing through SL.

Mode 1 : (SL:on, Sa & Sb:on)
To operate dc-link robustly, it requires initial inductor current. The Sa and Sb are turned on with zero current switching, then the resonant inductor current ILr is increase linearly to the desired value of Ii.

Mode 2 : (SL:off, Sa & Sb:on)
When the switch SL is turned off with zero voltage condition, the Lr and Cr circuits resonate with offset current Ii.

Mode 3 : (SL:off, Sa & Sb:on)
The very moment the resonant capacitor voltage VCr reach to zero, the resonant inductor current is freewheeling through the paths Sa-Da and Sb-Db.

Mode 4 : (SL:off, Sa & Sb:off)
To return the capacitor voltage VCr to the source voltage Vs, the switches Sa and Sb are turned off with zero voltage condition.

Mode 5 : (SL:on, Sa & Sb:off)
When the resonant capacitor voltage VCr is excess than the source voltage Vs, the capacitor voltage is clamped to the source voltage Vs and the remained energy in the resonant inductor is returned to the voltage source.

The required time for each mode should be considered to achieve successful the PRDCL operation. These are illustrated in the following table.

Mode	Required Time
Mode 0	Variable
Mode 1	$T1 = \frac{Lr\,Ii}{Vs}$
Mode 2	$T2 = \frac{1}{\omega r}\tan^{-1}\left(\frac{Vs/Zr}{Ii+Io}\right)$
Mode 3	Variable
Mode 4	$T4 = \frac{1}{\omega r}\sin^{-1}\left(\frac{Vs/Zr}{Ip-Io}\right)$
Mode 5	$T5 = \frac{Lr\,Ir}{Vs}$

where $\omega r = 1/\sqrt{Lr\,Cr}$ and $Zr = \sqrt{Lr/Cr}$.

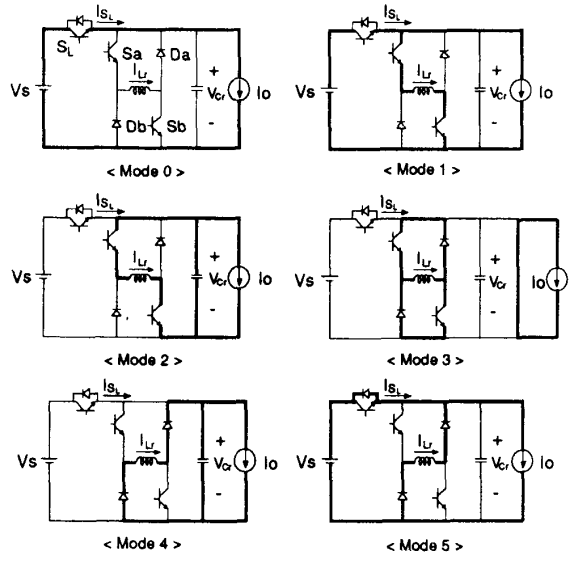


Fig. 2 Mode diagrams of the PRDCL operation

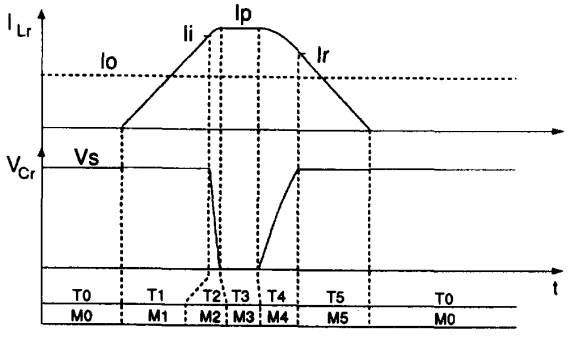


Fig. 3 Waveform of the PRDCL operation

III. New Space Vector PWM Algorithm

As mentioned previous chapter, the PRDCL inverter will change the switching pattern during the dc-link freewheeling operation. It is explicit that the dc-link operations require the minimum time for the current built-in, the resonant, and the restoring. These restrict the PWM pulse width and cause the narrow pulse problem. The conventional PWM methods such as the sinusoidal PWM, the harmonic injection PWM, the selective harmonic elimination PWM, hysteresis PWM, etc., can not be implementable for the PRDCL inverter without solving these problems because the dc-link operations should be predicted and the PWM pulse widths should be longer than the required minimum pulse duration. One solution was proposed previously named as the delta pulse modulation (DPM), however, it have sub-harmonic problem inherently. It requires higher switching frequency than the others to overcome such a problem .

As discussed in the above, the PRDCL inverter like the other resonant inverters needs PWM algorithm satisfing the following conditions:

1) minimum dc-link pulse density,
2) minimum harmonics,
3) minimum pulse duration for robust dc-link operations.

The space vector PWM method are well known and the harmonics characteristics is better than the others maintaining lower switching frequency. Also the switching time can be adjusted in the space vector PWM by varying the sampling angles. These features are well suited for the PRDCL inverter control algorithm. But the conventional space vector design processes should be modified to attain the above conditons successfully. The following paragraphs describe the design and the validation processes.

The Space Vector PWM:

The space vector PWM algorithm is well studied and there exists three possible trajectories which are illustraited in Fig. 4. Those are well analized with respect to the harmonics in the previous works [11]. Since the scheme of (c) in Fig. 4 attains lowest switching density having comparable harmonic characteristics, it is the most attractive control algorithm for the PRDCL inverter than the others. If the scheme is somewhat modified with proper considerations, it is well suited for this PRDCL control algorithm.

Adjusting the sampling angles, wTs, the narrow pulses can be removed in the design processes to satisfy the condition 3) which is verified in the simulation and the experiment.

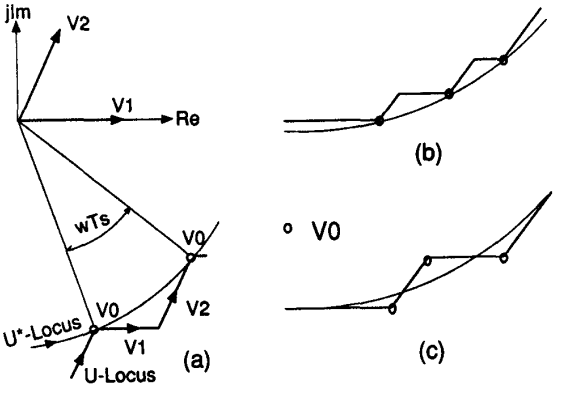


Fig. 4 Schemes of space vector PWM

Flux Error Definition:

The flux error in the space vector PWM is illustrated in Fig. 5. This flux error E caused by the difference from the reference flux U*(t) to the generated flux U(t), it can be divided into two vector components of the angular error, E-angular and the radial error, E-radial in the Fig. 5 (b). It was studied recently that the torque pulsation of the induction machins is more affected by the angular error than the radial error [13]. In this work, both of the two errors, flux error and angular error, are considered.

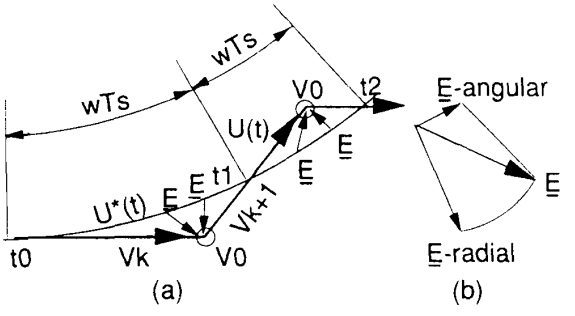
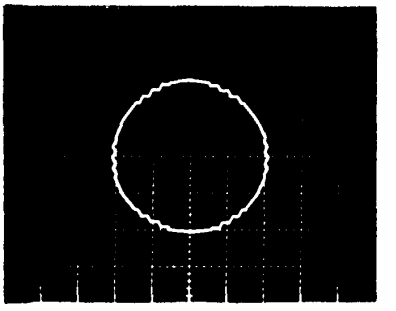


Fig. 5 Definitions of the flux error

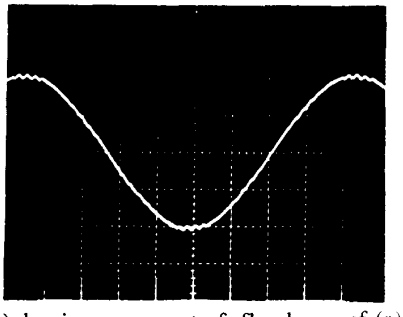
The Constrained Error Minimization:

The PRDCL PWM control data is generated by the constrained error minimization technique. The constrain used here is the minimum PWM pulse width to operate dc-link for a given switching frequency. The error minimization is achieved by the equal distribution of the maximum error within the subsectioned wTs with respect to the whole reference flux trajectory.

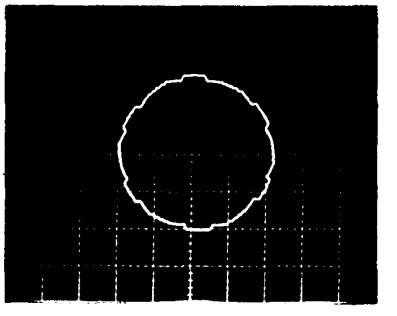
Since the reference flux and the generated flux coincide at t0, t1 and t2, the flux error E is becoming larger along U(t) in Fig. 5 (a). It is maximum at dc-link operation time. In order to minimize the flux error (even though angular error), the absolute flux error should be distributed as evenly as possible with respect to the whole the reference flux circle U*(t). But this minimization will be limited by the minimum pulse duration.



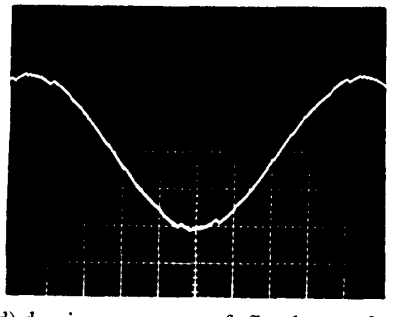
(a) flux locus of angular error criterion



(b) d-axis component of flux locus of (a)



(c) flux locus of flux error criterion



(d) d-axis component of flux locus of (c)

Fig. 6 New space vector algorithm

The above design algorithm have been examined by the simulation. The simulation results inform that the different PWM patterns are generated depending on the minimizing objects, i.e. the absolute flux error and the absolute angular error. These show us the similar results to the previous work [13]. To verify the new PWM algorithm, the generated PWM sequences are run on the PWM simulator. The simulator output are well coincided with the simulation and the differences between the two error criteria are well shown in Fig. 6.

IV. Implementation

The generated PRDCL PWM switching patterns which have been attained by the new space vector PWM algorithm, has complex and precise control timing sequences requiring more flexible controller. This timing sequences have to be generated and outputed at exact switching time in order to guarantee the safe PRDCL operation. Moreover, the control sequences vary with respect to time. These facts force adoping a processor based controller.

Most of the microprocessor based system use the interrupt to generate time intervals notwithstanding the time jitter and delay of interrupt response. It frequently cause missing of the control signals for the dc-link operation or hard switching of the inverter switches which diminish its performance. The PRDCL inverter requires too short time intervals for the processor to respond even though it has surplus throughput globally. The required data amount are also so large that the processor can not respond exact time, if the switching frequency is high.

The proposed controller scheme is able to solve the fore mentioned problems. The controller blockdiagram is configured in Fig. 7. It adopts one programmable timer and two buffers which operate independently from the processor. The programmable timer carries out interval pulses of clock period units and the buffers store timing and control output data. The processor generates control chart for specified frequency and modulation factor, then it is loaded to the buffer. The pointed buffer contents by the sequence counter are loaded to the timer and the output port. In the case of frequency change during the operation, the new data are loaded to the unused buffer, then the using buffer is changed at a proper time.

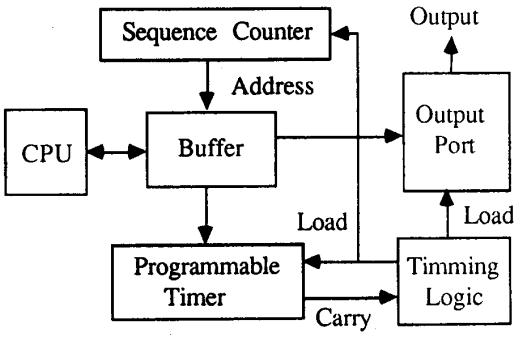
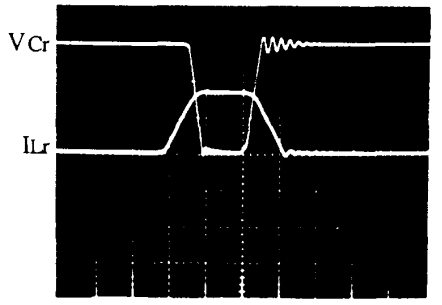


Fig. 7 Configuration of programmable controller

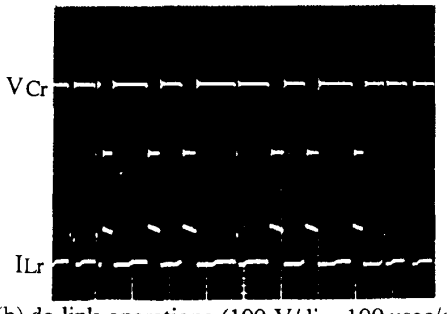
With this programmable controller, the two methods having different flux error criteria, are experimented and successful results are attained as shown in Fig. 8. The switching frequency is effectively 10 KHz. It can be noticed that the angular flux error minimization criterion is superior to the flux error minimization one.

V. Conclusions

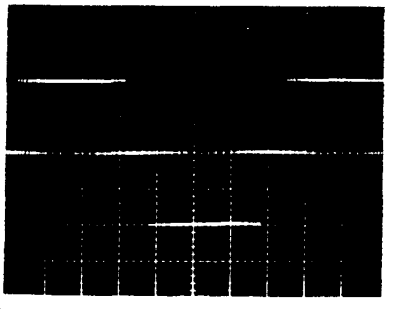
A program controlled soft switching PRDCL inverter is presented. It is verified that the programmed control with the new space vector PWM algorithm is applicable for this new PRDCL inverter. The proposed control scheme is also implementable the other PRDCL inverter and the VVVF inverter with high switching frequency. The controller with special hardware is designed to keep complex and fast control sequences which is beyond from the full program control. The space vector PWM is also adequate to adjust narrow PWM pulses different from the other PWM schemes. Because of the low voltage stress and low switching loss, the proposed PRDCL inverter equipped with processor based control can operate in a range with higher power and higher switching frequency.



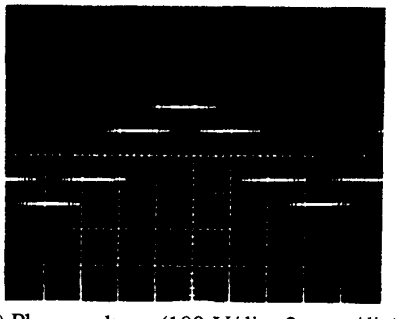
(a) Single dc-link operation (100 V/div, 5 usec/div)



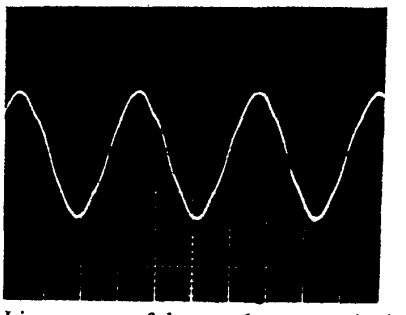
(b) dc-link operations (100 V/div, 100 usec/div)



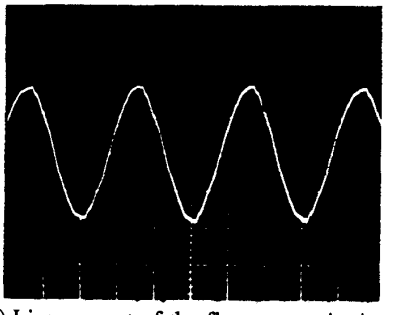
(c) Line-to-line voltage (100 V/div, 2 msec/div)



(d) Phase voltage (100 V/div, 2 msec/div)



(e) Line current of the angular error criterion (10 A/div, 5 mSec/div)



(f) Line current of the flux error criterion (10 A/div, 5 msec/div)

Fig. 8 Experimental results

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