An Integrated CMOS DC-DC Converter for Battery-Operated Systems

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Abstract -- This paper presents an optimum design for low-voltage, low-power DC-DC converter which has a controller and integrated CMOS switches using small size inductor (1uH). Optimum design for single chip DC/DC converter is achieved by analyzing the amount of conduction and switching losses. Through the loss analyses, it is turned out that a constant frequency hard switching PWM converter with synchronous rectifier is most suitable among the several kinds of DC-DC converters for low voltage and low power applications.

I. Introduction

In recent years, the number of portable personal communication systems such as mobile telephones, pagers and laptop computers has grown explosively. The miniaturization of power modules located inside portable systems is in progress. The size of the DC-DC converter is important for portable systems. Therefore, a technology for inductor and capacitor to make miniaturization and high frequency operation is urgently needed. In addition, a corresponding control-circuit techniques are also needed. Most DC-DC converters usually operate in the range of 100 kHz to 500 kHz, which are not suitable for further reduction of the sizes of passive elements.

This paper describes an optimum design for a small, low-voltage (3 V), low-power (1~2 W) single chip buck converter with synchronous rectifier. The high side and low side switches are PMOS and NMOS, respectively. The low side synchronous rectifier (NMOS) is used to reduce conduction loss. Their internal switches and synchronous rectifier eliminate the necessity of the external MOSFET and Schottky diode, reducing size and cost. The inductance is reduced less than 3uH by increasing the switching frequency up to 2 MHz. As the output power is small, the control circuit and the output switches are fabricated on one chip. In the small size switch, dominant loss comes not from switching loss but from conduction loss. Hard switching is more suitable than soft switching to minimize the loss. Optimum design for switch size and the selection of the switching frequency are described in the following.

II. Loss analysis

A buck converter with synchronous rectifier is shown in Fig. 1. C_{gs}, C_{gd} and C_{ds} are parasitic capacitors.[1] These parasitic capacitors cause switching losses. In addition, on resistance of PMOS and NMOS and series resistance of inductor produce conduction losses. If the size of switch is increased, conduction loss is decreased while switching loss is increased. In order to determine the optimum switch size, it is necessary to account for the switching loss and the conduction loss as a function of frequency and switch size. In our loss calculation, we made the following assumptions:

·V_{in}=5 V, V_{out}=3 V, L(Inductor)=600 nH,
Switching Frequency=2 MHz, R_{out}=10 Ω, $R_{inductor}$=0.5 Ω

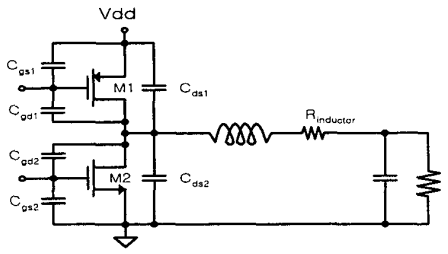

Fig. 1 Parasitic capacitors and series resistor of inductor in buck converter with synchronous rectifier

In Fig. 2, we can see that conduction loss is higher than switching loss. It is necessary to reduce the conduction loss rather than switching loss in order to achieve higher efficiency. The resonant converters, which are generally used in the high frequency region to reduce the switching loss, are not proper methods to raise efficiency in this low voltage case. As an example, zero voltage switching resonant converter makes

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use of resonant current to achieve zero voltage condition at each switching instant, but rms value of resonant current becomes higher than that of hard switching PWM converter. Thus, the total efficiency of resonant converter is reduced owing to high conduction loss caused by resonant current.

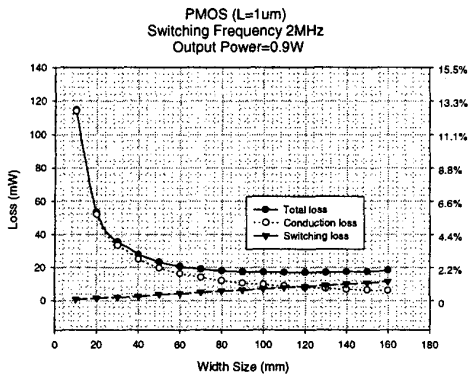
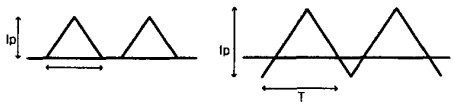


Fig. 2 PMOS Loss (Optimum switch size : 80 mm)



(a) (b)

Fig. 3 Inductor current : (a) Hard switching PWM ; (b) QSC

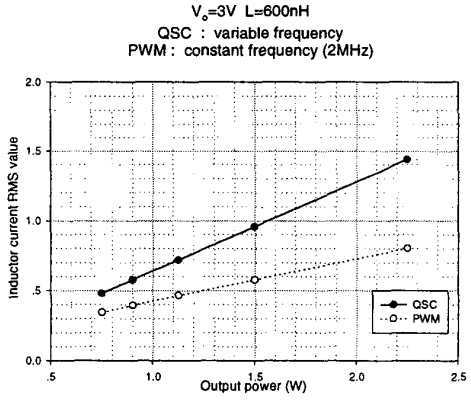


Fig. 4 Comparison of rms current value between QSC and PWM converter

In Fig. 4, the efficiency of hard switching PWM converter is compared with that of QSC (quasi square wave converter) [2, 3] which is generally used in small power DC-DC converter. In case of QSC, inductor current should form negative current to make zero voltage switching condition as shown in Fig. 3. Negative current causes wasteful power loss because the rms current of QSC is higher than that of PWM converter. So we can say that hard switching PWM converter is more suitable than QSC in this low voltage and low power case.

Optimum switch sizes are determined by investigating the lowest point of total loss from Fig. 2. The results are as follows:

- PMOS W/L=80,000
- NMOS W/L=30,000.

III. Control circuits

Control circuit block diagram for synchronous PWM buck converter is shown in Fig. 5. DC-DC converter topology, control mode and switch sizes are determined by loss analyses. We have developed a control IC capable of operating at high-frequency with low-power dissipation. Control block is composed of two blocks: one is digital block and the other is analog block. Digital block consists of logic circuits, flip-flops, shoot though protection circuit, gate driver and triangular waveform generator. Op-amp, comparators and band-gap reference are in the analog block.

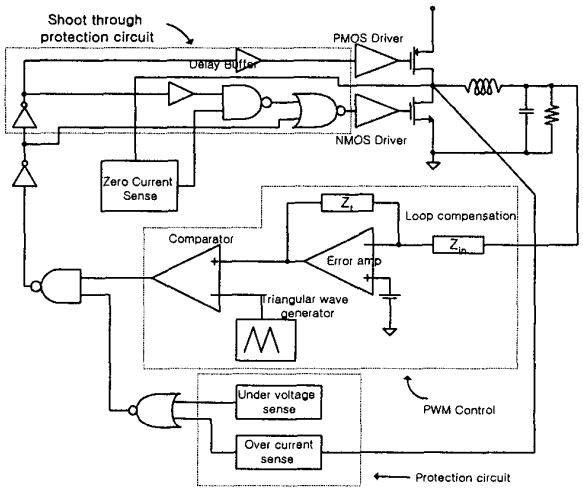


Fig. 5 Control circuit block diagram

A. *Zero Current Sensing block*

In the discontinuous current mode, NMOS should be turned-off when the inductor current reaches zero. Inductor current can be sensed by a series resistor, but it is not a good method in this case because of additional power loss in the series resistor.

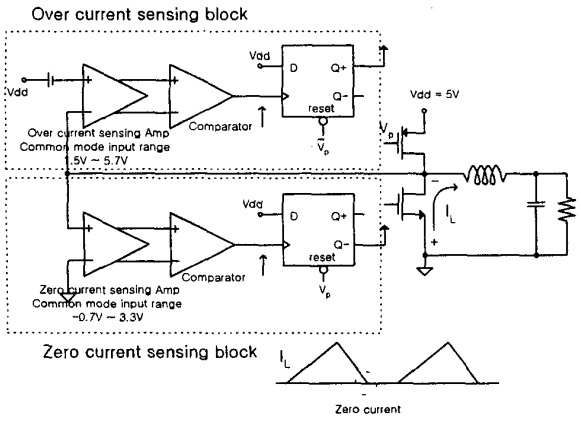


Fig. 6 Zero current and over current sensing block

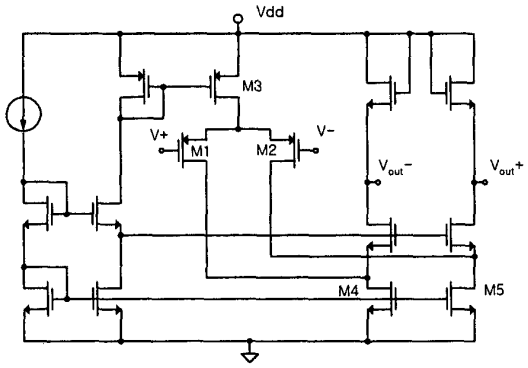


Fig. 7 Zero current sensing amplifier

To eliminate the wasteful power loss, the zero current is sensed by the on resistance voltage drop across drain and source of NMOS in our design. When the inductor current reaches 1A, the maximum voltage drop between drain and source becomes about 100 mV which is not enough to overcome the offset voltage of comparator. Hence the voltage between drain and source of NMOS is amplified nearly twenty times before feeding into the comparator, as shown in Fig. 6. During the conduction period of NMOS, the zero current sensing amplifier is designed to treat the common mode voltage around zero by using folded cascode structure with PMOS input differential pair. The common mode input voltage range of Fig. 7 is given by:

$$\begin{aligned} V_{\min} &= 0 + V_{p4} + V_{p1} - |V_{gs1}| \\ &= V_{p4} - |V_{TP}| \\ V_{\max} &= Vdd - V_{p3} - |V_{gs1}| \end{aligned} \tag{1}$$

Zero-current sensing amplifier is shown in Fig. 7 and the test waveform is shown in Fig. 11.

B. Over-current protection block

Over-current protection circuit is needed to protect DC-DC converter from being damaged by the shock of over-current. In this design, over-current is sensed by the on resistance of PMOS with the exactly opposite manner of zero current sensing, as shown in Fig. 6. When the inductor current reaches the preset value, PMOS switch is turned-off by disabling the signal from the PWM controller. By doing so, the maximum current is always limited within a safe range even for an over loaded case. Over current sensing amplifier is shown in Fig. 8.

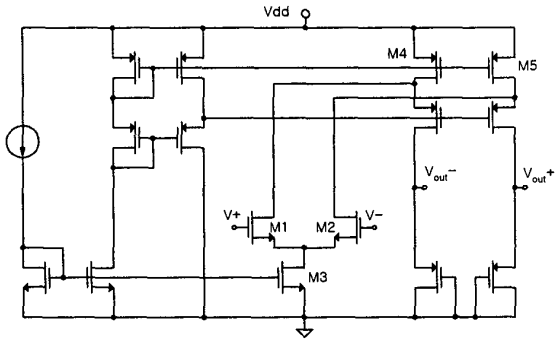


Fig. 8 Over current sensing amplifier

And this amplifier is designed to be that the common mode voltage range is around the supply voltage Vdd by using folded cascode structure with NMOS input differential pair. The common mode input voltage range of Fig. 8 is given by:

$$\begin{aligned} V_{\min} &= V_{GS1} + V_{p3} \\ V_{\max} &= V_{dd} - V_{p4} - V_{p1} + V_{GS1} \\ &= V_{dd} - V_{p4} + |V_{TN}| \end{aligned} \tag{2}$$

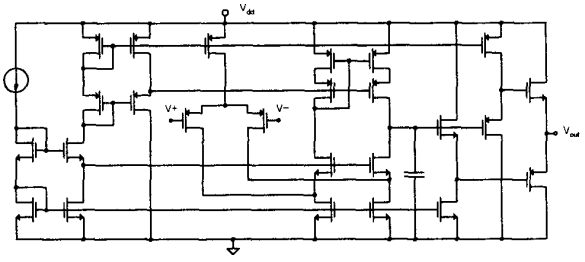


Fig. 9 Error amp

C. Error amp

An operational amplifier must have sufficiently wide bandwidth to cover the high-switching frequency operation of the converter. The unity-gain bandwidth is located at 40 MHz with phase margin of 60°. The open loop dc gain of the error amp is designed to have more than 60 dB.

D. Gate driver

The driver stage is very simple and is essentially a series of cascaded inverters, with each inverter stage being progressively larger to achieve a lower driving impedance. The two gate drivers are implemented with cascaded inverter stages with a tapering factor of 4.

E. EMI suppression circuit

In the discontinuous current mode, there exists a period that both switches are turned off. If both switches are turned off, a resonance occurs at node V_x in Fig. 10 by inductor and parasitic capacitor between drain and source as shown in Fig. 11(a). This causes the electromagnetic interference in noise-sensitive applications such as cellular phones. So we clamped the high-frequency inductor ringing using auxiliary switch on both sides of the inductor as shown in Fig. 10. If both main NMOS and PMOS switches are turned off, the auxiliary switch located on both sides of inductor is turned on. So the ringing is suppressed. The unclamped and clamped waveform of inductor ringing is shown in Fig. 11.

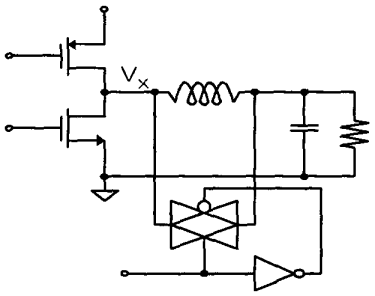
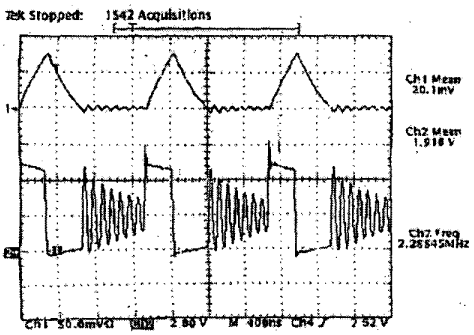
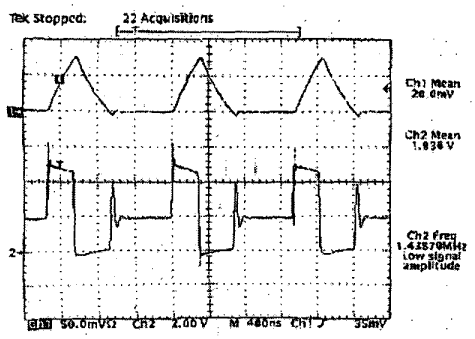


Fig. 10 Inductor ringing clamping circuit

It is very important that the auxiliary switch should be turned on after NMOS is turned off and turned off before PMOS is turned on. If these are not met, the output voltage would be connected directly to Vdd or ground, resulting in a large shoot-through current.



(a)



(b)

Fig. 11 Zero current switching and EMI suppression (b) Clamped waveform of inductor ringing

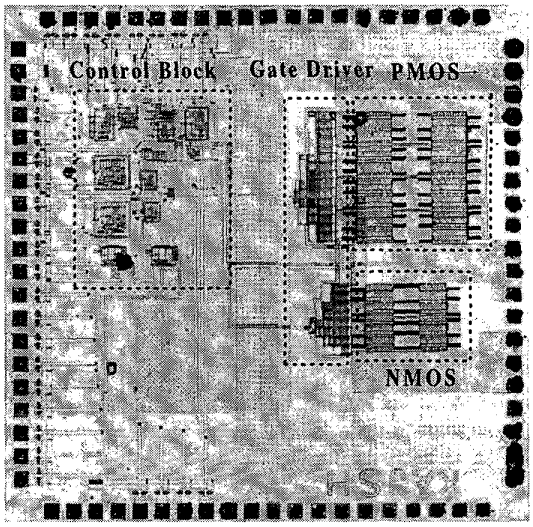


Fig. 12 Photograph of the integrated CMOS DC-DC converter IC

IV. Test results

A prototype IC is shown in Fig. 12 which is fabricated in a 0.6 u CMOS process. The circuit delivers up to 2 W at 3 V

output under the condition of 5 V input. The waveforms of drain voltage of main switch and inductor current at 2 MHz switching frequency are shown in Fig. 13. Fig. 14 shows the measured total efficiency versus output power with varying switching frequencies. This shows that the efficiency is above 78 % at 1 W output power and 2 MHz switching frequency. We can say that the conduction loss is dominant until the switching frequency is up to 2 MHz. The efficiency at 3 MHz switching frequency is a little bit lower than that of 2 MHz because the switching loss is higher than the conduction loss. In other words, the amount of reduction of conduction loss owing to the decrement of the inductor rms current is less than that of the increment of the switching loss. There is little difference in the inductor rms current value between 2 MHz and 3 MHz frequency with 1 uH inductor. Higher conduction loss results in lower efficiency.

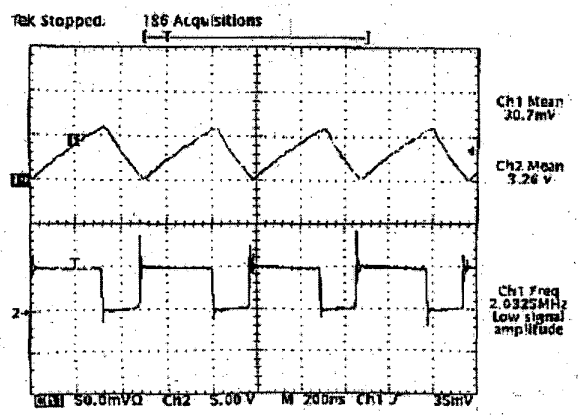


Fig. 13 Inductor current waveform and drain voltage of main switch
V_{in}=5V V_{out}=3V f=2MHz L=1uH R_o=10Ω

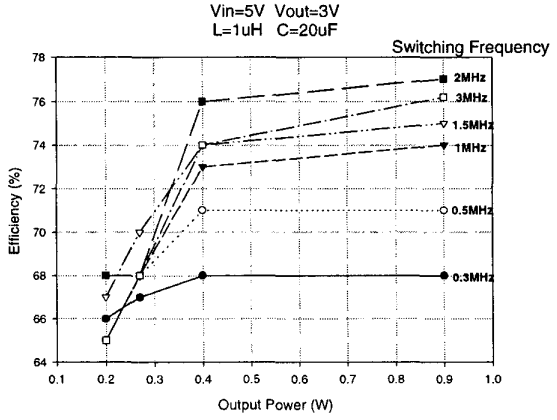


Fig. 14 Efficiency versus output power with varying switching frequency

V. Conclusion

This paper presents an optimum design of DC-DC converter for low voltage, low power and small size inductor. The optimum switching frequency is determined by considering of rms value of inductor current. We found the optimum size of switch through the loss analysis. The control IC is fabricated for a buck converter that is designed to operate at a constant frequency with hard switching PWM converter having synchronous rectifier. From the results, it is thought that the DC-DC converter can be integrated into one chip at low power range (1~2 W) except the inductor, and hard switching PWM converter is a good choice rather than a resonant converter for low voltage, low power applications.

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