DSP BASED SPACE VECTOR PWM FOR THREE-LEVEL INVERTER WITH DC-LINK VOLTAGE BALANCING

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ABSTRACT: This paper describes a new PWM method for three-level inverter considering DC-link capacitor balancing problem. Each voltage vector on space vector plane is classified in relation to charging discharging action of DC capacitors and a new modulation method is suggested based on the voltage vector selection principle. The algorithm is implemented on Motorola DSP 56000 and tested with 7.5KVA prototype three-level transistor inverter. The effectiveness of suggested PWM method is verified by the experimental results.

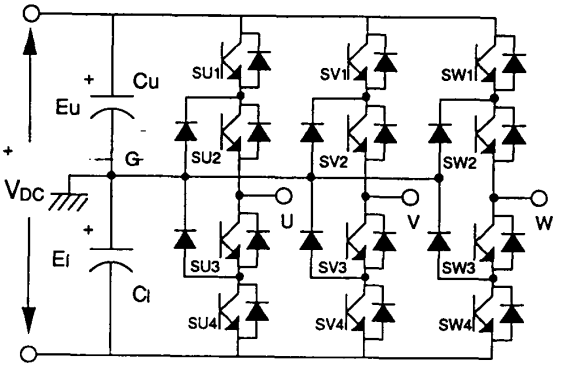


Fig. 1 Circuit diagram of three-level inverter

I. INTRODUCTION

Nowadays three-level PWM inverter is believed to be promising in high power/ high voltage AC drives above 4,500 V where there is no solution with single switching element. It is well known that the three-level inverter has advantages such that the blocking voltage of each switch is clamped to the half of DC-link voltage and the output voltage and current waveform contain low harmonics compared to conventional two-level inverter for the same switching frequency. Various PWM techniques for the three-level inverter have been studied[2-6] since Akira Nabe proposed the topology by the name of NPC inverter in 1981[1]. Such techniques which are regarded as an extension of the conventional two-level PWM include dipole modulation, harmonics elimination, space vector PWM and so forth. So far, however, little attention has been paid to DC-link capacitor voltage balancing problem which is inherent in the three-level inverter topology. It is required that the two DC-link capacitor voltages(E_u and E_l in Fig. 1) should be maintained balanced condition to guarantee the true three-level operation throughout the whole output voltage range. If it is violated, the output contains even order harmonics including second order which is fatal in AC drives.

In the following sections, DC-link voltage balancing problem is discussed in detail and two kinds of solutions are suggested: one is closed loop method with sensing circuitry the other is open loop method without any sensing. Especially the open loop method is described in detail and a new modulation technique is suggested for it. The new PWM is based on the synchronous space vector PWM with constant carrier frequency that controls the time integral of output vol-

tage to have circular trajectory in d-q plane and whereby neutral point can be controlled to maintain unbiased to upper or lower DC-link rail. Various experiments are also given to verify effectiveness of suggested PWM method.

II. DC-link capacitor voltage balancing problem

Fig. 1 shows the circuit diagram of three-level inverter and Fig. 2 shows equivalent simplified three-level inverter for respective two different switch states considering load connections to describe the voltage balancing problem of the capacitor. The two capacitors of Fig. 1 are replaced by a single one in Fig. 2 by adding together. The figure represents that the motor load is connected across E_u and E_l, respectively. The two case is completely equivalent at the load side providing that E_u is equal to E_l. As it is shown, the neutral terminal is not of a rigid voltage source but of a capacitor. Thus it is not guaranteed that E_u and E_l maintain equal because E_l goes larger in case (a) and goes smaller in case (b) according to charging discharging action. Either of the two states can't sustain even for one or two periods of the inverter frequency before the potential of the central terminal reaches to that of upper or lower rail by charging or discharging. If this situation happens, it is impossible to operate the inverter any longer. Furthermore, if the capacitor which has the voltage rating less than V_{DC} is adapted, all would burn out. If the two states are continued for T_u and T_l, respectively in average, then E_u and E_l approaches $T_u \cdot V_{DC}/(T_u + T_l)$ and $T_l \cdot V_{DC}/(T_u + T_l)$, respectively, with some time constant which is a function of

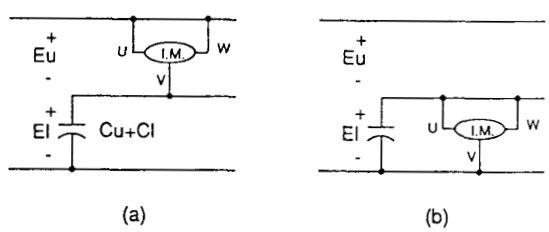


Fig. 2 Load connections of (a) charging, (b) discharging vector

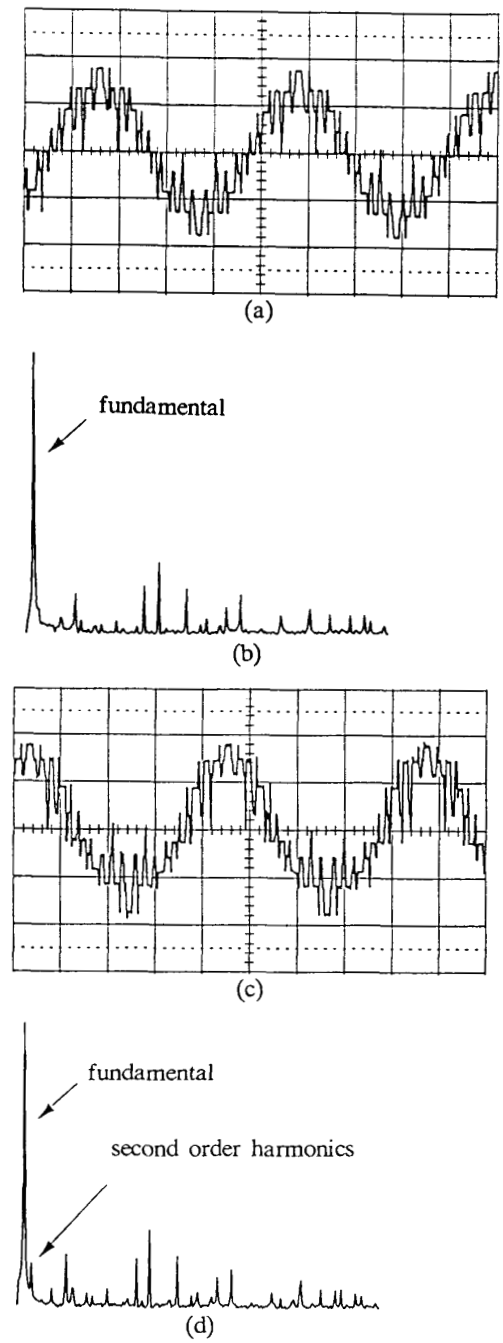


Fig. 3 Phase voltage and spectrum
(a)(b) under balanced condition
(c)(d) under unbalanced condition ($E_u/E_l = 1.7$)

capacity of DC capacitor and the load. So the capacitor voltage balancing problem is closely related to choice of vector and its duration. The capacitor balancing problem can also be regarded as load balancing problem.

Fig. 3(a) and (b) show the phase voltage waveform and its spectrum for balanced condition while (c) and (d) shows the case for unbalanced condition when $E_u/E_l = 1.7$. The output voltage waveform of the unbalanced case is seriously distorted compared to the balanced case. As shown in the frequency spectrum, the second harmonic does not exist in the balanced condition whereas it appears in the unbalanced condition. The second harmonic which is proportional to unbalanced voltage cause serious problems in AC drives such as current harmonics, torque pulsation and power losses.

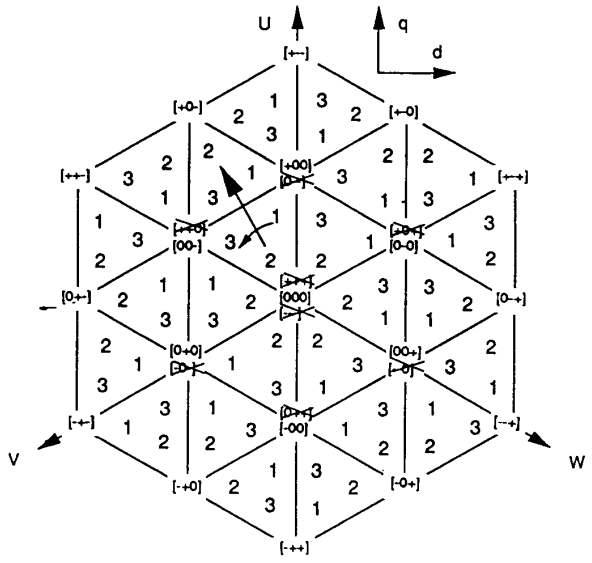


Fig. 4 Space vectors of three-level inverter

Table 1 Classification of space vectors

ZV		[---], [000], [+++]
SV	USV	[+00], [++0], [0+0], [0++], [00+], [+0+]
	LSV	[0--], [00-], [-0-], [-00], [--0], [0-0]
MV		[+0-], [0+-], [-+0], [-0+], [0-+], [+-0]
LV		[+--], [++-], [-+-], [-++], [--+], [+-+]

III. Space vector of three-level inverter

Space vector notation is very useful tool to understand capacitor voltage balancing problem because vector notation shows load connection directly. The output of three-level inverter has 27 different vectors as shown Fig. 4. We identify the voltage vectors such as [+0+], [−00] and so on. For example, in case of [+0−], SU1, SU2, SV2, SV3, SW3, and SW4 in Fig. 1 are in ON and the others in OFF states. Thus the output terminal U, V, and W has the potential of $+V_{DC}/2$, 0, and $-V_{DC}/2$, respectively, and the corresponding load connection is shown in Fig. 5(b). The voltage vector can be classified into some categories according to its magnitude. Such categories are zero vector(ZV), small vector(SV), medium vector(MV), and large vector (LV) as listed in Table 1. The SV group is subdivided into upper small vector(USV) and lower small vector(LSV) again. Each group has its own role concerning charging or discharging action. The ZV and the LSV has no effect on charging discharging because the load is not connected between neutral point and the upper/lower rail. The MV is somewhat effective on improving voltage unbalance. The SV is the most effective for the balancing because USV has charging action and LSV has discharging action. Thus special care must be paid in the selection between USV and LSV. We can control the neutral point voltage using SV group either by closed loop or by open loop control.

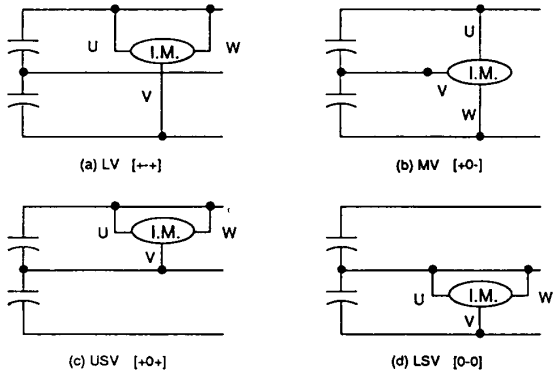


Fig. 5 Representative vectors and their load connections

i) Neutral point control by closed loop

Fig. 6 roughly shows closed loop control method with voltage sensor together with PWM algorithm. The **vector classifier** judges whether the present vector is SV and whether neutral point potential is in acceptable range. If the neutral point potential is close to that of the upper rail beyond boundary, the PWM controller decrease the USV duration by ΔT and increase LSV duration by ΔT. In this case it is necessary to compromise between dynamics and stability in considering ΔT.

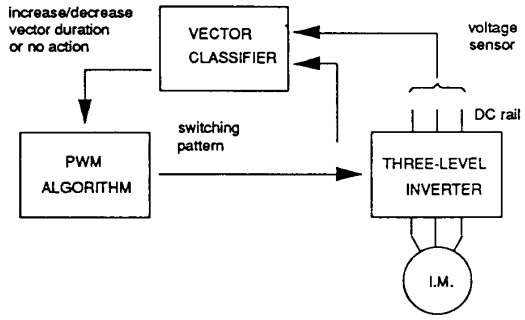


Fig. 6 Neutral point control by closed loop

ii) Neutral point control by open loop

Although we do not adapt closed loop control, voltage balancing can be achieved if special PWM technique is employed to select USV and LSV evenly. The PWM method must be synchronous one such as dipole modulation, harmonics elimination or synchronous space vector PWM (alias star modulation) because the load should be distributed evenly without feedback. In general, synchronous space vector PWM is preferred to others because relatively good waveforms can be obtained in spite of its simple configuration. If PWM algorithm is implemented on 16bit micro-processor, the calculation error can be under 10^{-5}. The error is mainly due to driver and device mismatch. However it is small enough in practice and is not accumulated. Thus the total unbalancing is not so large that the system could cause no serious problems.

IV. PROPOSED PWM TECHNIQUES

Fig.7 shows the different switch state in the first quadrant of d-q plane. Here, V_n is the sampled value of the reference voltage vector rotating with angular speed ω at certain instant. If V_n falls into the triangle established by the straight lines that interconnect the voltage vectors V_1, V_2, and V_3, the duration of each vector can be calculated by the following relations.

$$V_n \cdot T = V_1 \cdot t_1 + V_2 \cdot t_2 + V_3 \cdot t_3 \quad (1)$$

$$T = t_1 + t_2 + t_3 \quad (2)$$

where T is sampling time of reference voltage vector.

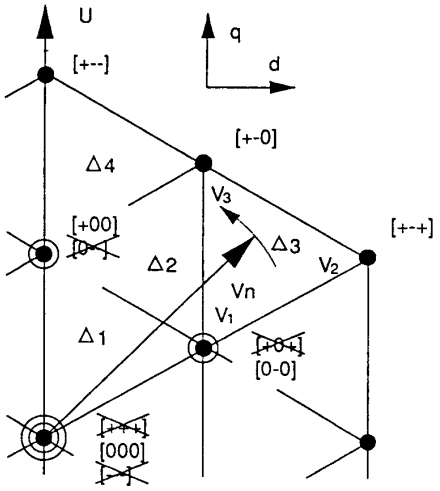


Fig. 7 Selection of vectors and their sequence

This is well-known technique in space vector PWM but the selection of vector and their sequence is the key in controlling the neutral point. The three region $\Delta 1$, $\Delta 2$ and $\Delta 3$ in Fig. 7 actually represent all regions of Fig. 4 because the control method is similar in the other regions. The selection methods of vectors and its sequences are explained for each region as in the following.

i) Region Δ1

In this region, the vector sequence is given in the order LSV[0−0] - USV[+00] - ZV[000]. voltage balancing is satisfied because LSV and USV are selected alternatively for the interval time T.

ii) Region Δ2

The vector sequence is given LSV[0−0] - MV[+−0] - USV[+00] in this region. Because LSV and USV are selected alternatively during time T, voltage balancing is satisfied. Furthermore MV influences in such a way to improve the voltage unbalance.

iii) Region Δ3

The vector sequence is given LSV[0−0] - MV[+0−] - LV[+−+]. Although only LSV is used, there is little problem in voltage balancing, because V_n will move into the region Δ4 in T or in 2T.

In this manner we chose the voltage vectors used in the PWM and determined their sequence satisfying in capacitor voltage balancing as in Fig. 3.

VI. Experiments

The implementation of the proposed PWM method is established on 7.5 KVA prototype transistor 3-level inverter controlled by Motorola DSP 56000. The PWM control algorithm is constructed with assembly language and operates in real time. The computation takes about 230 μsec which is enough to operate the inverter in real time because the T is larger than 4 msec. In this case the switching frequency for each device corresponds about 500Hz which is usual value in several MVA GTO inverter. The experimental results are shown for two different magnitudes of the output as represented in Fig. 8 and 9. The symmetry of the each voltage in Fig.8 and Fig.9 shows that DC-link capacitor voltage balancing is satisfied fairly good. Fig. 10 shows harmonic current factor (HCF) for various q by computer analysis where q is the number of division per cycle of the inverter frequency or

$$q = \frac{2\pi}{T\omega} \quad (3)$$

The T is sampling time of reference voltage vector and ω is the angular speed of the inverter output voltage.

The bold line represents selected PWM pattern to suppress HCF under 2.5 %.

V. CONCLUSION

This paper pointed out the seriousness of the voltage unbalancing problem inherently resides in the three-level topology. All the space vectors of three-level inverter are classified concerning voltage balancing. Two solutions to it are suggested, one is closed loop and the other open loop control. Especially, a new PWM technique is suggested based on space vector as a method of the open loop control. The experiment showed that the suggested PWM techniques is suitable to high power GTO three-level inverter satisfying capacitor voltage balancing.

REFERENCES

[1]A. Nabae, I. Takahashi and H. Akagi, "*A New Neutral Point Clamped PWM Inverter*", IEEE Trans. on IA, Vol. IA-17, No. 5, pp. 518-523, Sept/Oct 1981

[2]B. Velaerts et al., "*A Novel Approach to the Generation and Optimization of Three-Level PWM Wave Forms*", PESC '88 RECORD, pp. 1255-1262, Apr 1988

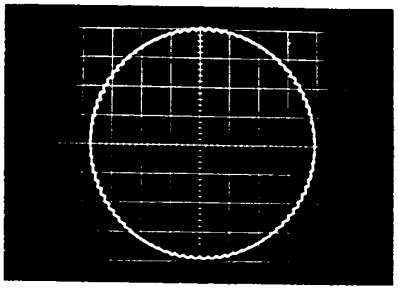
[3]G. Carrara et al. "*A New Multi-level PWM Method: A Theoretical Analysis*", RESC '90 RECORD, pp. 363-371, 1990

[4]P. Enjet, R. Jakkli, "*Optimal Power Control Strategies for Neutral Point Clamped (NPC) Inverter Topology*", IEEE IAS, pp. 924-930, 1989

[5]J. Holtz, L. Springob, "*Reduced Harmonic PWM Controlled Line-side Converter for Electric Drives*", IEEE IAS, pp. 959-964, 1990

[6]P. M. Bhagwat, V. R. Stefanovic, "*Generalized Structure of a Multilevel PWM Inverter*", IEEE Trans. on IA, Vol. IA-19, No. 6, pp. 1057-1096, Nov/Dec 1983

[7]*DSP 56000 /DSP 56001 Digital Signal Processor User's manual*, Motorola



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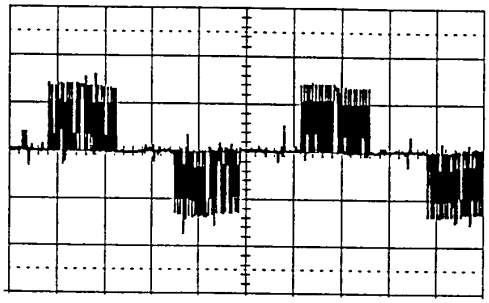

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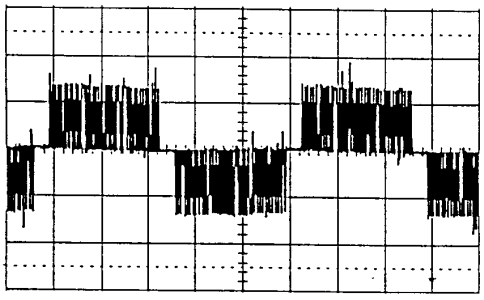

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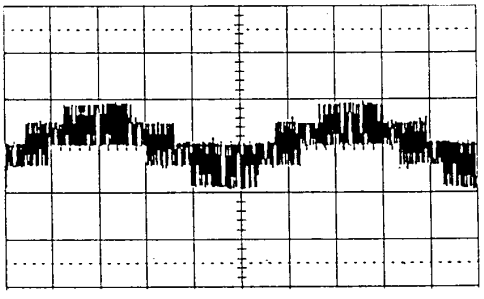

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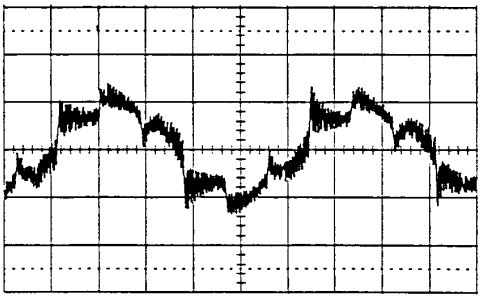

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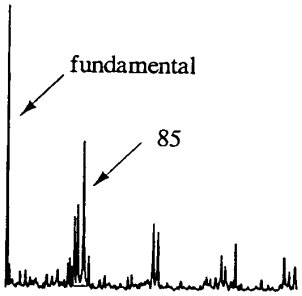
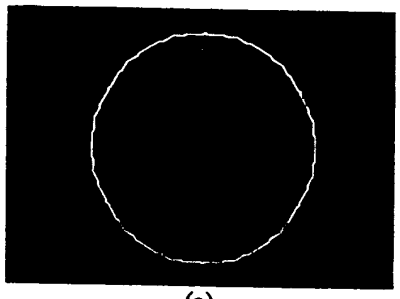


(f)

Fig. 8 When f_{inv} = 20Hz, m(modulation index) = 0.3 and q = 84

(a) trajectory of time integral of output voltage
(b) pole voltage (100V, 10msec/div)
(c) line-line voltage (100V, 10msec/div)
(d) phase voltage (100V, 10msec/div)
(e) line current (10A, 10msec/div)
(f) spectrum



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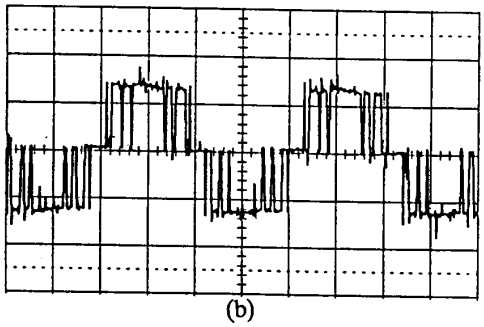

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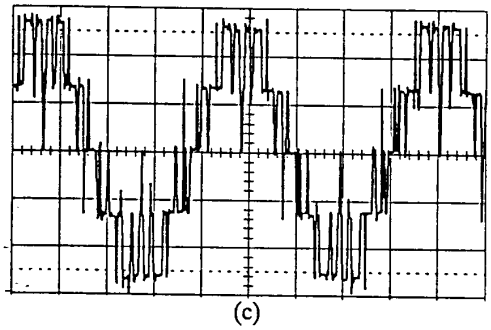

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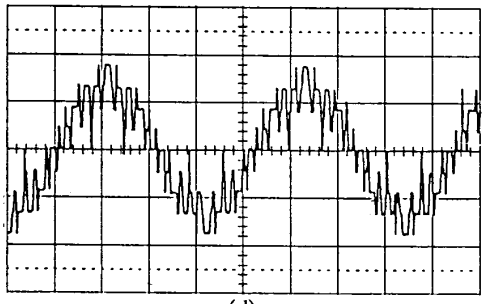

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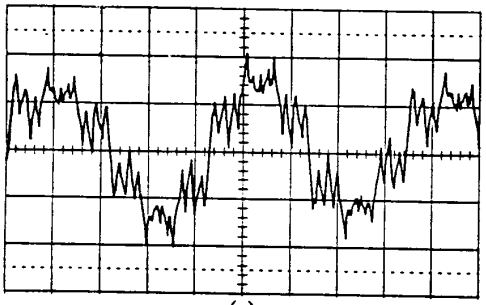

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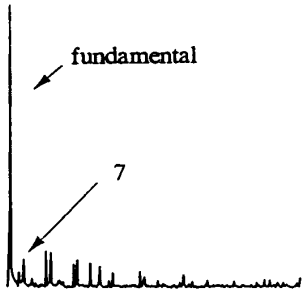

(f)

Fig. 9 When f_{inv} = 50Hz, m = 0.8 and q = 24
(a) trajectory of time integral of output voltage
(b) pole voltage (100V, 20msec/div)
(c) line-line voltage (100V, 20msec/div)
(d) phase voltage (100V, 20msec/div)
(e) line current (10A, 20msec/div)
(f) spectrum

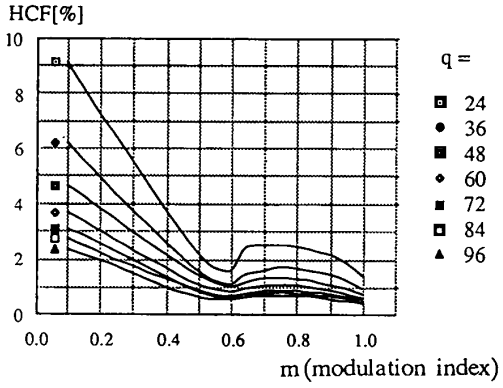

Fig. 10 HCF for various q