A Single-Inductor Switching DC–DC Converter With Five Outputs and Ordered Power-Distributive Control

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***Abstract*—An integrated five-output single-inductor multiple-output dc-dc converter with ordered power-distributive control (OPDC) in a 0.5 μm Bi-CMOS process is presented. The converter has four main positive boost outputs programmable from +5 V to +12 V and one dependent negative output ranged from −12 V to −5 V. A maximum efficiency of 80.8% is achieved at a total output power of 450 mW, with a switching frequency of 700 kHz. The performance of the converter as a commercial product is successfully verified with a new control method and proposed circuits, including a full-waveform inductor-current sensing circuit, a variation-free frequency generator, and an in-rush-current-free soft-start method. With simplicity, flexibility, and reliability, the design enables shorter time-to-market in future extensions with more outputs and different operation requirements.**

***Index Terms*—Ordered power-distributive control (OPDC), single-inductor multiple-output (SIMO) converter, soft-start, zero-current sensor.**

I. Introduction

A DC–DC converter has been an indispensable part of many power-management systems. Its importance is gaining more and more attention when the trend of voltage scaling is not only limited to digital circuits [1], [2], but also spreading to other applications, one of which is the emerging active-matrix OLED (AM-OLED) display panels of upcoming cellular phones and other portable devices [3]. As all designers put effort into size reduction, a converter with different output voltages cannot stay out of that trend, forcing designers to find a method to shrink the size in both on-chip and off-chip implementations. Of all of the approaches, single-inductor multiple-output (SIMO) converters come to prevail. SIMO converters can support more than one output while requiring only one off-chip inductor, promising many appealing advantages, in particular the reduction of bulky power devices, including inductors, capacitors, and control ICs. The cost of mass production, hence, is remarkably reduced, and SIMO therefore shows up as the most suitable and cost-effective solution in the future development of dc–dc converters, attracting many producers with various applications in portable devices. However, it is still a big challenge to dc–dc converter designers to find the best method of the implementation of this converter type.

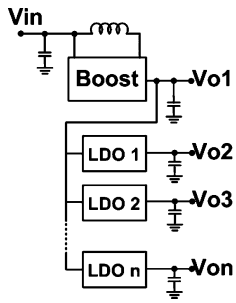

Fig. 1. One boost and $n-1$ LDOs.

The topology that has been frequently used by many designers and manufacturers is shown in Fig. 1. With this topology to make n outputs, one boost converter is used together with $n-1$ low drop-out (LDO) converters [4]. Although incorporates advantages of the LDO design, which are simplicity, low output ripple, and short time-to-market, the topology is not appropriate for future development owing to the main disadvantages of LDOs, including low efficiency and area consumption by serial power switches.

Most recently, a switching single-inductor dual-output (SIDO) boost converter has been reported in [5] and [6]. The SIDO converter, shown in Fig. 2, works in pseudocontinuous or discontinuous conduction mode (PCCM/DCM) with a freewheel period, trying to handle large load currents and eliminate cross-regulation. However, PCCM operation unnecessarily dissipates energy in the resistance of the inductor and freewheel-switch because of the nonzero inductor current during the freewheel time, illustrated in Fig. 3, which reduces the overall efficiency. More disadvantageously, using separate proportional-integral (P-I) compensators and output-switch current sensors for the outputs with time-multiplexing control causes unwanted complexity and increases the chip area. Therefore, PCCM/DCM is not a good solution, especially when the number of outputs increases.

The drawbacks of these conventional approaches, therefore, urge the development of a new SIMO converter, which can reduce area consumption while maintaining good regulations for

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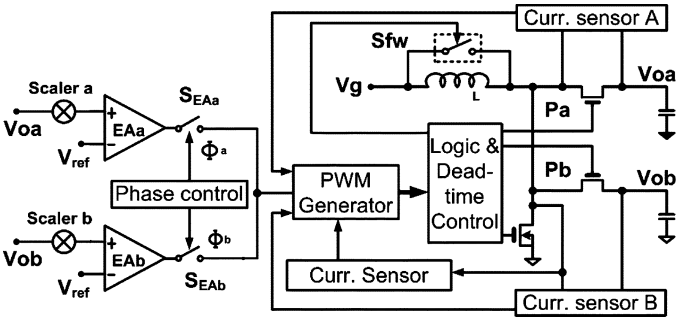

Fig. 2. Architecture of the PCCM SIDO dc–dc converter.

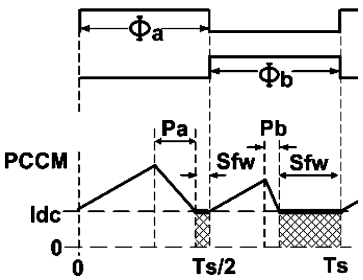

Fig. 3. Loss in the PCCM SIDO dc–dc converter.

outputs. The converter should also work properly in DCM and CCM. In addition, it is desirable to have a new control method of simplicity and flexibility in implementation that can be applied to different converter types of multiple-output topologies for different application requirements.

In this paper, we present an integrated SIMO dc–dc converter, fabricated in a 0.5 μm Bi-CMOS technology. Employing a novel ordered power-distributive control (OPDC), which will be introduced in Section II, the SIMO converter can regulate four main programmable positive boost outputs and one dependent negative output developed by a charge-pump. Important proposed circuits and techniques, including inductor-current sensor, frequency generator, soft-start method, dead-time control, and cross-regulation, are discussed and verified in Section III. In Section IV, experimental results will be provided to prove the OPDC and the performance of the converter. Section V will present the future extensions of the design, and conclusions will be made in Section VI.

II. SIMO Converter With Five Outputs

A. Architecture and OPDC for Boost Outputs

The architecture of the five-output SIMO converter suggested in this paper is shown in Fig. 4. The OPDC arranges four boost outputs Vo1, Vo2, Vo3, and Vo4 in descending order of priority to, one by one, share the charge from the inductor in every switching cycle or, more correctly, every power distribution cycle. The first three output voltages Vo1, Vo2, and Vo3 are controlled using comparators and are thus called comparator-controlled outputs, while the last-ordered output Vo4 is P-I controlled with an error amplifier that is responsible

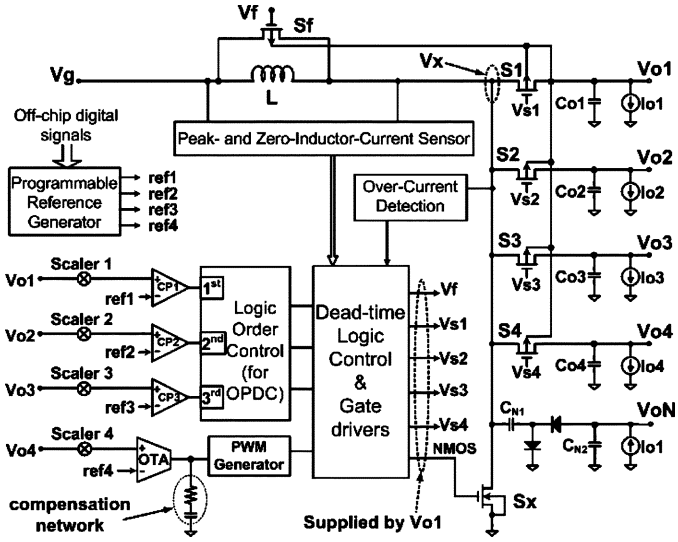

Fig. 4. Architecture of the proposed OPDC SIMO dc–dc converter.

for the converter's total charge. Therefore, in this OPDC, all of the errors of the preceding comparator-controlled outputs are transferred and accumulated to the last, which is the only one requiring a compensation network in the feedback loop.

The operating principle of OPDC can best be explained using the timing diagram in Fig. 5, where the high part of the signal Si represents the on-state of the switch Si. During the time denoted DT, the inductor current I_L ramps up at a rate of Vg/L. The duty-cycle D is determined by peak-current mode control. The four output switches S1, S2, S3, S4 and the freewheel switch Sf (which is active in DCM), in order, turn on during the time $D'T$, where $D' + D = 1$. During $D'T$, I_L ramps down with different slopes depending on the output voltages and switching sequence. S1 is on at the beginning of $D'T$, making I_L ramp down at a rate of $-(Vo1-Vg)/L$ and flow into Vo1. As soon as comparator CP1 detects that Vo1 is larger than its target voltage, D_1T expires, S1 is turned off, and S2 is turned on. The same sequence then repeats as the inductor current ramps down with a slope equal to $-(\text{Vo2} - Vg)/L$ during D_2T, then $-(\text{Vo3} - Vg)/L$ during D_3T, while Vo2 and then Vo3, in turn, get the second and third portions of charge, respectively. Switch S4 is the last output switch to turn on, and the last portion of charge flows into Vo4 while the slope of the inductor current is $-(\text{Vo4}-Vg)/L$ during D_4T. When the inductor current is zero, D_4T expires, S4 is off, and Sf turns on during D_fT to short the two ends of the inductor and suppress possible ringing at Vx until the end of the switching cycle. In this mode of operation, the converter is said to work in DCM. Since I_L does not decrease to zero in CCM operation, there is no freewheel period, which is indicated by D_fT, as illustrated by $I_L(1)$. Dependent on the last portion of charge, the loop containing Vo4 and the total current loop are compensated and controlled by the well-known peak-current control method. These control loops guarantee that the last portion of charge is enough to keep channel 4 at its target voltage, while good voltage regulation is already maintained in the preceding outputs Vo1, Vo2, and Vo3.

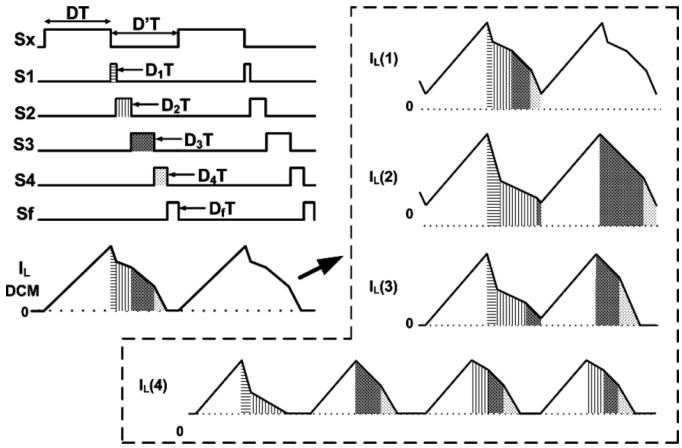

Fig. 5. Timing diagram of the OPDC SIMO dc–dc converter.

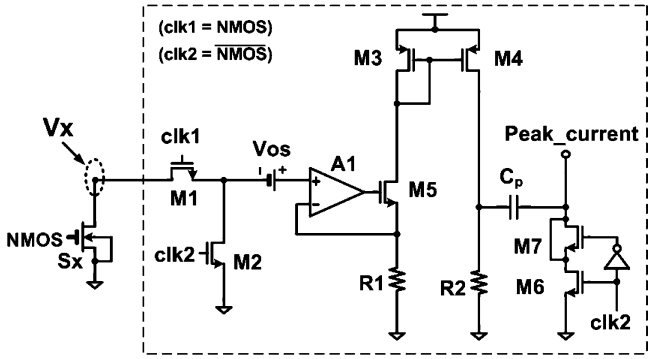

Fig. 6. Peak-inductor-current sensor.

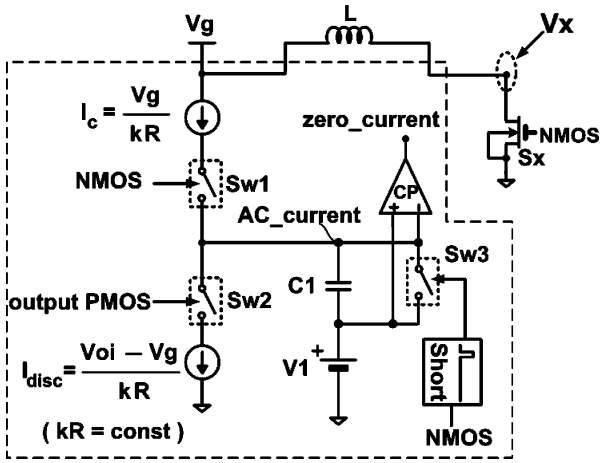

Fig. 7. Zero-inductor-current sensor.

B. Dependent Negative Output With a Charge-Pump

The charge-pump circuit included in Fig. 4 with two Schottky diodes and two capacitors is connected to the node Vx and makes a negative output from the voltage changes at Vx. The flying capacitor C_{N1} gets charge when the positive outputs get energy and Vx goes high and then transfers negative charge to the output capacitor C_{N2} when the switch Sx is on and Vx goes low. The negative output voltage, therefore, depends on the voltage drop over the Schottky diodes V_D and the highest positive output voltage, which is Vo1 in this design, $|VoN| =$ Vo1 $- 2V_D$. Since good regulation is not necessary in the negative output, feedback control is not added, and C_{N1} is chosen sufficiently small to have no effect on the total operation and dead-time control.

C. OPDC and Switching Flexibility

The simplicity and flexibility of the OPDC, with three voltage comparators for the three preceding outputs and one P-I control for the last output, prove that the converter can have different switching patterns in regulating the outputs, as shown in Fig. 5. $I_L(2)$ shows the case of CCM operation where three or two output switches are orderly and alternately on in one switching cycle. Operation at the boundary of CCM and DCM and one in DCM are illustrated with $I_L(3)$ and $I_L(4)$, respectively. It is worth noting that OPDC allows that the turn-on frequency and the duty D_i of an output switch do not always have to be constant, provided that the output voltage be regulated. However, the principle of OPDC is always sustained in that the total charge from the inductor is, one by one, distributed to four boost outputs Vo1, Vo2, Vo3, and Vo4 in descending order of priority in every power distribution cycle. One power distribution cycle is said to end when the last output Vo4 gets its portion of charge.

III. Circuits and Implementations

The converter has important blocks, as shown in Fig. 4. The reference voltages are programmed from off-chip digital signals. The function of the logic order control block is to pass the signals from comparators in order of priority to make OPDC. Since Vo1 is always set to the highest voltage, it is used to bias all of the bodies of pMOS power transistors and supply all gate drivers for power transistors.

A. Full-Waveform Inductor–Current Sensor

The implementation of current-mode control schemes described in [7] and [8] requires sensing of the complete waveforms of inductor current, including the peak- and zero-current information of the inductor–current waveform. The design challenge arising from such inductor current sensing is not completely overcome, but usually overlooked, especially in dc–dc step-up converters. Some published solutions [9], [10] only focus on sensing inductor current in nMOS turn-on time, while current sensing in pMOS turn-on time is usually omitted by using only CCM operation. However, DCM operation is often required for light-load outputs with maintained low-output voltage ripple; otherwise, inductor values need to be big.

A current sensor, which can sense complete waveforms of inductor current, is proposed in this paper with two partial sensors to achieve both the peak- and the zero-current information.

1) Peak-Current Sensor: The circuit of an accurate peak-inductor-current sensor is illustrated in Fig. 6. The circuit is designed to sense the inductor current waveform in the charge period through the drain–source voltage over the on-resistance of the main switch Sx of the converter when it is on. The current information in the form of the drain–source voltage is transferred

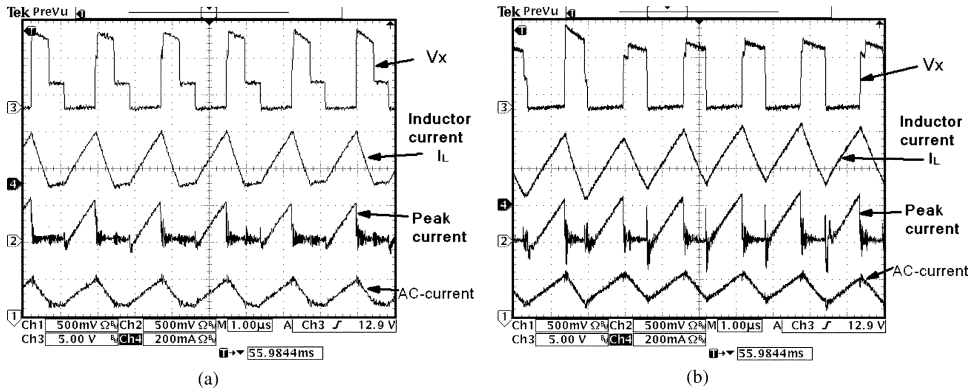

Fig. 8. Measured waveforms of current sensor (a) in DCM and (b) in CCM.

through a V–I converter composed of amplifier A1, transistor M5, and resistor R1, then mirrored via the 1:1 current mirror M3-M4, and, finally, appears at node Peak_current in the form of voltage over R2. The gain of this sensor, therefore, is determined by the ratio R2/R1. A small positive offset Vos, which is given at the positive input of A1, is saved and then cancelled at output by capacitor C_p and clk2. The intentional positive offset Vos and offset cancellation technique are proposed in this circuit to eliminate any possible offset at A1 inputs and improve the performance. M7 is inserted as shown in this circuit to remove the charge injection errors that can be seen at the output when M6 is turned off.

2) Zero-Current Sensor: Zero-inductor-current sensing is necessary to enable DCM operation when the converter supplies light loads. In conventional techniques [5], [6], detecting zero-inductor current through the on-resistance of output pMOS switches causes unnecessary complexity and area consumption, especially when the number of outputs of SIMO step-up dc-dc converters and output voltages are increased. Moreover, in this OPDC, the switching flexibility of output power switches requires a new zero-inductor-current sensor that can work with any switching sequence and different programmable output voltages.

A novel precise zero-inductor-current sensor is shown in Fig. 7. The core idea of this circuit lies in the fact that, in a dc–dc converter, inductor current waveforms are formed by a fixed inductor value and the voltage differences between the two terminals of the inductor. The AC_current signal is thus correlatively generated with a constant kR and the said voltage differences. With this approach, the AC_current signal has the same shape as the real inductor current waveform, thus enabling zero-inductor-current detection. This circuit is also called a current observer, as it precisely detects a zero-inductor current without difficulties in sensing online current through output pMOS switches. More details of this circuit are reported in [11].

3) Experimental Results of the Current Sensor: The experimental results in Fig. 8(a) and (b) show that the proposed circuit of the full current sensor, including peak-current sensor (or nMOS current sensing) and zero-current sensor (through AC-current signal), works correctly and as designed. The circuit of the full-waveform current sensor can be applied partially or fully in different converters with its simplicity and reliability.

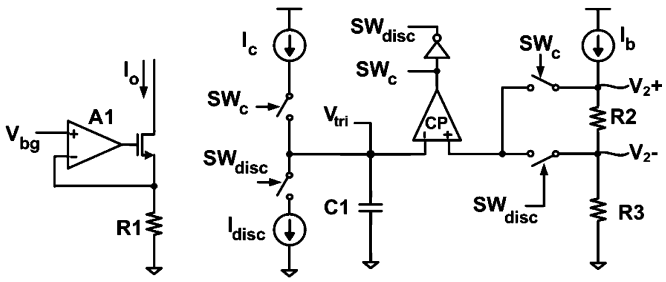

Fig. 9. Frequency generator.

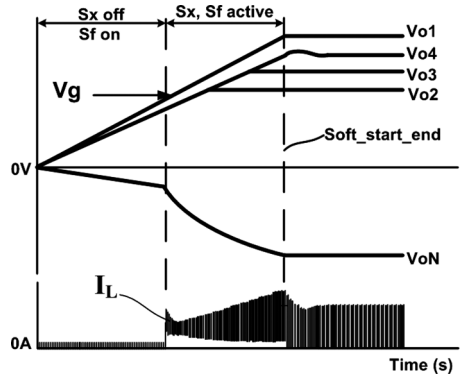

Fig. 10. In-rush-free soft-start.

B. Frequency Generator

The circuit in Fig. 9 is one modification from that reported in [12]. The triangular signal at the $V_{\rm tri}$ node is formed by two predetermined slopes and limited within V_2- to V_2+, where $V_2 = I_bR2$. The currents I_b, I_c, and $I_{\rm disc}$ are proportional to the current $I_O = V_{bg}/R1$. The ramp-up and ramp-down slopes of $V_{\rm tri}$ are $I_c/C1$ and $-I_{\rm disc}/C1$. The triangular voltage $V_{\rm tri}$ is arranged to always be chasing the voltage at the positive input of the hysteretic comparator CP, which is switched between V_2+ and V_2- periodically by the output of the comparator. The output of the comparator, in fact, is used to make the main clock and one-shot signal for PWM operation of the converter. The maximum duty cycle of the main nMOS switch Sx, determined by the ratio of I_c and $I_{\rm disc}$, is about 85% in this design. The triangular signal is used to make the slope compensation for peak-current-mode control [7], [8].

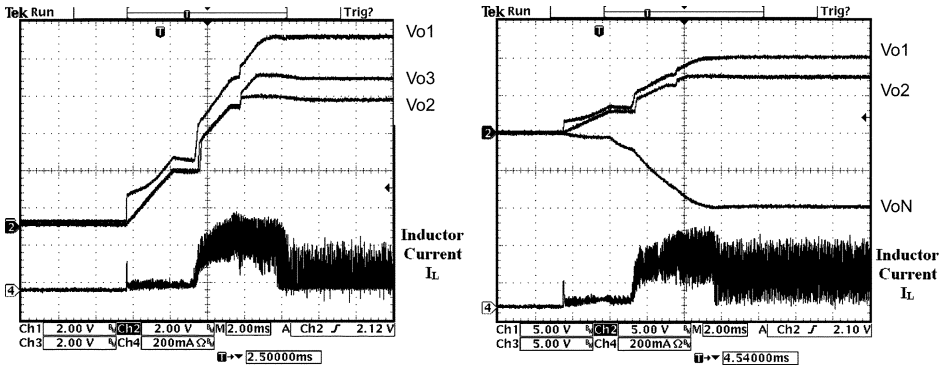

Fig. 11. Experimental waveform of the proposed soft-start method.

C. Soft-Start Method

In synchronous-switching dc–dc converters where outputs often increase from zero, a soft-start method and circuits are mandatory to avoid in-rush current in the inductor that can cause damage to the circuits and components of the converter at start-up. Many designers have been trying to overcome the difficulty in making a proper soft-start by using either step-current limits [13] or a different switching frequency [9]. However, the in-rush current in the inductor is not efficiently eliminated, and outputs are not increased smoothly. A novel soft-start method is introduced in this section, arranging the output voltages to increase from zero to the predetermined level without in-rush current in the inductor.

The soft-start time is divided into two periods, as depicted in Fig. 10.

In the first period, after the converter is enabled, when output voltages increase from zero and are much smaller than the input voltage, the freewheel switch Sf is kept on to short the two ends of the inductor, while the main switch Sx is sustained in the off-state. The converter thus works as a switching LDO without inductor, since, in fact, there is no need for any current charge and transfer to raise output voltages in this period. In this period, output pMOS switches are switched in a predetermined order of OPDC to make outputs increase slowly following ramping reference voltages. This method of switching, when output voltages are still smaller than the input, helps eliminate in-rush currents that often occur in inductors of other dc–dc step-up converters, while the soft-start for output voltage from zero is still maintained.

The second period of the soft-start begins when Vo1 is close to the input voltage. From here, the switch Sx is enabled for switching for the inductor to store energy and boost up output voltages to higher than the input. As the peak current is forcibly controlled to follow a ramp and appropriately limit the peaks of the inductor current, the duty-cycle of Sx is increased slowly in a controlled manner, and output voltages continue to proportionally follow ramping reference voltages until the final required voltages.

Experiment results shown in Fig. 11 prove that the novel two-period soft-start with all the output voltages started from zero. Noticeably, with a switching-LDO-like operation in the first period, there is no in-rush current. This soft-start method with the switching-LDO-like period can be applied to different types of switching dc–dc converters to improve the lifetime of internal circuits, off-chip components, and batteries at the input sources in many portable applications.

D. Folded-Cascode OTA With G_m Control in Light Loads

As can be seen from the topology and operation of the OPDC SIMO converter, the fast response of comparator-controlled outputs allows us to consider the P-I loop as that of a single-output converter described in many well-known publications [7], [8]. The folded-cascode OTA with M1 $\sim$ M14, shown in Fig. 12, is used as the error amplifier of the P-I loop. Three cascode stages at the output are used to increase the total loop gain, thus improving regulations of the converter. The compensation in current-mode control for the output real poles is implemented by a dominant pole at RoCc and zero at RzCc, where Ro is the output resistance of the OTA, and Rz and Cc form the compensation network.

When the output load is changed to a lower value, the output pole, which is formed by a filter capacitor and the load, moves towards the low-frequency range, decreasing the total loop phase margin, because the zero used to compensate this pole is optimized and fixed in normal operation points. To prevent this potential problem, a Gm-control circuit is proposed in this OTA to reduce its gain when the converter works in a light load. By doing this, the unity-gain frequency of the total loop gain is reduced, thus increasing the phase margin and improving the converter stability. The Gm-control circuit composed of bias current sources Ibc1 $\sim$ Ibc3, transistors Mc1 $\sim$ Mc8, and resistors Rc1 $\sim$ Rc5 is also included in Fig. 12. Note that load conditions of the converter can be detected from the output signal of the OTA, which is lower when the converter works at a lighter load and higher at a heavier load. Therefore, the output of the OTA is the input of the Gm-control circuit. As the output load changes to light, detected by Ibc3, R5, and the pair Mc5–Mc6, Vc1 and Vc2 are changed to control Mc1 $\sim$ Mc4, and then the differential current from M1–M2 to the output cascode stage, from that, controlling the Gm of OTA. Rc1, together with Rc2–Rc3 and the ratio between Mc1–Mc2 and Mc3–Mc4, is chosen to determine the linear range of the Gm-control circuit such that it should not affect the OTA gain and the total loop under normal and heavy load operations. Ibc3 and R5 are designed to determine the location of the linear range that makes the Gm-control circuit effective only

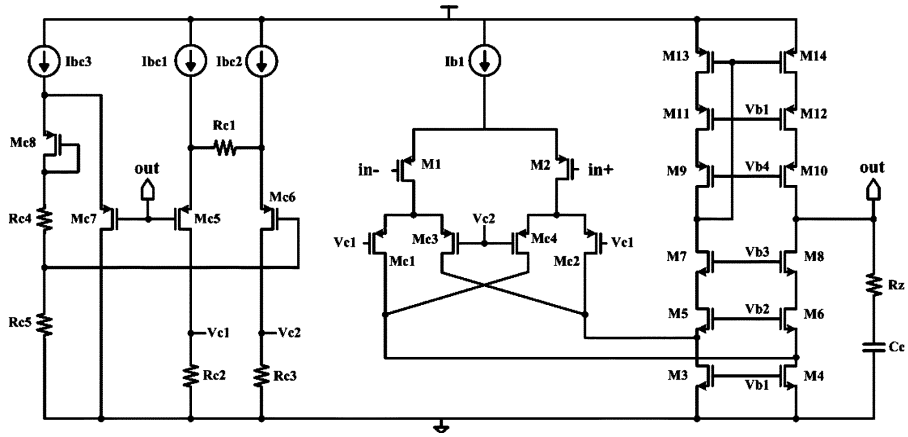

Fig. 12. OTA with G_m control in light loads.

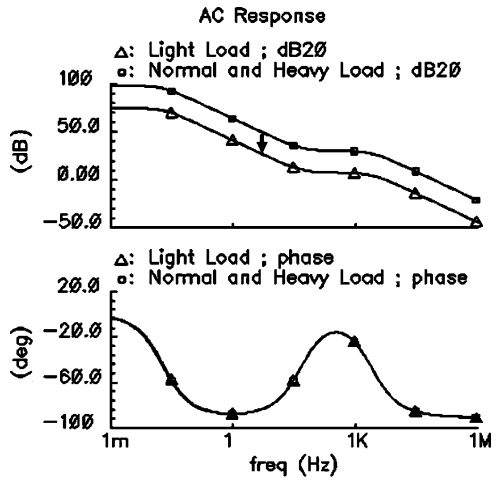

Fig. 13. Simulation results of the Gm-control OTA.

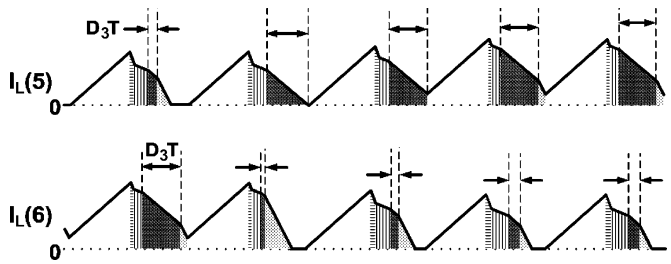

Fig. 14. Load change at Vo3.

in a light load. Rc4 and Mc7–Mc8 are used to guarantee the normal operation of the OTA. Simulation results of the OTA with Gm-control are shown in Fig. 13. In this design, the Gm-control circuit becomes effective when the total output load goes lower than approximately 200 mW. In experiments, the converter is proved to work in a stable fashion in the whole range of output loads.

E. Cross-Regulation Consideration

Voltage comparators, together with only one P-I voltage loop and one current loop in OPDC, help maintain desirable low cross-regulation by fast recovery from load change.

Controlled by a voltage comparator, preceding outputs respond very fast to a load change. Inductor current waveforms $I_L(5)$ and $I_L(6)$ in Fig. 14 are used as examples for load changes in Vo3, which are seen similar to those in Vo1 and Vo2. In $I_L(5)$, the load suddenly changes to a heavier load, making Vo3 drop below the predetermined voltage. Detecting that by the relative comparator, OPDC will allow S3 to occupy the rest of the discharge period after S1 and S2 in the next switching cycles until Vo3 returns to its required voltage. As Vo4 receives no charge in those cycles, the P-I loop understands that more charge is needed, thus increasing the duty D of Sx or, other words, the current charge in the inductor. At the same time, the duties D_1 and D_2 are spontaneously reduced by the comparators CP1 and CP2 to make sure Vo1 and Vo2 stay at their level. The opposite situation is shown with $I_L(6)$. As the load is cut down from Vo3, the duty D_3 is reduced abruptly by the comparator CP3 to keep Vo3 at the predetermined level, leaving the residual charge to Vo4. Vo4 will soon be stabilized back to its level because of the P-I and the total current loops. In case of any load change in Vo4, it is considered to be single output converter, because OPDC makes preceding outputs act very fast with voltage comparators.

Experimental results, illustrated in Fig. 15(a) and (b) prove the low cross-regulation characteristic of OPDC.

F. Dead-Time Consideration

As synchronous rectification is applied for high efficiency and proper output voltage control, dead time should be managed in the nanosecond scale to guarantee appropriate nonoverlap between on-states of the power switches during switching transients. In this design, since each power switch occupies a certain time slot in a switching cycle, dead time between different pairs of switches is chosen differently, considering overall operations and zero-voltage- or zero-current-switching (ZVS or ZCS) to reduce switching loss. After Sx is off, an adequate dead time is given that is enough for the voltage at node Vx to rise close to the output voltage before the relative output pMOS switch is on in consideration of ZVS and output glitches. However, dead time between output pMOS switches can be small such that two adjacent switches can be slightly on together at transient, making a smooth voltage transition at Vx, while still suppressing glitches

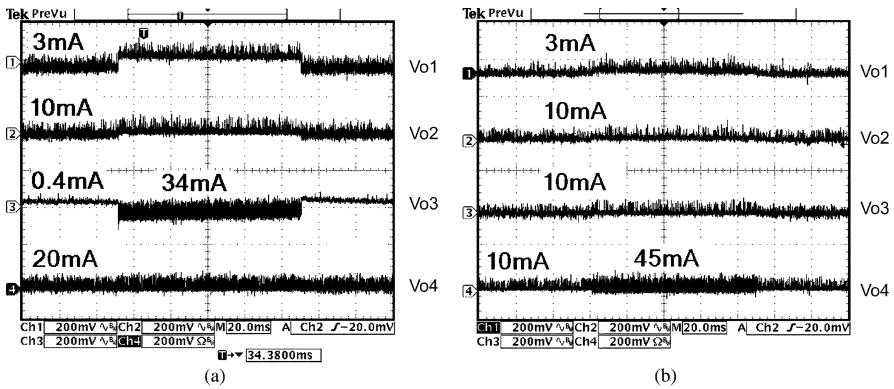

Fig. 15. Measured load change (a) at comparator-controlled Vo3 and (b) at P-I controlled Vo4.

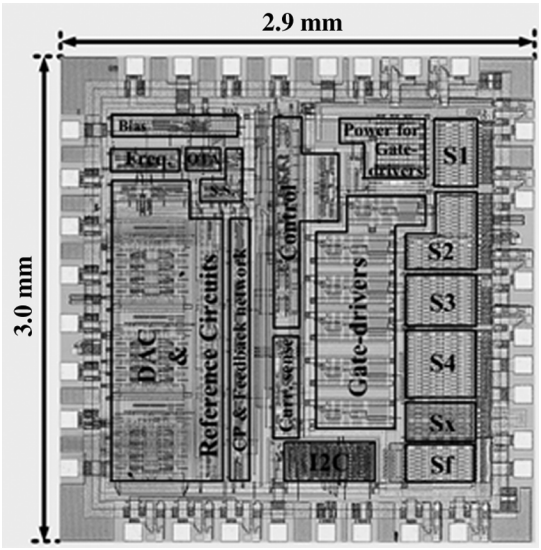

Fig. 16. Die photograph.

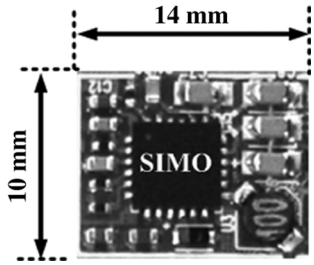

Fig. 17. Implementation on FPCB.

and noise interactions between the two channels. The dead-time consideration is also given before freewheel switch Sf is on to achieve ZCS.

IV. Experimental Results

The converter is implemented in an 8.7 mm^2 die area using a 0.5 μm 1P3M BiCMOS process. The die photograph is shown in Fig. 16, and its implementation photograph on flexible printed circuit board (FPCB) is given in Fig. 17.

Fig. 18(a)–(c) shows experimental results of the converter working in DCM, at the boundary of DCM and CCM, and in CCM, respectively. In these figures, ac-coupling output voltages, together with the inductor current and the waveforms at Vx, verify the ordered switching actions of OPDC and prove the reliability of this novel control method of fast comparator-controlled loops and only one P-I loop. Note that, in Fig. 18(b), Vo2 is set at a lower voltage (5 V) to see clear slope changes in the inductor current waveform at the boundary of CCM and DCM.

TABLE I
Summary of the Converter Performance

Process	**0.5μm Bi-CMOS, t-well, 3AL, 1PS**				
Chip area	**2.9 × 3.0mm^2**				
Package	**QFN, 24 pins, 5 × 5mm^2**				
Supply voltage	**2.5V to 4.5V (3.7V, nominal)**				
Inductor/ESR	**10μH / 350mΩ**				
Oscillator frequency	**700kHz (nominal)**				
Current ripple	**290mA**				
Maximum efficiency	**80.8 %**				
Output	**Vo1**	**Vo2**	**Vo3**	**Vo4**	**VoN**
Voltage (V)	**10.2**	**7.0**	**7.5**	**8.0**	**- 9.5**
Load current (max) (mA)	**5**	**30**	**30**	**40**	**5**
Load regulation (mV/mA)	**1.5**	**0.78**	**0.5**	**0.4**	**x**
Line regulation (mV/V)	**58**	**73**	**85**	**90**	**80**
Output ripple (max) (mV)	**160**	**140**	**140**	**120**	**60**
Filtering capacitor / ESR (μF) / (mΩ)	**4.7/300**	**4.7/300**	**4.7/300**	**4.7/300**	**1/250**

The converter's performance is summarized in Table I. The converter can work from 2.5 V to 4.5 V of input voltage. The inductor is 10 μH with a parasitic resistance of 350 mΩ, and the switching frequency is 700 kHz. The four boost outputs Vo1, Vo2, Vo3, and Vo4 are programmable from 5 V to 12 V, but normally regulated at 10.2, 7.0, 7.5, and 8.0 V with ripple voltages of 85, 55, 55, and 50 mV, respectively. All four outputs use 4.7 μF/300 mΩ-ESR filtering capacitors. Line and load regulation standards for commercial products are satisfied. The non-regulated dependent negative output VoN is normally -9.5 V and uses a 1 μF filtering capacitor C_{N2}, a 1 nF charge-pump

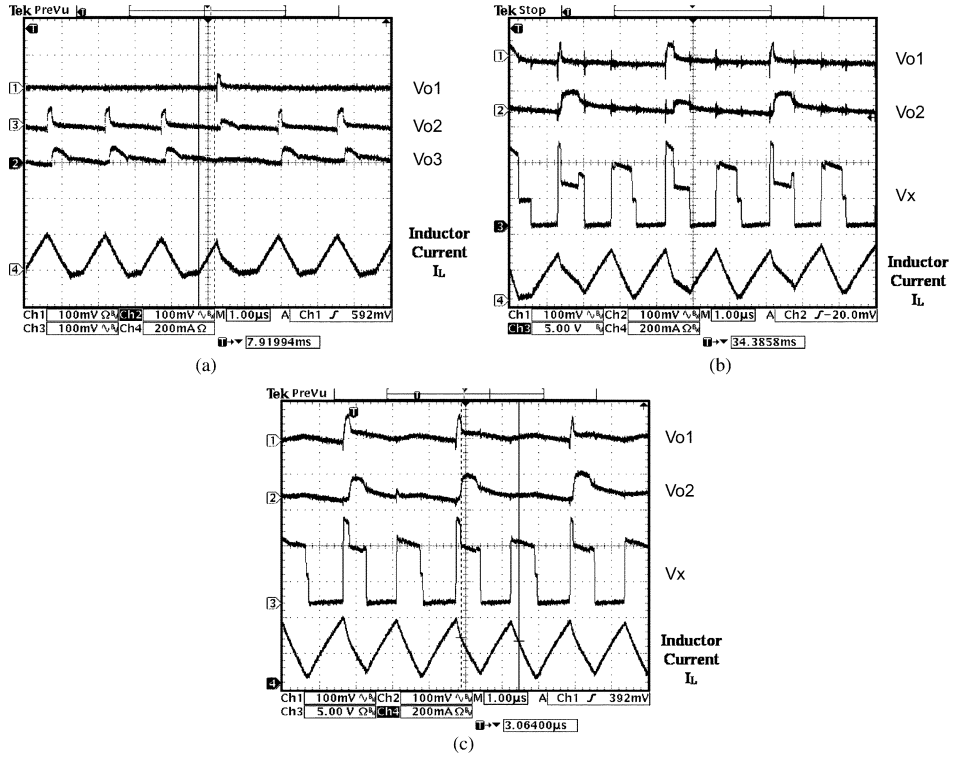

Fig. 18. Measured waveforms. (a) In DCM. (b) At the boundary of DCM and CCM. (c) In CCM.

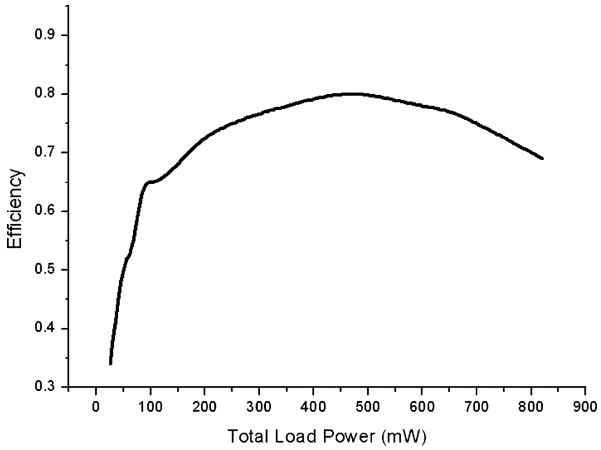

Fig. 19. Efficiency curve.

flying capacitor C_{N1}, and 0.35 V Schottky diodes for high efficiency. Fig. 19 shows the efficiency curve of the converter versus the total output loads. The maximum output power that the converter can still supply with good efficiency is 850 mW, and a maximum efficiency of 80.8% is achieved at a total output power of 450 mW.

V. Future Extension

The simplicity and flexibility of OPDC give SIMO switching dc–dc converter designers a great potential in extending the design. For each additional output, one additional power switch, one comparator in the feedback loop, and a few logic gates are the only necessary components. It is also clear in OPDC that this additional output will be comparator-controlled, preceding the last P-I controlled output. Note that extensions of this design are greatly reduced in size and complexity compared with the design reported in [5] and [6] and greatly improved in terms of output ripples compared with normal hysteretic control like that reported in [7].

VI. Conclusion

In this paper, a first-ever SIMO switching dc–dc converter with five outputs and OPDC is proposed. Several important circuits and concerns with SIMO are discussed, including a full-waveform current sensor, a frequency generator, an in-rush-free soft-start, dead-time control, and cross-regulation. The experimental results verify the validity of OPDC and the other proposed circuits and prove the performance of the converter to be a promising commercial product. Extensions and developments of this design are positively expected.

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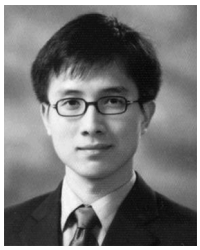

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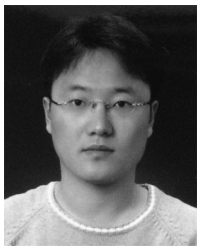

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