A Gray-Level Dependent Pre-Emphasis Column Driver With Fast Settling for Active-Matrix LCD Applications

Young-Suk Son, Hong-Hee Son, Yong-Suk Kim, Hyeong-Seog Oh, and Gyu-Hyeong Cho

***Abstract*—In this brief, simple analytical solutions for pre-emphasis driving conditions in active-matrix liquid crystal display (AMLCD) applications are presented. According to the solutions presented, the column driver with a gray-level dependent pre-emphasis (GLDP) function is designed for fast settling. The GLDP column driver is implemented without using additional frame memory. Also, modifications to the display system and integrated circuit fabrication process changes are not required. The GLDP column driver provides output voltage signals with variable pre-emphasis durations according to the magnitude of the gray-level shift to be driven. By applying the GLDP column driver, 8-μs reduction of the required one row line time was achieved on average. This one row line time reduction makes it possible to realize high performance and low cost AMLCDs. The 640 channel, full function GLDP column driver is fabricated by a 13.5-V 0.35-μm CMOS process.**

***Index Terms*—Active-matrix liquid crystal display (AMLCD), CMOS, column driver, data driver, fast settling, overdrive, pre-emphasis.**

I. Introduction

As THE MARKET for active-matrix liquid crystal displays (AMLCDs) matures, cost and performance are the key factors in market competition. The physical size and resolution of large-sized AMLCD panels have increased and power consumption has decreased according to market demand and to enhance performance competitiveness. Moreover, in order to reduce the cost of a display module, the integration of components has been accelerated and a reduction in the number of column driver integrated circuits (ICs) has been required. Resulting from this trend, the column line *RC* time constant is becoming longer and the allowable one row line time is becoming shorter. Within the reduced row line time, the column line driving with an elongated time constant suffers from an insufficient charging problem and a long liquid crystal (LC) response time.

The driving methods and active matrix architectures proposed to reduce the number of column drivers in a display module have also reduced the given one row line time by half or a third [1]–[5]. By doing this, both the cost and power consumption can be reduced at the same time. However, realizing the proposed schemes in high resolution AMLCDs with several microseconds of column line time constants is difficult using conventional column drivers due to the insufficient charging problem [3].

In order to improve the image quality degradation that originates from a long *LC* response time, various driving systems and circuits have been proposed [6]–[11]. The driving systems primarily use the overdrive methods in the digital domain [7]–[11]. The implementation of overdrive in the digital domain requires changes in the display system and increases costs due to additional frame memories or look-up tables for data processing. As a result, for a more cost-effective method, the analog domain pre-emphasis driving in a column driver has been proposed [6]. The analog domain pre-emphasis driving used pre-emphasis amplitudes that vary according to the magnitude of the gray-level shift to be driven by the capacitance ratio. Thus, in order to ensure the operating voltage margins of the overdrive, this method requires a higher voltage IC fabrication process than that used for conventional column drivers. However, the lower operation voltage of the column driver is important in terms of layout area and power consumption [12]. In addition, the pre-emphasis amplitude control method is inappropriate for various display panels unless the circuit parameters are changed because the pre-emphasis conditions need to change according to the display panel load conditions to maintain the effects of the pre-emphasis drive.

In this brief, we present simple analytical solutions for efficient pre-emphasis driving conditions to improve the insufficient charging problem in low cost, high performance AMLCD applications. A gray-level dependent pre-emphasis (GLDP) column driver that does not require display system changes and additional frame memory is developed according to the solutions presented here.

The flexibility of the column driver for various panel load conditions can be obtained by controlling the pre-emphasis duration in the midgray regions via line-by-line partial data comparisons in the column driver. This duration control does not need a higher voltage process if it is only used in the midgray regions although the effectiveness is somewhat limited. However, the limitation can be mitigated by the gamma curve adjustments or dynamic gamma controls [17], [18]. Therefore, the proposed GLDP column driver can be one of the cost-performance trade-off solutions to solve the insufficient charging problem and enhance the *LC* response time.

II. Solutions for Pre-Emphasis Driving

For simplicity in the analytical solutions, the electrical model of a column line is approximated as a first order circuit, as shown

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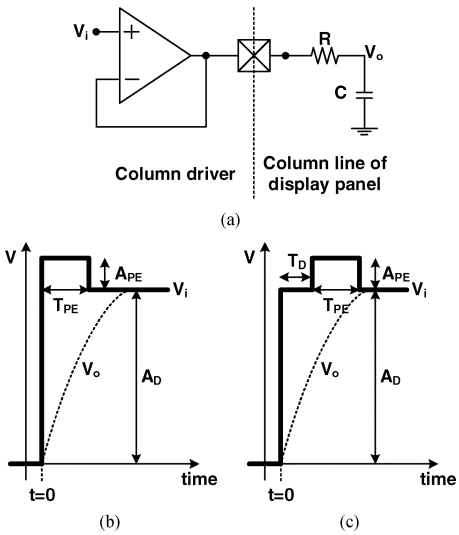


Fig. 1. Pre-emphasis driving conditions. (a) Simplified load model. (b) Pre-emphasis driving without delay. (c) Pre-emphasis driving with delay.

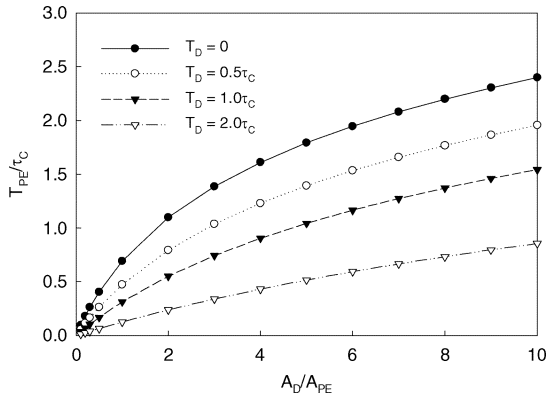


Fig. 2. Normalized plot for the pre-emphasis conditions.

in Fig. 1(a). The driving waveforms with pre-emphasis can be categorized as shown in Fig. 1(b) and (c). The shape of the waveforms depends on the pre-emphasis voltage generation method [6]. The driving waveform with pre-emphasis has three control parameters: T_D, $T_{\rm PE}$, and $A_{\rm PE}$. T_D is the pre-emphasis delay time after starting the data drive; $T_{\rm PE}$ is the pre-emphasis duration; and $A_{\rm PE}$ is the pre-emphasis voltage.

For the input voltage in Fig. 1(b), the corresponding output voltage signal is shown in (1) at the bottom of the page, where τ_C is the time constant *RC* of a column line and A_D is the voltage shift to be driven. For $V_o(t) = V_i(t)$ at $t = T_{\rm PE}$, (i.e., at the end of pre-emphasis) the required pre-emphasis duration $T_{\rm PE}$ is

$$T_{\rm PE} = \tau_C \cdot \ln\left(\frac{A_D + A_{\rm PE}}{A_{\rm PE}}\right). \tag{2}$$

Equation (2) shows that the amplitude and duration of the pre-emphasis can become the design parameters for pre-emphasis driving; moreover, it is shown that the pre-emphasis conditions should change according to the panel load conditions, i.e., τ_C.

For the input voltage in Fig. 1(c), the corresponding output voltage signal is shown in (3) at the bottom of the page, where $T_A = T_D + T_{\rm PE}$. For $V_o(t) = V_i(t)$ at $t = T_D + T_{\rm PE}$, (i.e., at the end of the pre-emphasis), the required pre-emphasis duration $T_{\rm PE}$ is

$$T_{\rm PE} = \tau_C \cdot \ln\left(\frac{A_{\rm PE} + e^{-T_D/\tau_C} \cdot A_D}{A_{\rm PE}}\right). \tag{4}$$

Using (2) and (4), the pre-emphasis conditions that allow the node voltage in a panel to converge on the input voltage at the end of the pre-emphasis are defined. The pre-emphasis duration or amplitude should be varied according to the voltage shift to be driven and the panel load conditions for implementing an efficient pre-emphasis irrespective of the waveform shapes.

By normalizing the pre-emphasis duration to the column line time constant and the voltage shift to be driven to the pre-emphasis voltage in (2) and (4), the pre-emphasis conditions can be defined in a single plot, as shown in Fig. 2. $T_{\rm PE}/\tau_C$ represents the required relative length of the pre-emphasis duration compared with the column line time constant. $A_D/A_{\rm PE}$ represents the relative swing of the voltage shift to be driven compared with the pre-emphasis voltage. The effective driving time (i.e., $T_D + T_{\rm PE}$) to converge cannot be shortened by T_D, although T_D allows the required pre-emphasis duration to shorten.

From these solutions, it can be concluded that the equivalent effects of pre-emphasis can be obtained by controlling the pre-emphasis duration with a limited voltage magnitude, $A_{\rm PE}$, instead of a variable pre-emphasis amplitude. Consequently, the duration control can be more efficient than amplitude control in relation to operation voltages. In addition, the operation voltage of a column driver with the pre-emphasis function can be maintained by confining the valid pre-emphasis operation range to the midswing regions.

III. Proposed Column Driver

A. Column Driver Architecture

The full-function GLDP column driver is implemented by adding three functional circuit blocks into a conventional column driver, as shown in Fig. 3. The pre-emphasis timing generation circuit (PTGC), pre-emphasis voltage generation circuit (PVGC), and GLDP timing generator achieve the GLDP

$$v_o(t) = \begin{cases} (A_D + A_{\rm PE}) \cdot \left(1 - e^{-t/\tau_C}\right), & t \le T_{\rm PE} \\ A_D \cdot \left(1 - e^{-t/\tau_C}\right) - A_{\rm PE} \cdot \left(e^{-t/\tau_C} - e^{(T_{\rm PE}-t)/\tau_C}\right), & t \ge T_{\rm PE} \end{cases} \tag{1}$$

$$v_o(t) = \begin{cases} A_D \cdot \left(1 - e^{-t/\tau_C}\right), & t \le T_D \\ A_D \cdot \left(1 - e^{-t/\tau_C}\right) + A_{\rm PE} \cdot \left(1 - e^{-(t-T_D)/\tau_C}\right), & T_D \le t \le T_A \\ A_D \cdot \left(1 - e^{-t/\tau_C}\right) - A_{\rm PE} \cdot e^{-(t-T_D)/\tau_C} \cdot \left(1 - e^{T_{\rm PE}/\tau_C}\right), & t \ge T_A \end{cases} \tag{3}$$

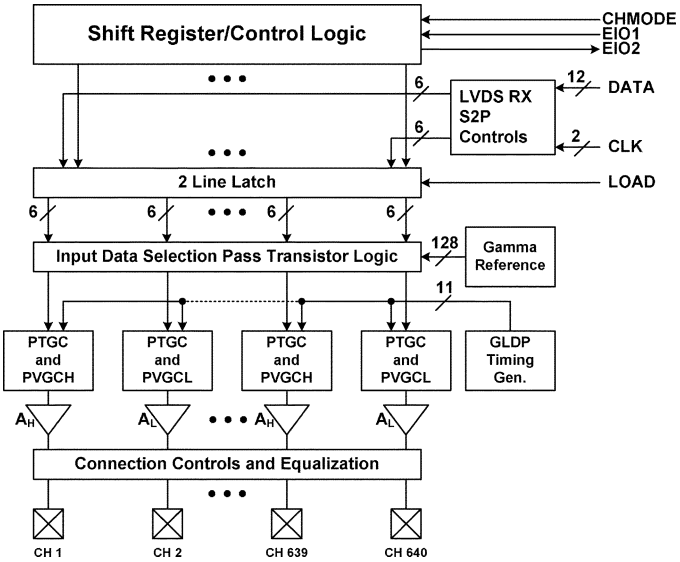


Fig. 3. Proposed column driver architecture.

function. The PTGC controls the duration of the pre-emphasis according to the voltage shift to be driven. The PVGC combines the input data voltage and pre-emphasis voltage by utilizing the control signals from the PTGC. The GLDP timing generator provides 11 timing signals that define the pre-emphasis duration for each channel. One of 11 timing signals is selected by the PTGC and given to the PVGC for variable pre-emphasis durations according to the voltage shift to be driven in each channel. For area and power efficiency, various column driver and channel buffer amplifiers have been introduced into the architecture [12]–[16]. Among these architectures, the proposed GLDP circuits are applied to the column driver architecture as explained in [12].

Fig. 4 shows the composition of the gamma curves and valid GLDP operation ranges. For the polarity inversion operation, these voltage levels are divided into two groups: one composed of 64 voltage levels between 0.1 V and half of the $V_{\rm dd}$ for the negative gamma curve and the other composed of 64 voltage levels between half of the $V_{\rm dd}$ and $V_{\rm dd}$ –0.1 V for the positive gamma curve. The voltages in the negative gamma curve are driven through A_L while the voltages in the positive gamma curve are driven through A_H, where A_L and A_H are the drive amplifiers for negative and positive voltages, respectively. The outputs of the chip are automatically assigned to their column inversion mode as the chip provides the outputs of A_H and A_L simultaneously.

For simplicity in operation, a vertical 1-dot inversion operation is adopted and the operation of the GLDP is confined to the midgray regions. This confined valid pre-emphasis voltage range provides advantages in terms of chip size and supply voltage. With these GLDP operation ranges, the supply voltage of the GLDP column driver does not exceed that of a conventional column driver. Therefore, higher voltage processes are not required during the fabrication of the proposed GLDP column driver.

B. GLDP Timing Generator

Fig. 5 shows the GLDP timing generator that gives the 11 timing signals. $f_{\rm CLK}$ is a system clock of 100 MHz. The system

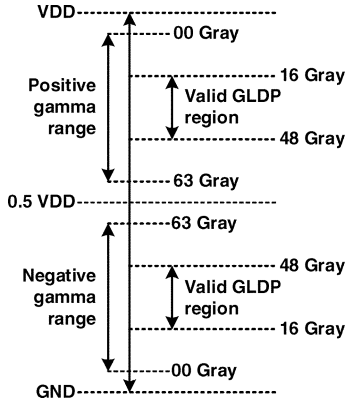


Fig. 4. GLDP operation ranges and transmittance curves.

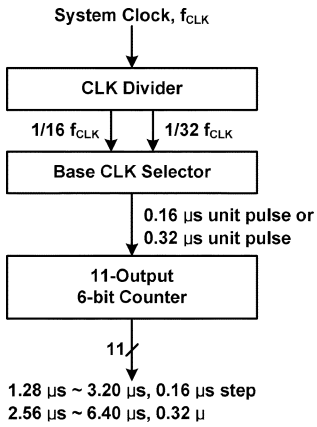


Fig. 5. GLDP timing generator.

clock is divided to make sufficient pulse widths with a compact counter. The dividing ratio is 1/16 or 1/32; one of the ratios is set by an external control. According to the dividing ratio, the pre-emphasis duration can be changed for all gray-levels in a valid pre-emphasis range. A 6-bit counter is produced from the base clock and provides the 11 timing signals generated to each PTGC in the channel.

C. Pre-Emphasis Timing Generation Circuit

The unit channel architecture of the GLDP column driver is shown in Fig. 6. The unit channel architecture is composed by adding the PTGC and PVGC to each channel as explained previously. The PTGC is composed of a 3-bit latch (third latch), a 3-bit comparator, and a timing selector. The comparator receives the 3-bit MSB data from the 2nd latch, which stores the present driving data, and the 3-bit MSB data from the third latch, which stores the previous line driving data. By comparing the two data states, the 4-bit data that determines the pre-emphasis duration is generated in the comparator and sent to the PVGC. The data from the PTGC controls the switch states of the PVGC. The pre-emphasis duration varies from 1.28 to 3.2 μs by a 0.16-μs step as the magnitude of the gray-level changes in the default mode. Fig. 7 shows the design result of the pre-emphasis duration compared with the result calculated in (4). Using a 3-bit MSB data comparison instead of a full data comparison reduces the layout area of the third latch and the comparator while maintaining performance advantages. The partial data comparison has an advantage of reducing the circuit area and complexity.

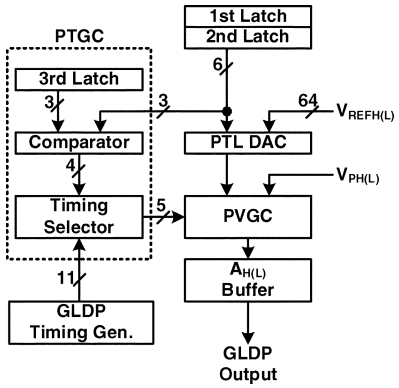


Fig. 6. Unit channel architecture of the GLDP column driver.

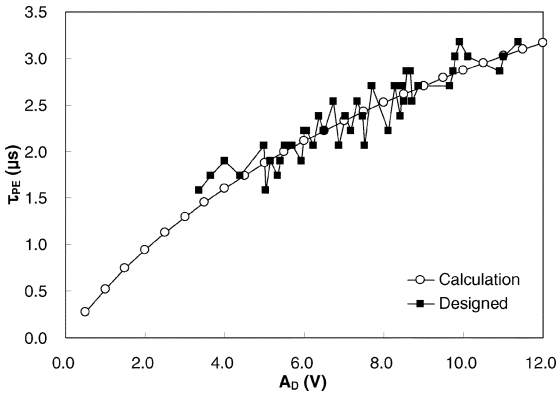


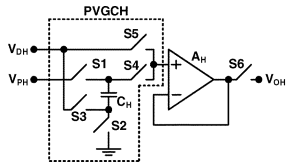
Fig. 7. Designed pre-emphasis duration according to the voltage shift to be driven (for $T_D = 2\,\mu$s, $A_{\rm PE} = 1.5$ V and $\tau_C = 2.2\,\mu$s).

However, the required pre-emphasis durations generated deviate slightly from the calculated result.

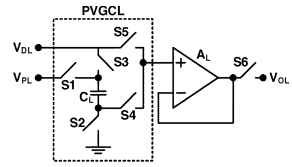
D. Pre-Emphasis Voltage Generation Circuit

Fig. 8 shows two complementary PVGCs and switch states for operation modes. For the polarity reversal operation, the voltage levels are divided into two groups: one for the positive gamma curve and the other for the negative gamma curve, as shown in Fig. 4. For this operation, two PVGCs are required. The PVGCH generates $V_{DH} + V_{PH}$ as the input data of the A_H buffer for the positive gamma curve and the PVGCL generates $V_{DL} - V_{PL}$ as the input data of the A_L buffer in the negative gamma curve. Each PVGC has one capacitor and five switches.

When the GLDP column driver operates, the operation periods are divided into three periods: equalization, overdrive, and normal drive. During the equalization period, S1, S2, and S5 are closed while the other switches are open. Therefore, the pre-emphasis voltages V_{PH} and V_{PL}, are sampled and stored in C_H and C_L, respectively. After the equalization period, GLDP driving, which depends on control signals from the PTGC, begins. If the GLDP operation is enabled, all switches are open, except S3, S4, and S6. The pre-emphasis duration is then proportional to the magnitude of the gray-level shifts. The duration of the GLDP is controlled by signals from the PTGC. After the GLDP driving, the normal driving continues. During the normal driving pre-emphasis is disabled. Due to the combined operation of the PVGC and PTGC, pre-emphasis duration-controlled voltage waveforms are generated according to the voltage shift to be driven.



(a)

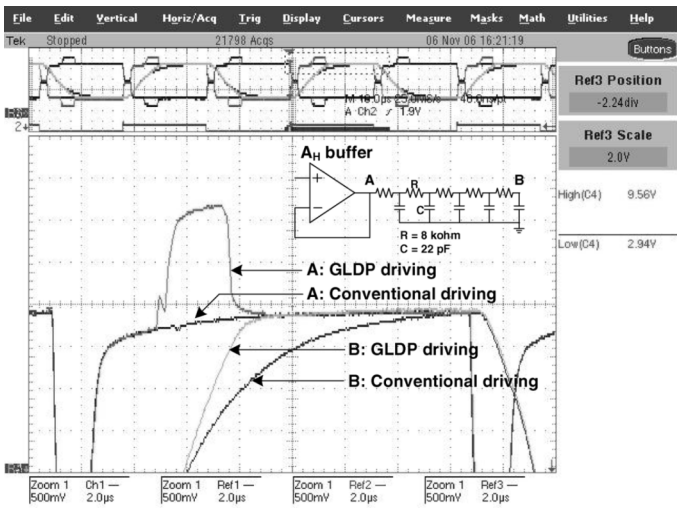


(b)

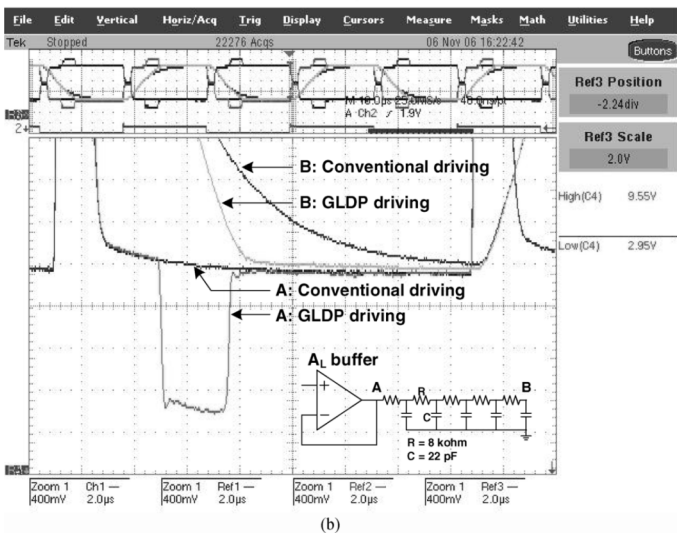
Period	S1	S2	S3	S4	S5	S6
Equalization	ON	ON	OFF	OFF	ON	OFF
GLDP Driving	OFF	OFF	ON	ON	OFF	ON
Normal Driving	ON	ON	OFF	OFF	ON	ON

(c)

Fig. 8. Pre-emphasis voltage generation circuits. (a) PVGCH. (b) PVGCL. (c) Switch states for the three different operation modes.



(a)



(b)

Fig. 9. Pre-emphasis driving waveforms (a) A_H buffer. (b) A_L buffer.

IV. Experimental Results

We manufactured the proposed column driver using a 13.5-V 0.35-μm CMOS process. The size of the GLDP column driver is 14454 μm$\times$ 1654 μm. The pre-emphasis durations have two options as the magnitude of the gray-level changes: from 1.28 to 3.2 μs with a 0.16-μs step or from 2.56 to 6.4 μs with a

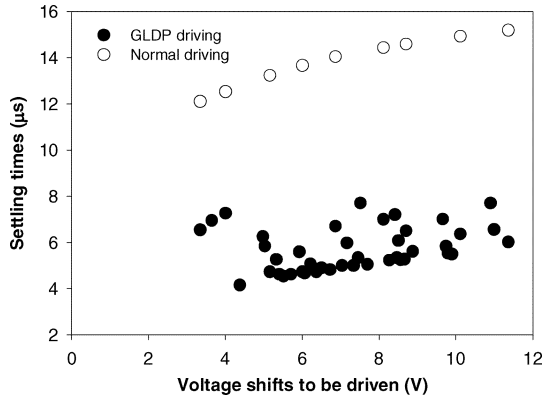


Fig. 10. Measurement of settling times (for $T_D = 2\ \mu$s, $A_{\rm PE} = 1.5$ V).

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED COLUMN DRIVER

	This work	Ref. [5]	Ref. [8, 9, 10]
Requirements for overdrive			
System change	No	No	Yes
Additional memory	No	No	Yes
Process change	No	Yes	Yes
Operation voltage increase	0 V	> 3 V	> 3 V
Application flexibility	Good	Bad	Good
Settling time reduction (20 mV error voltage)	5.3 ~ 8.9 μs	6.83 μs	NA
Circuit size (μm x μm)			
PTGC	180x35/ch		
PVGC	20x35/ch	NA	NA
GLDP Timing Gen.	250x1100		

0.32-μs step for various panel load conditions. Fig. 9 shows typical GLDP driving waveforms that reduced the settling times compared with conventional driving. The effectiveness of the GLDP column driver was verified in terms of electrical requirements with a five-stage *RC* distributed model as a panel load. The total resistance and capacitance were 40 kΩ and 110 pF as column line parasitic resistance and capacitance, respectively. The data driving times required to converge to the final data line voltages within 20-mV error were measured as shown in Fig. 10. The fluctuation of the settling time was generated by the pre-emphasis duration deviation from the calculations. An 8-μs reduction of the settling time was achieved, on average. Improvements in visual performance were also verified using an AMLCD panel with 20.1-in WSXGA (1680 RGB $\times$ 1050) resolution.

Table I summarizes the performances of the proposed column driver. As stated previously, the GLDP column driver could be implemented with minimum cost and change to realize the pre-emphasis function. The area portion of PTGC, PVGC, and GLDP timing generator in the chip was 25%.

V. CONCLUSION

We presented analytical solutions for pre-emphasis driving conditions. With the solutions obtained, the pre-emphasis conditions were defined for various driving conditions. Also, the GLDP column driver was designed to overcome the insufficient charging problem and achieve response time acceleration in the LC. After applying the GLDP to a conventional column driver, an 8-μs reduction of the required row line time was achieved. The GLDP column driver is cost effective because display system changes, higher voltage IC fabrication processes, or additional frame memory are not required in the driver. Full functionality and effectiveness of the GLDP column driver have been verified through waveform measurements in an *RC* distributed model and its application to an AMLCD panel.

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