A Series-Parallel Compensated Uninterruptible Power Supply with Sinusoidal Input Current and Sinusoidal Output Voltage

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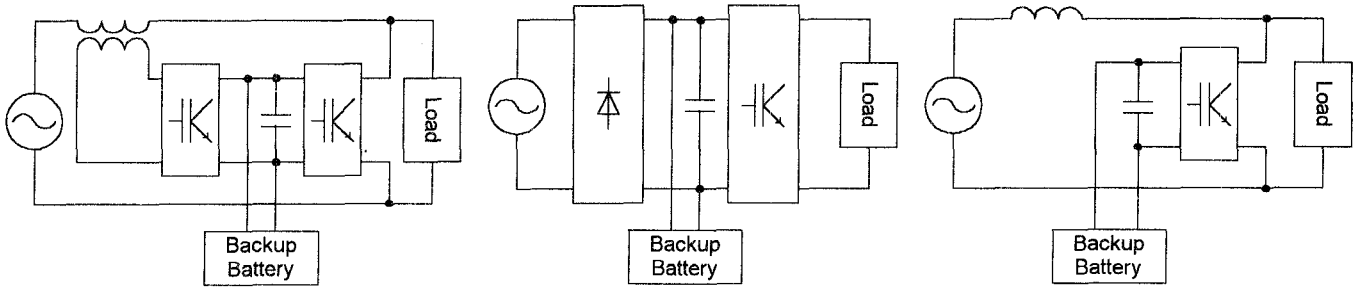
Abstract -

In this paper a series-parallel compensated UPS is suggested, which has high input power factor and sinusoidal output voltage regulation capability. Compared to conventional cascaded UPS, the size can be reduced significantly with high quality input and output waveforms. In this paper, analysis and experimental results for a prototype are presented.

I. INTRODUCTION

UPS is indispensable in the critical loads such as on-line system for banks, life-supporting system, etc. The proposed series-parallel compensated UPS shown in Fig.1-(a) has excellent input-output characteristics and can be sized small. The series-parallel structures are also found in other applications[1-3]. Unified power flow controller(UPFC) and unified power quality conditioner(UPQC) are very similar to the proposed system[1,2]. The proposed system however, is quite different in purpose, operation and control strategy from the other series-parallel systems. The parallel elements of UPFC and UPQC control current, and the series elements of those control voltage. In other words, the parallel elements of those inject current in order to compensate line current, and the series elements compensate voltage to sustain desired output voltage. On the other hand, the parallel element of the proposed system controls output voltage to shape sinusoid with constant RMS value, and the series element controls line current to shape sinusoid in phase with the input voltage. Since it is imperative that output voltage be sinusoidal in UPS even when an outage occurs, a voltage-controlled parallel element is preferable to a current-controlled parallel element.

Compared to conventional cascaded UPS shown in Fig.1-(b), the front converter of the proposed system shown in Fig.1-(a) has smaller size and the main inverter handles smaller amount of power during normal operation. On the other hand, the parallel processing UPS shown in Fig.1-(c), in which loads are connected to the lines and a power converter is connected in parallel, is also small-sized with harmonic and reactive compensation[4-6] but losing its voltage regulation capability, or with voltage regulation capability losing line current control capability.



(a) The Proposed UPS (b) Conventional cascaded UPS (c) Parallel processing UPS

Figure 1. Structures of UPS's

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II. OPERATION OF THE SYSTEM

The detailed circuit diagram of the proposed system is shown in Fig. 2. The front converter and the main inverter have the common DC link which consists of a capacitor and a backup battery. The front converter is connected in series with the line and the load through a linking transformer. The system has two operation modes. One is bypass mode, and the other is backup mode. When the line is alive, the system operates in bypass mode and when an outage occurs, the system operates in backup mode. In bypass mode, the front converter is controlled so that the line current i_1 is sinusoidal and in phase with the line voltage v_1 and the DC link voltage of the converter is constant. The main inverter is controlled for the output voltage v_2 to be sinusoidal and in phase with the line voltage with constant RMS value. The phasor relation in bypass mode is shown in Fig.3. In backup mode, the front converter is disconnected from the line and does not regulate the line current. The main inverter alone operates supplying power to the load from the backup battery. The system changes the modes simply by turning on and off the front converter according to the input condition and the main inverter just regulates the output voltage continuously. Since the backup battery can be charged by the co-operation of the front converter and the main inverter, no extra charging circuit is needed. To get the power relations of the converter at normal operation, let the complex power required by the load be

$$\mathbf{S}_L = P_L + jQ_L . \tag{1}$$

In the steady state when the input power is equal to the output power, the input current becomes

$$\mathbf{I}_1 = \frac{P_L}{V_1} = \frac{V_2 I_2 \cos\phi}{V_1} . \tag{2}$$

where I_2 is RMS value of the load current, V_2 is of the load voltage, and V_1 is of the line voltage. The power delivered from the line to the front converter is given by

$$\mathbf{S}_a = (\mathbf{V}_1 - \mathbf{V}_2)\mathbf{I}_1^* = P_L\left(1 - \frac{V_2}{V_1}\right) . \tag{3}$$

If $\mathbf{V}_1$ and $\mathbf{V}_2$ are out of phase, some reactive power flows through the front converter and the apparent power $|\mathbf{S}_a|$ increases.

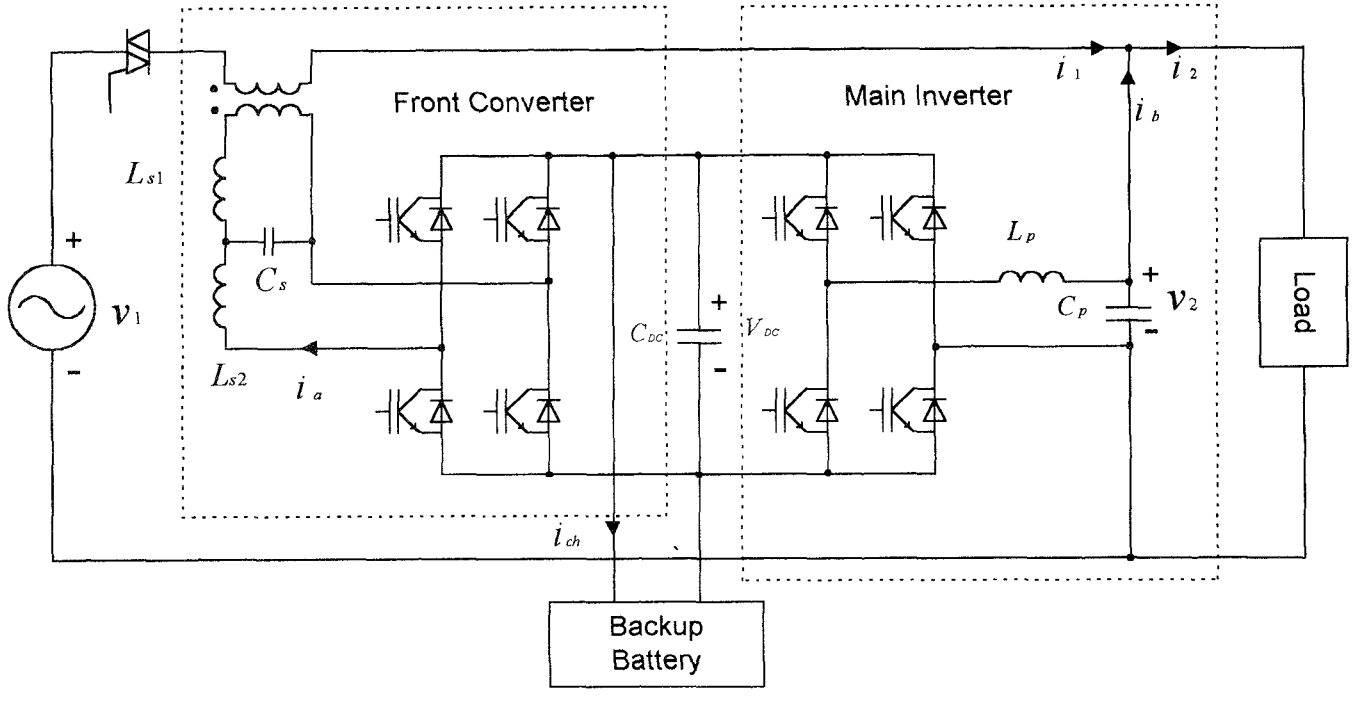


Figure 2. Detailed Circuit diagram of the proposed UPS

The power delivered from the main inverter to the load becomes

$$\mathbf{S}_b = \mathbf{S}_L - \mathbf{V}_2\mathbf{I}_1^* = P_L\left(1-\frac{V_2}{V_1}\right) + jQ_L . \qquad (4)$$

When the input voltage is greater than the output voltage, $\mathrm{Re}\{\mathbf{S}_a\}$ and $\mathrm{Re}\{\mathbf{S}_b\}$ are positive, i.e., voltage compensating power flows from lines to the front converter and from the main inverter to the load. When the input voltage is less than the output voltage, $\mathrm{Re}\{\mathbf{S}_a\}$ and $\mathrm{Re}\{\mathbf{S}_b\}$ are negative, i.e., voltage compensating power flows from the load to the main inverter and from the front converter to the line.

In Fig. 4-(a), the power handled by the front converter is plotted. When the allowable input voltage variation is 20[%], the required power rating is only 25[%] of the load. In Fig.4-(b), the power handled by the main inverter at normal operation is plotted. If the load power factor is high, the main inverter handles only a small portion of the load power. Hence the operation efficiency is improved compared to conventional cascaded UPS.

Charging of battery is accomplished by increasing input current above the value given by (2). In this case the excess power P_{ex} given as (5) flows into the backup battery and the average charging current I_{ch} is given as (6).

$$P_{ex} = \mathrm{Re}\{\mathbf{S}_a\} - \mathrm{Re}\{\mathbf{S}_b\} = V_1 I_1 - V_2 I_2 \cos\phi . \qquad (5)$$

$$I_{ch} = \frac{P_{ex}}{V_{DC}} = V_1 I_1 - V_2 I_2 \cos\phi . \qquad (6)$$

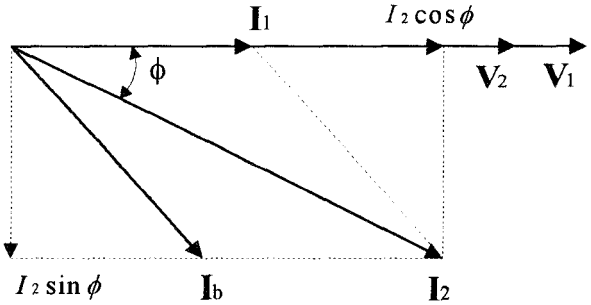
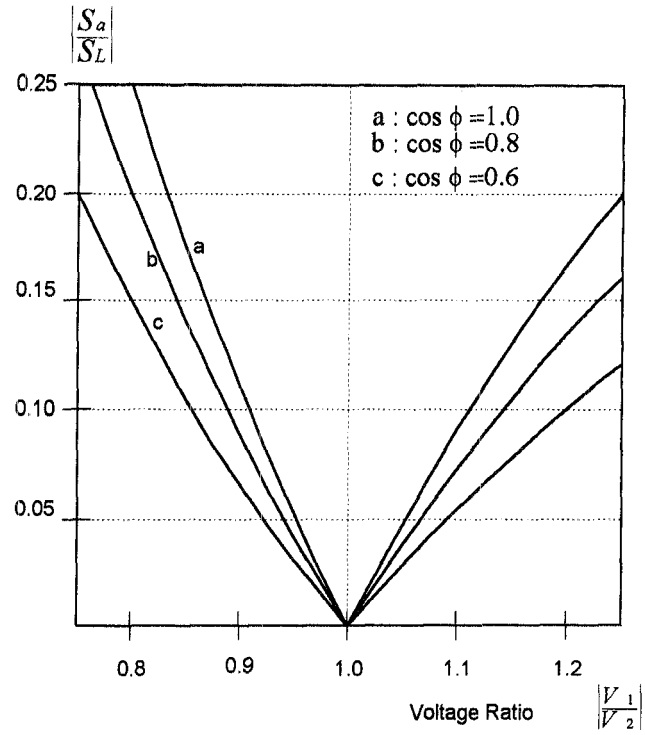
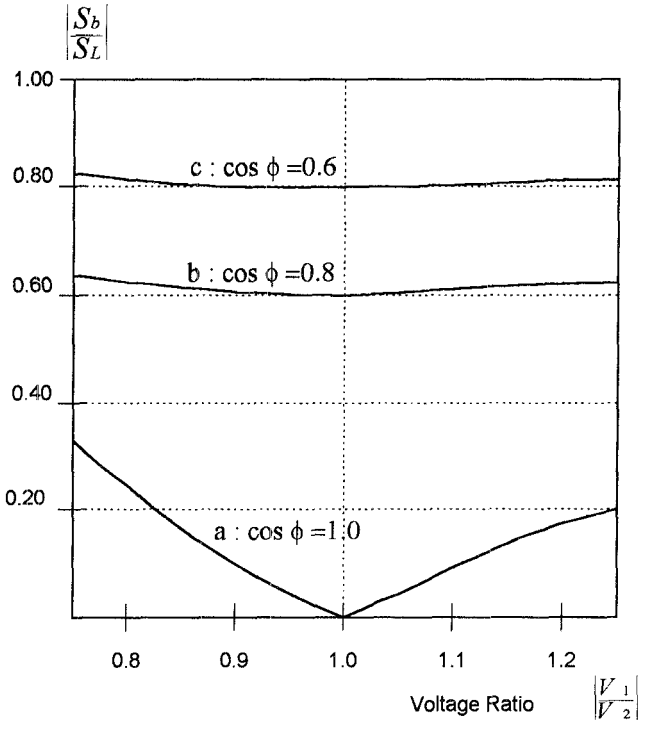


Figure 3. Phasor Diagram



(a) Power handled by the front converter



(b) Power handled by the main inverter

Figure 4. Power handled by the system

III. CONTROL OF THE SYSTEM

When the system operates properly, the system can be thought conceptually as in Fig. 5. We can consider the front converter as a sinusoidal current source and the main inverter as a sinusoidal voltage source. The high order harmonics of the load current i_2 are absorbed in capacitor C_p, and the low order harmonics are supplied by the main inverter. The sinusoidal current source i_1 isolates the input from the output with regard to harmonics.

A. Control of the line current

Since we can consider the main inverter as sinusoidal voltage source, we can simplify the system as in Fig. 6. The load current is supplied by the main inverter freely. The block diagram of the line current control is shown as in Fig. 7. The right part of the block diagram is obtained from the circuit shown in Fig. 6 and the left part is added for the controller. In the prototype, the front converter operates at discontinuous conduction mode as shown in Fig. 8 where i_a is the actual current waveform and i_{ar} is peak current reference. Averaging the triangular shape current i_a, the gain of the innermost loop is 0.5. We can consider that the innermost loop is a linear current amplifier and the innermost pole is neglected if the bandwidth of the second loop is narrow enough. The second loop controls terminal voltage of the inductor Ls1 with the current amplifier. The outermost loop controls the line current i_1. PI controllers are used for Gc1(s) and Gc2(s). Transfer function is given as (7). The effect of the difference of the input and the output voltage on the line current i_1 is given as (8). The frequency response is obtained as in Fig.9, where (a) is for the transfer function between i_{1r} and i_1 and (b) for the transfer function between i_1 and $v_1 - v_2$. From (a) we know that the bandwidth of the sytem is about 500Hz which is enough for the line current control loop whose reference signal is 60Hz, and from (b) that the admitance obtained from (8) is less than 1 milli mho which is enough to isolate the lines from the load with regard to harmonics.

$$\frac{I_1(s)}{I_{1r}(s)} = \frac{0.5\,G_{c1}(s)\,G_{c2}(s)}{1 + C_s L_{s1} s^2 + 0.5\,L_{s1}\,s\,G_{c3}(s) + 0.5\,G_{c1}(s)\,G_{c2}(s)} \quad (7)$$

$$\frac{I_1(s)}{V_1(s) - V_2(s)} = \frac{C_s s}{1 + C_s L_{s1} s^2 + 0.5\,L_{s1}\,s\,G_{c3}(s) + 0.5\,G_{c1}(s)\,G_{c2}(s)} \quad (8)$$

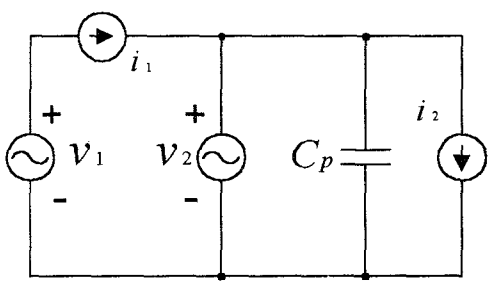


Figure 5. Simplified Equivalent Circuit

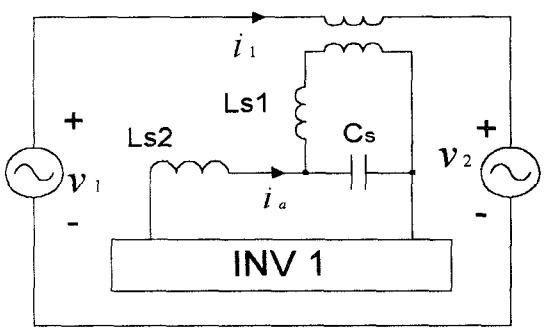


Figure 6. Equivalent circuit for the front converter

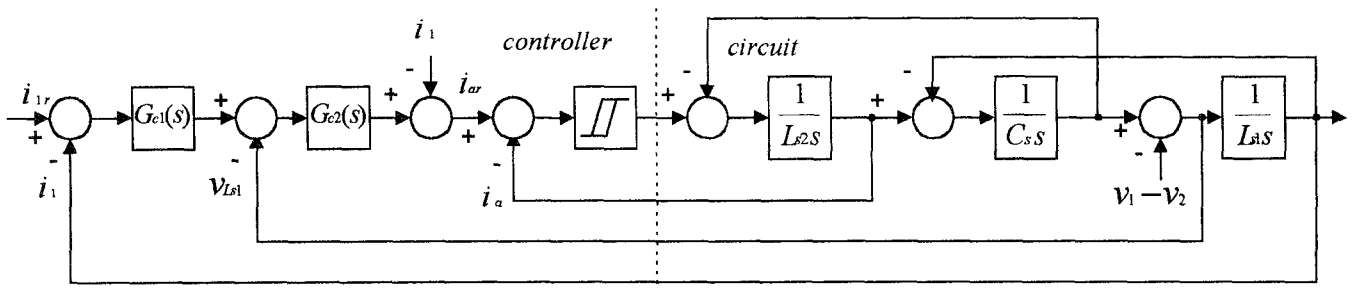


Figure 7. Control loop for the front converter

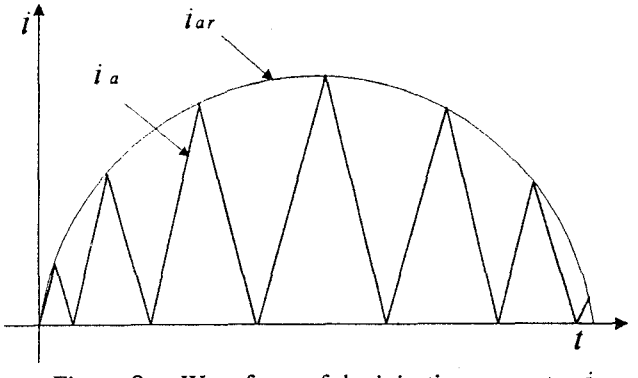


Figure 8. Waveform of the injection current i_a

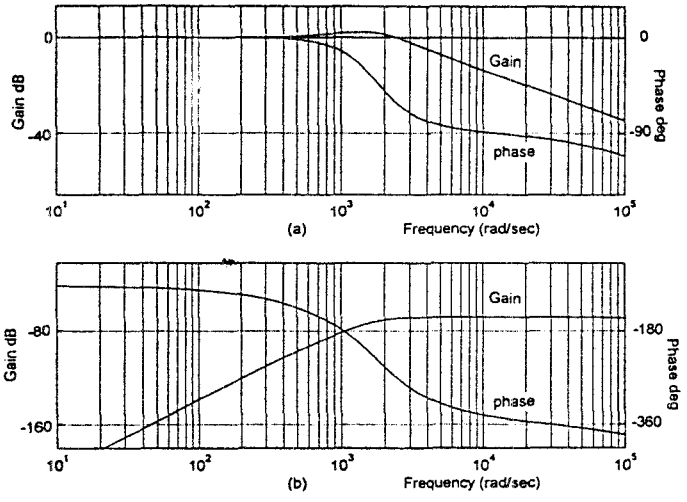


Figure 9. Frequency reponse of the front converter (a) I_1/I_{1r}, (b) $I_1/(V_1-V_2)$

B. Control of the output voltage

Since we can consider the front converter as a sinusoidal current source, we can simplify the system as in Fig. 10 for the output voltage control. The control loop for this case is constructed as in Fig. 11. Removing the outermost feedback loop and controller Gc2(s) from the block diagram shown in Fig. 7 we obtain a block diagram very similar to Fig. 11. The transfer function between v_{2r} and v_2 is given as (9). The effect of the difference between the line current and the load current on the load voltage which is treated as disturbance is represented as (10) and to be minimized. The effect is minimum when H(s) is 2, hence it is desirable that the gain of the innermost loop and the gain H(s) are well-matched.

$$\frac{V_2(s)}{V_{2r}(s)} = \frac{0.5G_{c3}(s)}{C_p s + 0.5G_{c3}(s)} \quad . \tag{9}$$

$$\frac{V_2(s)}{I_2(s) - I_1(s)} = \frac{0.5}{C_p s + 0.5G_{c3}(s)}\left(1 - \frac{H(s)}{2}\right) \quad . \tag{10}$$

The frequency response is obtained as in Fig. 12 where (a) is for the transfer function between v_{2r} and v_2 and (b) for the transfer function between $i_2 - i_1$ and v_2 with H(s)=0.5 and H(s)=1.8. From (a) we know that the bandwidth of the sytem is about 1.6kHz which is enough for the load voltage control loop whose reference signal is 60Hz, and from (b) that 1.8 of H(s) gives the main inverter low impedance enough to absorb the harmonic current of the load.

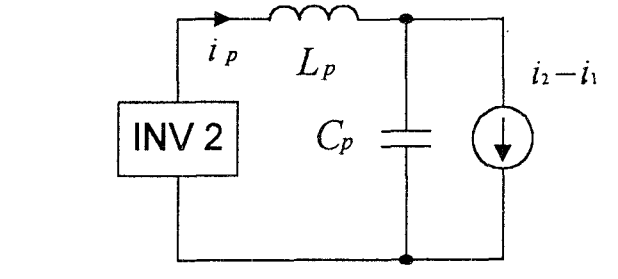


Figure 10. Equivalent Circuit for the main inverter

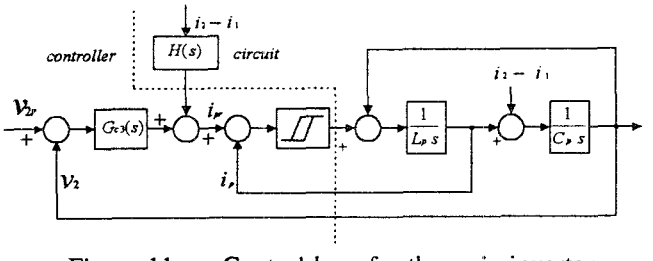
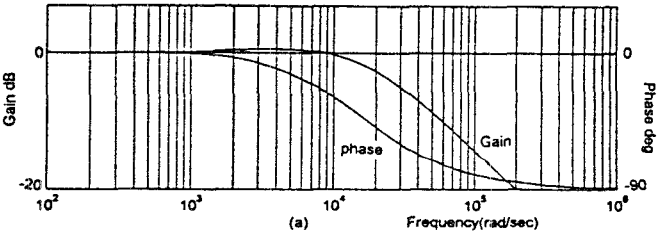


Figure 11. Control loop for the main inverter



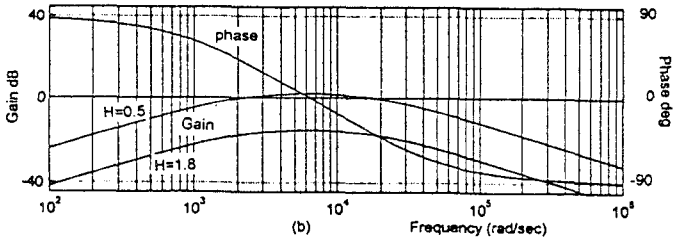


Figure 12. Frequency reponse of the main inverter
(a)V_2/V_{2r}, (b) $V_2/(I_2-I_r)$

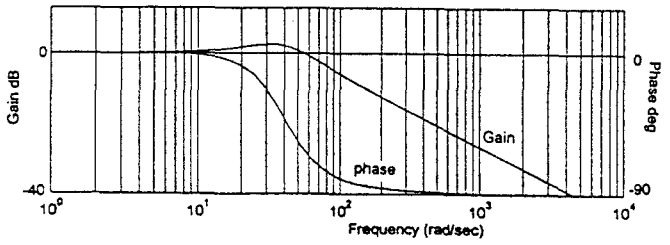


Figure 14. Frequency response of the DC link controller

C. Control of the DC-link voltage

Because the UPS system has large energy storage system in the DC-link and 120[Hz] ripple has to be rejected, DC-link control loop need not to have wide bandwidth. Since the DC-link voltage varies slowly and its variation is small, we can construct the DC-link control loop as in Fig. 13 using low frequency small signal model. PI controller is also used for Gc4(s) which is designed initially without backup battery and feedback loop having gain K, and then the backup battery and the loop are connected. I_{1r} is RMS reference for the line current i_1, and the value of K is selected according to the characteristics of the backup battery used. The transfer function between ΔV_{DCr} and ΔV_{DC} is given as (11).

The frequency response is obtained as in Fig. 14. The bandwidth of the closed loop is about 8Hz.

$$\frac{\Delta V_{DC}(s)}{\Delta V_{DCr}(s)} = \frac{V_1 G_{c4}(s)}{V_{DC} C_{DC} s + V_1 G_{c4}(s)} \quad . \qquad (11)$$

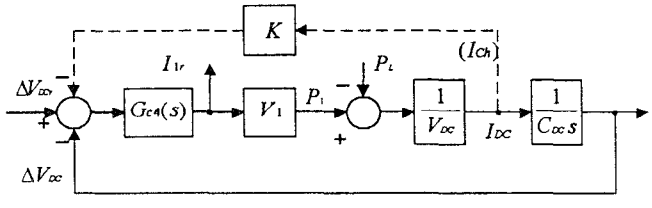


Figure 13. Low Frequency Small Signal Model for DC-link control

D. Change of modes and generation of reference signals

To synchronize the line current and the load voltage with the line voltage, a PLL(phase locked loop) is used. The output of PLL v_{PLL} is sinusoidal and in phase with v_1. The voltage reference signal v_{2r} is obtained attenuating v_{PLL}. The current reference i_{1r} is obtained multiplying v_{PLL} with I_{1r} which is the RMS reference generated in DC link control loop. When an outage occurs, the PLL is free-running. The free-run frequency is set to 60 Hz. It is thought that an outage occurs when the difference between the line voltage and the reference exceeds allowable range. In this case, the front converter is disconnected from the line and the system operates in backup mode. If the line recovers to normal voltage, the front converter resumes to regulate the line current and the system returns to bypass mode. The change from backup mode to bypass mode is accomplished after the PLL is exactly synchronized.

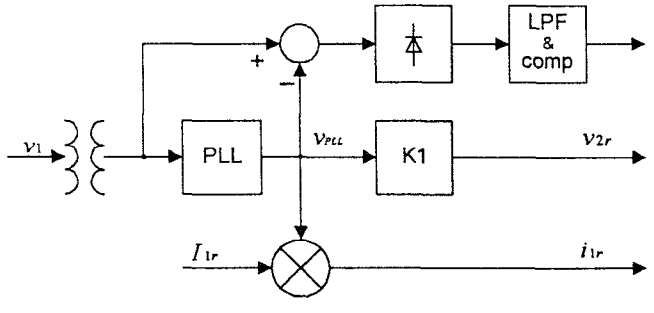


Figure 15. Outage detection and reference generation circuit

IV. EXPERIMENTAL RESULTS

1 kVA prototype is made and tested. Experimental results are shown in Fig. 16 - 18. The load is a capacitor input type rectifier with a series inductor. Inspite of nonlinear load, the line current and the output voltage is sinusoidal and in-phase with the input voltage in Fig. 16. Changes of modes are shown in Fig. 17, where the output voltage is observed not affected. Fig. 18 shows the response of output voltage to step load change, where the output voltage is also observed not affected.

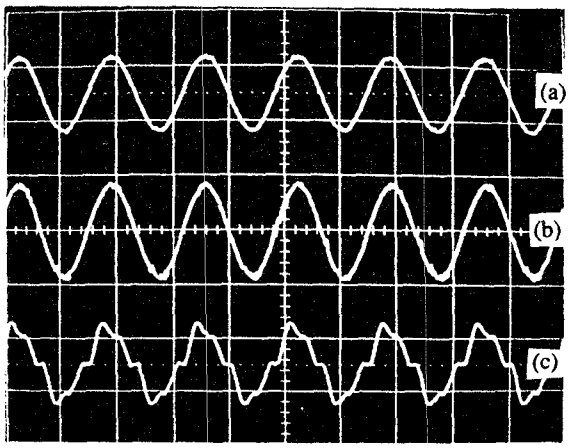


Figure 16. Input and output waveforms
(a) load voltage 200[V/div], (b) line current 10[A/div], (c) load current 10[A/div], time base : 5[msec/div]

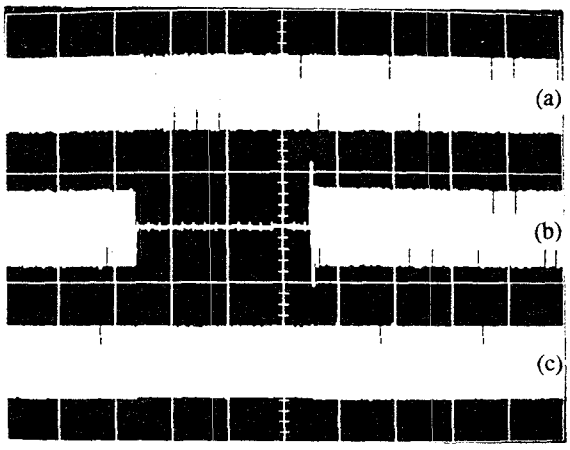


Figure 17. Change of modes
(a) load voltage 200[V/div], (b) line current 10[A/div], (c) load current 10[A/div], time base : 0.5[sec/div]

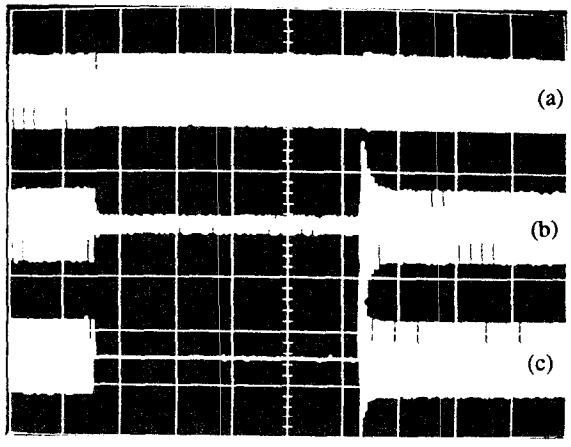


Figure 18. Response to step load change
(a) load voltage 200[V/div], (b) line current 10[A/div], (c) load current 10[A/div], time base : 0.5[sec/div]

V. CONCLUSION

In this paper, a series-parallel compensated UPS is represented. It can be small-sized compared to conventional cascaded UPS. Its input power factor is high and output voltage is well regulated to sinusoid. The proposed system and control strategy is confirmed by the experiment. This system is considered to be adequate for such applications requiring high quality input and output waveforms.

REFERENCES

[1] L. Gyugyi, "Unified power-flow control concept for flexible AC transmission systems", IEE PROC. pt. C, Vol. 139, No. 4, pp.323-331, JULY 1992

[2] H. Fujita, and H. Akagi,"The Unified Power Quality Conditioner: The Integration of Series Active Filters and Shunt Active Filters", IEEE, PESC'96 record, pp494-501, 1996

[3] S. Moran,"A Line Voltage Regulator/Conditioner for Harmonic Sensitive Load Isolation", IEEE IAS 24th annual meeting, pp947-951, 1989

[4] G. Ioannidis, et al., "A Novel Uninterruptible Power Supply System with Sinusoidal Input-Output Characteristic and Simplified Control Circuit", IEE EPE '95 record vol. 2, pp.351-356, 1995

[5] H. L. Jou, et al., "A New Parallel Processing UPS with the Performance of Harmonic Suppression and reactive Power Compensation", IEEE PESC '94 record, pp.1443-1450, 1994

[6] Y. Lin, G. Joos, and J.F. Lindsay, "Performance Analysis of Parallel Processing UPS Systems," IEEE APEC '93 record, pp533-539, 1993