A High Dynamic Range CMOS Power Amplifier

Changkun Park, Younsuk Kim, Jeonghu Han, Dongho Lee, *Donghyun Baek, and Songcheol Hong

Korea Advanced Institute of Science and Technology(KAIST)

*Samsung Electronics Co., Republic of Korea

A 1.9 GHz CMOS differential power amplifier for polar transmitter applications is implemented with 0.25 μm RFCMOS process. All of matching components, input transformer and output transformer are fully integrated with 50-Ω input and output matching. The each power transistor in an each differential branch are again split and controlled separately to have a high power mode and a low power mode. It achieves a drain efficiency of 32 % at the maximum output power. The maximum output power is 29.5 dBm at 3.3 V supply voltage. The dynamic range is measured about 27.5 dB with the Vdd range of 0.7 V ~ 3.3 V.

To satisfy the GSM standard, the dynamic range of Pout must be above 20 dB. For the given range of Vdd which is presented in the output of LDO or DC-DC converter, it is very important to find the way to increase the dynamic range of a power amplifier especially for polar transmitter applications. The proposed power amplifier shows high dynamic range using split topology, and is implemented with 0.25 μm CMOS process.

A single turn transformer (STT) is used as the output transformer, which has a direct influence on the output power and efficiency of power amplifiers. The STT is composed of high-Q coupled slab inductors to minimize the loss of output transformer [1]. In Fig. 1, the schematic of STT structure is shown. With an additional shunt MIM capacitor, which has higher Q than the slab inductor of STT, the output matching network is fully integrated.

The conventional cascode structure of Class-E is shown in Fig. 2 (a). Theoretically, the dynamic range of cascode Class-E power amplifier is also 13.5 dB for the Vdd range of 0.7 V ~ 3.3 V. To get the higher dynamic range of power amplifier, the gate voltage of the common gate MOSFET (M1) is bound to Vdd as shown in Fig. 2 (b).

The second method to increase the dynamic range is to split the power-stage. In high power mode, all the power transistors are turned on. In low power mode, a part of power transistors are turned off. The previous work uses additional switch in the power stage to turn on and off a part of power transistors, as shown in Fig. 3. The additional switch may reduce the efficiency of power amplifier during a maximum output power.

ACKNOWLEDGEMENT

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REFERENCES

[1] Ichiro Aoki, Scott D. Kee, David B. Rutledge, and Ali Hajimiri, “Distributed active transformer – A new power-combining and impedance-transformation technique,” *IEEE Transactions on microwave theory and techniques*, pp. 316-331, vol. 50, January. 2002.

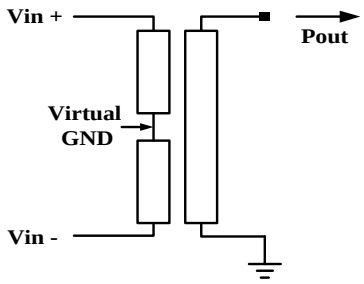
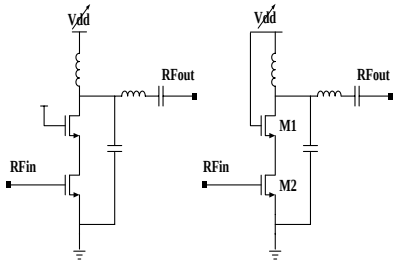


Fig. 1. Schematic of output transformer - single turn transformer (STT).



(a) (b)

Fig. 2. (a) Conventional Class-E power amplifier (b) Class-E power amplifier where Vgs of common gate

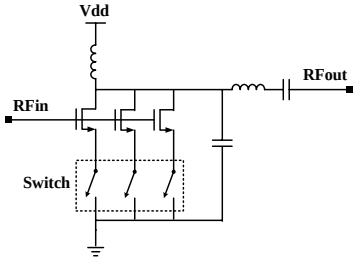


Fig. 3. Conventional power-controllable structure of Class-E.

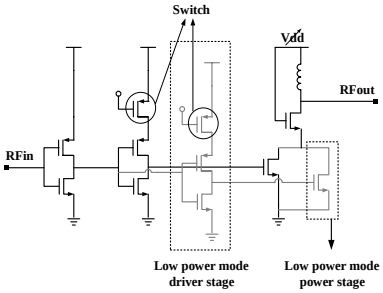


Fig. 4. Schematic of the proposed power amplifier.

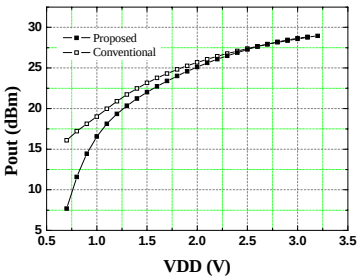


Fig. 5. Dynamic range of a conventional and the proposed

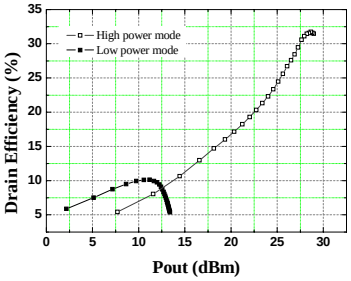


Fig. 6. Drain efficiency vs. Pout of high power mode

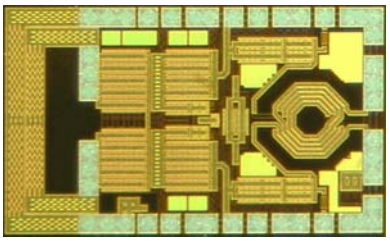


Fig. 7. Chip photograph of proposed power amplifier.