# A Ka Band MMIC Power Amplifier With Bus-bar Combiner

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## Abstract

A Ka-band power amplifier MMIC was made using 0.15-μm gate length GaAs pHEMT technology. A bus-bar power combiner at the output stage is used to minimize the combiner size and to simplify bias network. The fabricated power amplifier shows 30dBm (1 Watt) P1dB CW output power, 14.84dB G1dB, and 18% PAE at P1dB in Ka band. The chip size is $4 \times 2.4mm^2$.

## 1. Introduction

As satellite communication system market is increased, the high power amplifier (HPA) with output power levels of 1 watt or more is required [1,2,3]. Additionally, the chip cost and the power of 1dB gain compression point is key requirement of HPA. It should be noted that the size of chip is necessarily reduced, because it relates with chip cost. To achieve high output power, power transistors have to be combined. Therefore, the power combiner method is very important for high output power and small chip size. For minimizing size and simplifying bias connection, the bus-bar power combiner at the output stage is used. Most of reported researches use the balanced topology due to good input/output return loss. However, it has lower output power and gain performance because there is loss due to an additional coupler. This paper presents the design and development of the 1-watt Ka band MMIC power amplifier with bus-bar combiner.

## 2. Circuit Design

The device used in this work is a Triquint's 3MI 0.15μm GaAs pseudomorphic HEMT technology. A 0.15 μm × 400 μm transistor is used as a basic cell. A modified Marteka model was supported as a transistor model. Load-pull source pull simulation is performed using HP ADS to obtain the optimum load and source impedances.

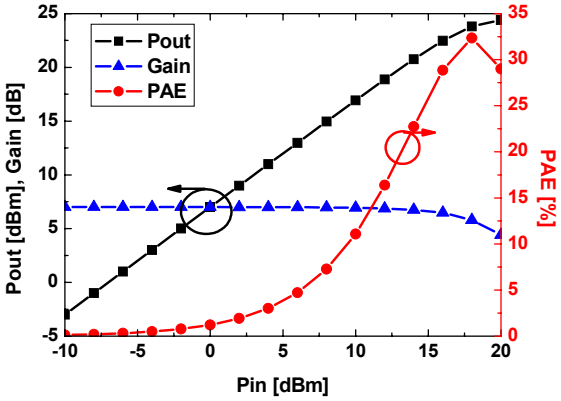


**Fig. 1. The Power Sweep Simulation Results of the Basic Cell.**

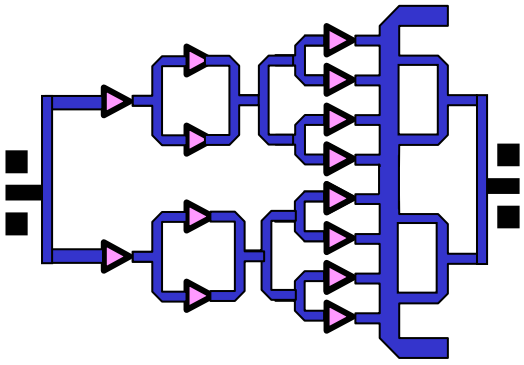

**Fig. 2. The Topology of Implemented Power Amplifier.**

At the optimum impedance, the power sweep simulation results of the basic cell are shown in Fig.1. This transistor shows P1dB of 23dBm and G1dB of 6dB, and 31% PAE under the bias condition of $V_{DS}$=5V and $I_{DS}$=70mA at the 30GHz. To get output power above 30dBm, eight transistors need to be combined at the output stage.

Also, to achieve the gain above 15dBm, three-amplication state is needed.

The topology of implemented power amplifier is shown Fig.2.

To achieve small chip size and simple drain-bias connection, a bus-bar power combiner is used [4,5]. Also the output of the power amplifier is fully matched single-ended design for more output power. The inter-stage ratio of 1:2:4 was chosen to achieve sufficient output power, power gain and power drive margin on each stage.

The bus-bar combiner has more asymmetry than a binary tree combiner such as the Wilkinson combiner. But, the drain bias line is longer than 1/16λ, the lowering of performance due to those asymmetries in the power amplifier will be negligible. As longer length of the drain bias line increased to 1/4λ, the asymmetries of phase and amplitude are decreased. However, the longer length of the drain bias line needs large chip size. Therefore, the trade off between performance and chip size is needed.

The resistor between the combined transistors is included to suppress odd-mode oscillation. Also, in order to prevent low frequency oscillation in bias-circuit, RC resonance circuits were included at the gate and the drain-bias line. And to prevent oscillation in band, the series resistance is inserted at the front gate of transistor. The power amplifier satisfies the unconditionally stable condition in simulation results using the K-factor at various bias conditions for the maximum oscillation frequency as shown Fig. 3.

In these conditions, the simulation result is summarized in Table.1.

## 3. Measurement Results

Fig.4 shows the photo of the chip of the high power amplifier. The chip area is 4mm × 2.4mm.

To measure the performance of the fabricated power amplifier, a test fixture was used in consideration of heat dissipation and to eliminate bias-circuit oscillation, the power amplifier was tested using GSG probes on Cascade probe station. All measurements were carried out under CW operation condition of $V_{DS}$=4.4V and $I_{DS}$=1.5A.

Fig. 5 shows the measured S-parameters of the power amplifier. The small-signal gain is above 15dB from 30.085 to 30.885GHz.

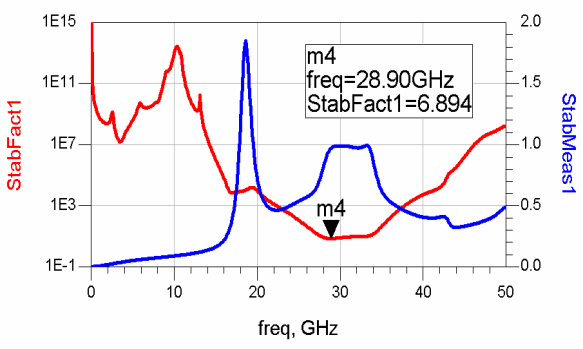


**Fig. 3. Stability Simulation Results**

| GHz | Frequency | 29~33GHz(3GHz) |
|---|---|---|
| dB | Small signal gain | >18dB |
| dBm | P1dB( output) | > 30dBm |
| %@P1dB | PAE | >12.8 % |
| dB for return loss & unitless for VSWR | Input<br>Output | <-15dB |
| V | Supply | 5V |
| mA | Current consumption | 1550 mA |

**Table.1. Summary of the Simulation Results of Ka Band Power Amplifier**

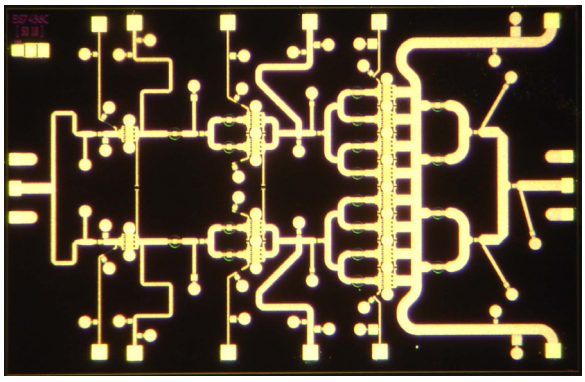

**Fig. 4. Photo of the Chip of 1 Watt MMIC Power Amplifier with Chip Size of 4 mm× 2.4 mm**

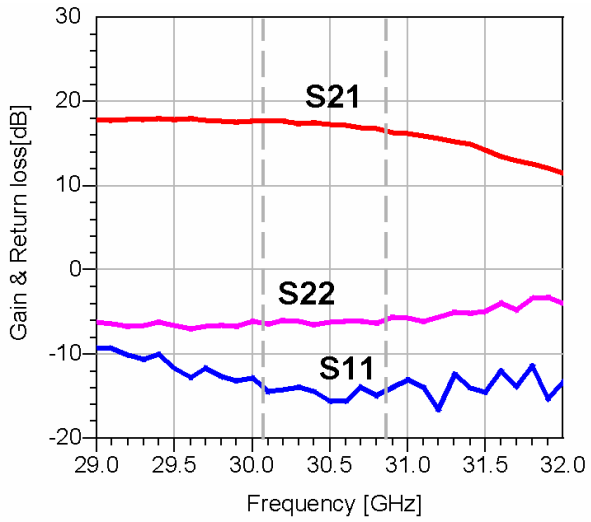


**Fig. 5. Measured S-parameters of the Power Amplifier.**

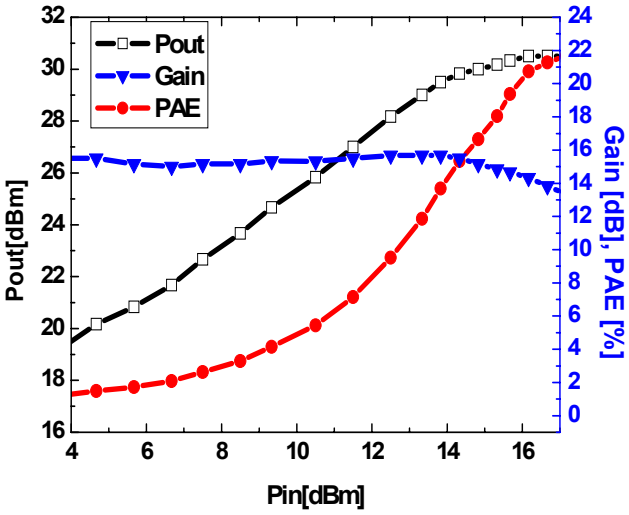


**Fig. 6. Measured Performance of the Power Amplifier at 30GHz.**

Input/output return loss is less than -12dB and -6dB in the Ka band. Fig. 6 shows the measured power performance of the power amplifier. The fabrication power amplifier shows P1dB of 30dBm, G1dB of 14.84dB, and PAE of 18% at 30GHz.

These measurement results are summarized in Table.2. Compared with table.1, the power amplifier is well matched with simulation results except the output return loss.

| | | |
|---|---|---|
| GHz | Frequency | 30GHz |
| dB | Small signal gain | >15dB |
| dBm | P1dB( output) | > 30dBm |
| %@P1dB | PAE | >18 % |
| dB for return loss & unitless for VSWR | Input<br>Output | <-12dB<br><-6dB |
| V | Supply | 4.4V |
| mA | Current consumption | 1500 mA |

**Table 2. Summary of the Fabricated Power Amplifier**

## 4. Conclusions

We have presented the 1-watt ka band MMIC power amplifier with bus-bar combiner. For minimizing size and simplifying bias connection, the bus-bar power combiner at the output stage is used. And in order to get output power and gain, the single ended structure is used. This chip, with P1dB of 30dBm, G1dB of 14.84dB, and PAE of 18% at 30GHz, has chip size of $4 \times 2.4 mm^2$.

## Acknowledgement

This work was partly supported by KOSEF under the ERC program through the MINT research center at Dongguk University and by the Agency for Defense Development, Korea, through the Radio Detection Research Center at Korea Advanced Institute of Science & Technology.

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