

## Direct growing of lightly doped epitaxial silicon without misfit dislocation on heavily borondoped silicon layer

HoJun Lee, ChangSoo Kim, ChulHi Han, and ChoongKi Kim

Citation: *Appl. Phys. Lett.* **65**, 2139 (1994); doi: 10.1063/1.112769

View online: <http://dx.doi.org/10.1063/1.112769>

View Table of Contents: <http://apl.aip.org/resource/1/APPLAB/v65/i17>

Published by the [American Institute of Physics](#).

---

### Additional information on *Appl. Phys. Lett.*

Journal Homepage: <http://apl.aip.org/>

Journal Information: [http://apl.aip.org/about/about\\_the\\_journal](http://apl.aip.org/about/about_the_journal)

Top downloads: [http://apl.aip.org/features/most\\_downloaded](http://apl.aip.org/features/most_downloaded)

Information for Authors: <http://apl.aip.org/authors>

## ADVERTISEMENT



**Goodfellow**  
metals • ceramics • polymers • composites  
70,000 products  
450 different materials  
**small quantities fast**

[www.goodfellowusa.com](http://www.goodfellowusa.com)

# Direct growing of lightly doped epitaxial silicon without misfit dislocation on heavily boron-doped silicon layer

Ho-Jun Lee

Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Kusong-dong 373-1, Yusong-gu, Taejon 305-701, Korea

Chang-Soo Kim

Korea Research Institute of Standards and Science, P. O. Box 102, Taeduk Science Town, Taejon 305-600, Korea

Chul-Hi Han and Choong-Ki Kim

Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Kusong-dong 373-1, Yusong-gu, Taejon 305-701, Korea

(Received 23 May 1994; accepted for publication 16 August 1994)

Without buffer layers, a lightly boron-doped epitaxial layer of good crystalline quality has been directly grown on a heavily boron-doped silicon layer by eliminating misfit dislocations in the heavily boron-doped layer. X-ray diffraction analysis revealed that the epitaxial silicon has good crystallinity, similar to that grown on lightly doped silicon substrate. The leakage current of an  $n^+/p$  diode fabricated in the epitaxial silicon has been measured to be  $0.6 \text{ nA/cm}^2$  at 5 V. © 1994 American Institute of Physics.

The structure of lightly boron-doped ( $p$ ) epitaxial silicon on heavily boron-doped ( $p^+$ ) silicon is popular for ultralarge scale integrated (ULSI) fabrication because of the low junction leakage current and less affection of alpha particle due to the short minority carrier diffusion length in the  $p^+$  silicon.<sup>1-3</sup> Recently, bonding wafers were fabricated using the structure in which the  $p^+$  (above  $7 \times 10^{19}/\text{cm}^3$ ) layer serves as an etch-stop in ethylenediamine-pyrocatechol-water mixture during substrate etching and epitaxial  $p$  layer as silicon-on-insulator film.<sup>4</sup> In these applications, electronic properties of the epitaxial layer are very critical because the electronic devices are fabricated in the layer. However, misfit dislocations which can degrade electronic properties (especially, increase junction leakage current) are frequently generated in the epitaxial  $p$  layer due to in-plane lattice mismatch between the  $p$  layer and  $p^+$  layer.<sup>3,5</sup> Thus, elimination of misfit dislocations in the epitaxial layer is very important for the successful fabrication of electronic devices in the layer.

It is known that the in-plane lattice mismatch between the epitaxial layer and  $p^+$  layer originates from the misfit dislocations in the  $p^+$  silicon layer which release tetragonal distortion of the  $p^+$  silicon by insertion of extra-half planes.<sup>6</sup> Thus, if the misfit dislocation in a  $p^+$  layer can be suppressed, an epitaxial  $p$  layer on the  $p^+$  layer can be directly grown without misfit dislocation. Already, we have suggested a method to suppress the misfit dislocation in a  $p^+$  layer by surrounding with undoped region which protects the propagation of misfit dislocation from the wafer edge to the  $p^+$  region inside the undoped region.<sup>7</sup>

In this letter, we report that a high quality epitaxial  $p$  layer can be directly grown without buffer layers on a  $p^+$  layer formed by the method suggested in Ref. 7 and the

epitaxial layer is misfit dislocation-free and has good crystallinity and good electronic properties.

The experiments are as follows. 4-in.,  $p$ -type, and (100)-orientation Czochralski silicon wafers with the resistivity of  $2-10 \Omega \text{ cm}$  and defect density of  $1-2/\text{cm}^2$  are prepared. Chemical-vapor deposited (CVD) oxide of  $1 \mu\text{m}$  thickness is deposited and patterned. After RCA cleaning, boron diffusion is subsequently performed as shown in Fig. 1(a). The diffused regions are classified into two, i.e., one surrounded by the CVD oxide pattern (interior region) and the other which is open to the wafer edge (exterior region). Boron

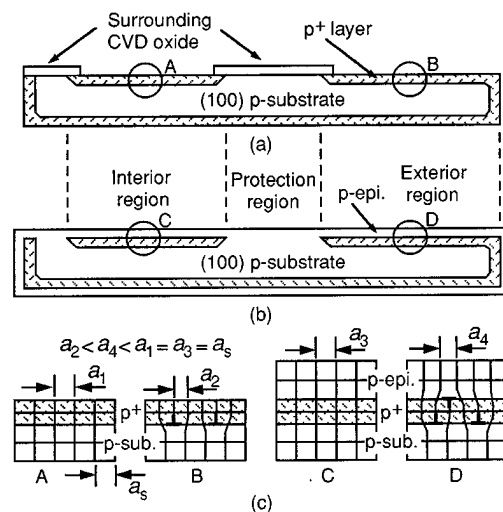


FIG. 1. Process sequence for the experiments. Vertical wafer structures (a) after boron diffusion and (b) after epitaxial growing. (c) Vertical lattice structures showing lattice match or mismatch in the circled regions (A, B, C, and D) of (a) and (b).  $\perp$  and T are misfit dislocations in the  $p^+$  layers and epitaxial layers, respectively.

<sup>a</sup>Also with Hyundai electronics industry Co.

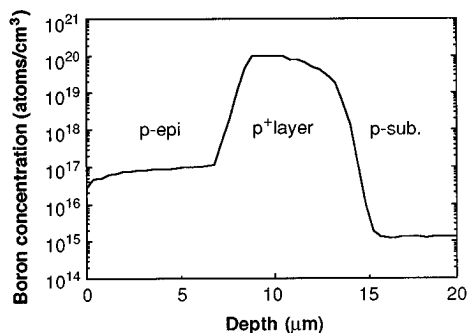


FIG. 2. Measured boron-doping profile in the epitaxial wafer.

diffusion is carried out at 1100 °C for 3 h using  $\text{BBr}_3$ . The diffusion condition can produce misfit dislocations in the  $p^+$  layer of the exterior region, but cannot in that of the interior region because misfit dislocations propagating into the interior region from the wafer edge are protected by the undoped region (protection region) under the surrounding CVD oxide. Thus, as illustrated in Fig. 1(c), in-plane lattice size ( $a_1$ ) of the  $p^+$  layer of the interior region remains as that ( $a_s$ ) of the substrate, while that ( $a_2$ ) of  $p^+$  layer of the exterior region is reduced by insertion of extra half-planes accompanying the misfit dislocations. After boron diffusion, the wafer is oxidized at 850 °C for 30 min in steam ambient and all oxides including the CVD oxide are removed in HF solution. Then, epitaxial silicon of 8  $\mu\text{m}$  thickness is grown on the wafer as shown in Fig. 1(b) with growth rate of 0.5  $\mu\text{m}/\text{min}$  using  $\text{SiHCl}_3$  at 1130 °C. Before epitaxial growing, HCl etching of 0.3  $\mu\text{m}$  was performed for the surface cleaning at 1120 °C for 2 min in the epitaxial reactor. After epitaxial growing,  $\text{N}_2$  purging is performed and the wafers are pulled out of the reactor. One can infer that there is no misfit dislocation in the epitaxial layer of the interior region because of the absence of in-plane lattice mismatch between the epitaxial layer and the  $p^+$  layer ( $a_3 = a_1$ ), while there exist misfit dislocations in that of the exterior region ( $a_4 \neq a_2$ ). Figure 2 shows the boron-doping profile of the wafer measured by spreading resistance profile analysis.

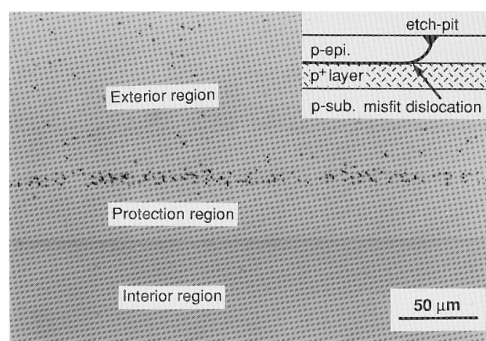


FIG. 3. Photomicrograph of the surface of the epitaxial layers etched in Secco etchant for 30 s. Many etch pits (dark dots) are shown in the exterior region. The relation between misfit dislocation in the epitaxial layer and the etch pit is illustrated in the inset which is the vertical structure of the exterior region.

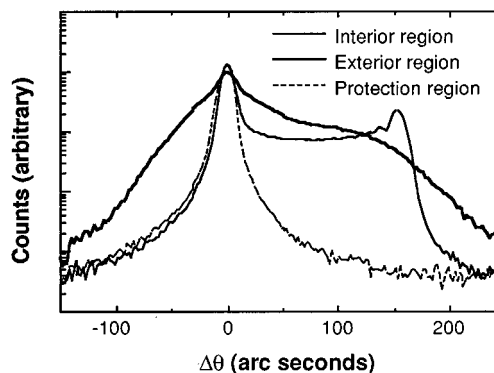


FIG. 4. (400) double-crystal x-ray rocking curves for the interior region, exterior region, and protection region.

Figure 3 shows a photomicrograph of the surface of the epitaxial layer defect etched in Secco etchant for 30 s. There are many etch pits in the exterior region, especially near the boundary with the protection region, while there is no etch pit in the protection region and the interior region. The etch pits show terminations of the misfit dislocations in the epitaxial layer as depicted in the inset of Fig. 3. Thus, it can be known that the epitaxial layer of the interior region is grown without misfit dislocation inherently and propagation of the misfit dislocations from the exterior region to the interior region is prohibited by the protection region.

To examine the crystallinity of the wafer, x-ray diffraction analysis was performed. Figure 4 shows (400) rocking curves for the interior region, exterior region, and protection region obtained by a double-crystal x-ray diffractometer, using  $\text{Cu } K\alpha_1$  radiation. The main peaks (at  $\Delta\theta = 0$ ) for each curve are due to the substrates and the epitaxial layers. The main peak for the interior region is sharp and is similar to that for the protection region which has good crystalline quality due to the direct growing of the epitaxial layer on the substrate, while the peak for the exterior region is widely

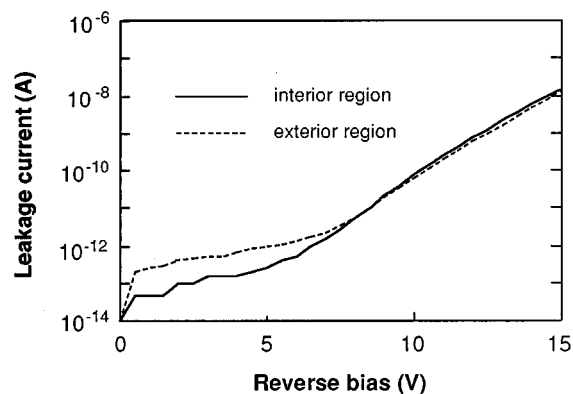


FIG. 5. Measured leakage currents of  $n^+/p$  gated diodes with an area of  $4 \times 10^{-4} \text{ cm}^2$  fabricated in the interior region and exterior region.

spread due to poor crystalline quality of the epitaxial layer. Also, the satellite peak which is due to the  $p^+$  layer is apparent and sharp for the interior region, while the peak is broad for the exterior region. Thus, we can find that the crystallinities of the epitaxial layer and the  $p^+$  layer in the interior region are good, while those in the exterior region are degraded by misfit dislocations in the layers.

We fabricated  $n^+/p$  gated diodes with area of  $4 \times 10^{-4}$   $\text{cm}^2$  in the wafer and measured  $I$ - $V$  characteristics. Figure 5 shows typical  $I$ - $V$  characteristics of the diodes for reverse bias with weak accumulation under the gate electrode. As expected, the diode in the interior region shows lower leakage current (0.6  $\text{nA}/\text{cm}^2$  at 5 V) than that in the exterior region (2.2  $\text{nA}/\text{cm}^2$  at 5 V).

In conclusion, directly grown lightly doped epitaxial silicon on a misfit dislocation-free  $p^+$  silicon layer also shows misfit dislocation-free characteristics. The epitaxial silicon also shows good electrical property as well as good crystal-

linity compared with the conventional epitaxial silicon. It can be expected that the method for formation of misfit dislocation-free epitaxial silicon on the  $p^+$  silicon layer can be successfully used for the ULSI and bonding wafer fabrications.

We would like to thank J.-M. Lee and S.-H. Park in Samsung Electronics Co. for the great help on the boron diffusion and epitaxial growing.

<sup>1</sup>J. W. Slotboom, M. J. J. Theunissen, and A. J. R. de Kock, IEEE Electron Devices Lett. **EDL-4**, 403 (1983).

<sup>2</sup>D. S. Yaney and C. W. Pearce, IEDM Tech. Dig. 236 (1981).

<sup>3</sup>G. A. Rozgonyi and R. R. Kola, in *Defect Control in Semiconductors*, edited by K. Sumino (Elsevier Science, North-Holland, 1990), p. 579.

<sup>4</sup>K. Mitani and U. M. Gosele, J. Electron. Mater. **21**, 669 (1992).

<sup>5</sup>R. B. Fair, J. Electrochem. Soc. **125**, 923 (1978).

<sup>6</sup>H. J. Queisser, J. Appl. Phys. **32**, 1776 (1961).

<sup>7</sup>H. J. Lee, Y. J. Jeon, C. H. Han, and C. K. Kim, Appl. Phys. Lett. **64**, 2955 (1994).