Permeable Base Transistor for Optoelectronic Integrated Circuits by Selective Liquid Phase Epitaxy

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ABSTRACT

A permeable base transistor has been proposed as a possible device in OEIC. The close placement between the electronic device and the optical one would make coupling parasitics small. The selective LPE was used for the lateral growth of GaAs over tungsten fingers.

1. INTRODUCTION

There has been a great deal of efforts in the development of optoelectronic integrated circuit (OEIC) technology. The structural differences between the devices to be integrated make the OEIC difficult to be fabricated. To solve this problem, there have been two approaches, the horizontal integration (HOEIC) and the vertical integration (VOEIC). In HOEIC, the laser diodes are usually embedded into the substrate for planarization. In VOEIC, the laser diodes are integrated vertically with the electronic devices. This can have small parasitics and tight coupling between the electronic devices and the optical ones. Furthermore, the vertical devices have larger power handling capability than the horizontal devices. The representative vertical device is the vertical FET or permeable base transistor (PBT) [1]. The PBT is accepted suitable for high power millimeter wave transistor because of low parasitics and compact structure. In this paper, the use of PBT in OEIC is proposed as a control device for high power laser diode. Figure 1 shows the proposed integration of PBT and laser diode. As shown in the figure, the optical device is placed on top of the PBT. The embedded electrodes control the current to the optical device. As a first step, the PBT has been fabricated by selective LPE. The fabrication and the result will be described.

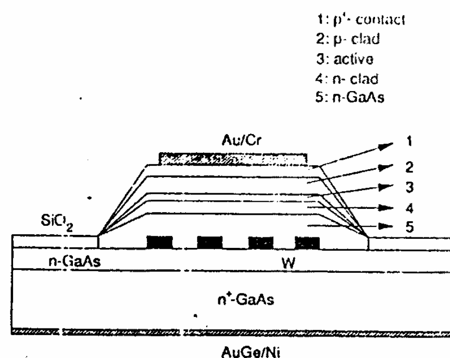

Fig. 1. Suggested vertical integraton scheme of a PBT and a laser diode.

2. EXPERIMENT AND RESULT

To fabricate the PBT, it is necessary to implement the embedded semiconductor-metal-semiconductor structure (SMS). The SMS structure is usually realized by MOCVD and MBE. Here, the selective LPE is used for the lateral growth of GaAs over the tungsten fingers in the SMS structure. This method has been used for the fabrication of the embedded metal-semiconductor- metal photodetector [2]. In the selective LPE, the metal grating for the GaAs overgrowth is surrounded by the masking material. The horizontal growth rate is increased because of the As flux in the melt from the masked region and the overgrowth is obtained [3]. Though it is known that W-GaAs junction is thermally stable up to the temperature of 800°C, the long thermal cycle during the LPE has deteriorated the junction property [4]. From an AES study, tungsten of 20nm thickness has shown the diffusion tail into GaAs up to 80nm after annealing at 800°C for

6hrs. The growth temperature has been reduced from 800°C to 750°C to minimize the interdiffuison of tungsten and GaAs. The schematic structure of the PBT fabricated by the selective LPE is shown in Fig. 2. The grating period of the tungsten was 3μm and the thickness was 100nm. To prevent the interaction between the Ga-melt and the tungsten, an additional SiO_2 layer over the tungsten was used. The tungsten was rf sputter deposited and the SiO_2 layer was in situ deposited just after the tungsten deposition. The SiO_2 region outside the active region served as a masked region for the lateral overgrowth. After the 2nd epitaxy at 750°C with the cooling rate of 0.2°C/min for 12min, AuGe/Ni ohmic contact was made. Figure 3 shows the current-voltage characteristics. The curve 1) in Fig. 3 a) is the current-voltage characteristics of the fabricated diode between source and gate and the curve 2) is that of the diode between drain and

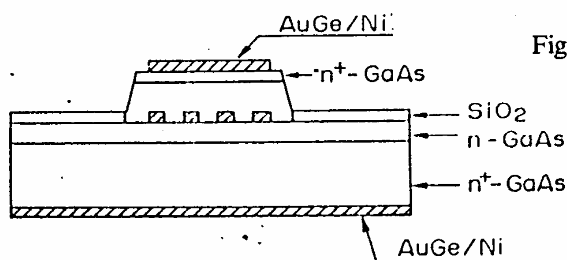

Fig. 2. Structure of the PBT by the SLPE.

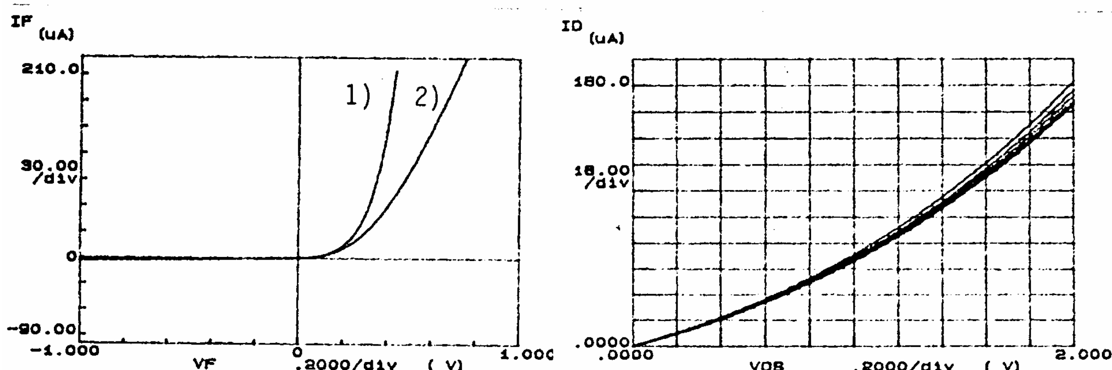

Fig. 3. a) Current-voltage characteristics of the diodes between source and gate 1), drain and gate 2), respectively.

b) Modulation characteristics of the PBT. (gate bias: -0.2V/step, start voltage : 0.0V)

gate. The drain-gate diode formed by the overgrown GaAs and the tungsten shows the increased series resistance. Fig. 3 b) shows the modulation characteristics of the fabricated transistor. The gate voltage is decreased from 0V to -1.0V by the step of 0.2V. Because of the large leakage current of the drain-gate diode, the slight modulation of I_{DS} has been obtained. The characteristics of the PBT will be improved by modifying the growth conditions and the electrode structure.

In conclusion, a vertical optoelectronic integrated circuit with the PBT is proposed. To increase the modulation depth, the diode characteristics should be improved.

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