Overview of Power/Ground Effects on Data Eye and Clock Jitter : from Board Resonance to Silicon Substrate Coupling

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Abstract

In high speed digital systems, clean clock signal and data signal are guaranteed by a clean power supply network. This paper shows how power supply network affects clock jitter and data eye pattern at each power hierarchy level, that is, board level, package level, on-chip level and silicon substrate coupling level. Especially, this paper shows what is the most dominant factors on data eye and clock jitter by observing relations of each power level coincidentally.

1. Introduction

It is well known that good design of a power supply network has a crucial role in implementing high speed data transmission systems. Accordingly, lots of research results already exist about power supply network design methods. However, most of them treat just one part of a total power supply network such as board power resonance problem, package parasitic inductance problem, and silicon substrate-coupling problem separately. Some of them are not dominant anymore when they are considered together or can even be useful although it is just a problem when considered separately.

This paper shows quantitative results of power/ground effects and relations from board resonance noise to silicon substrate-coupling noise through observing clock jitter, and data eye pattern.

2. Modeling of power supply network

Figure 1 shows the conceptual block diagram of a simulation model to evaluate power/ground effects. This model includes 10cm x 10cm board model using TLM(Transmission Line Matrix) method, off-chip decoupling capacitors, package pin RLC model, on-chip power line model, on-chip decoupling capacitors, and silicon substrate coupling model. With this power network model from board to chip, three kinds of circuit models are also included. 1) Transmitter/receiver model to observe data eye pattern. 2) Analog circuit (Delay Locked Loop) to observe clock jitter. 3) Digital circuit to generate digital power noise. The power/ground of analog and digital circuits is assumed to be shared on board, isolated on package, isolated on chip, and coupled through silicon substrate. All these models were designed and simulated using ADS(Advanced Design System).

Figure 2 shows some parts of this model in detail. TLM board model shown in Figure 2 (a) is valid to 2.5GHz and consists of 7.6mm unit cells. Impedance value of each cell is also shown in Fig 2(a). On-chip power lines are separated into three parts, that is, digital power, analog power, and I/O power, and all of them have enough on-chip decoupling capacitors. Figure 2 (b) shows on-chip digital power line model. Analog and I/O on-chip power lines have similar form except the number of package pins. In this model, 5, 1, and 5 power/ground pin pairs are assigned to digital, analog, I/O part respectively.

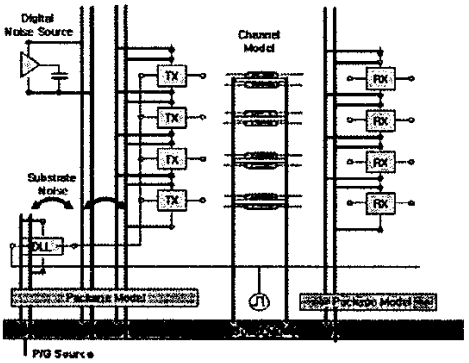


Fig. 1. Conceptual block diagram of simulation model

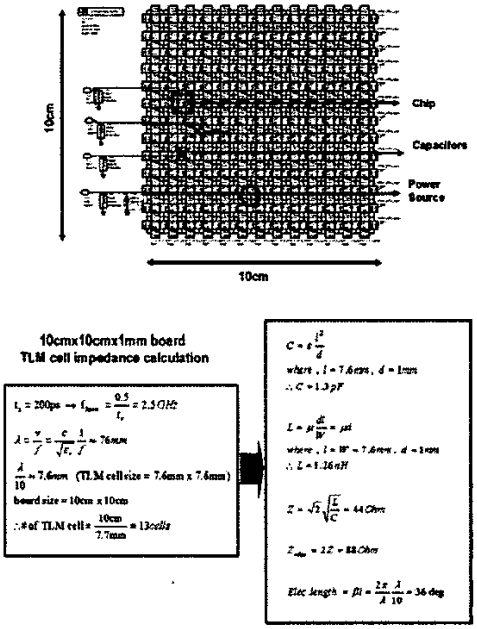


Fig. 2(a) 10cm x 10cm Board TLM Model

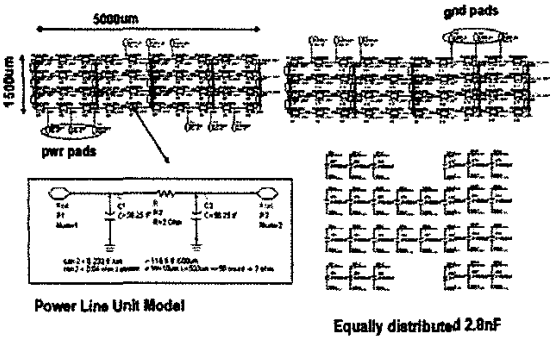


Fig. 2(b) On-chip digital power line model

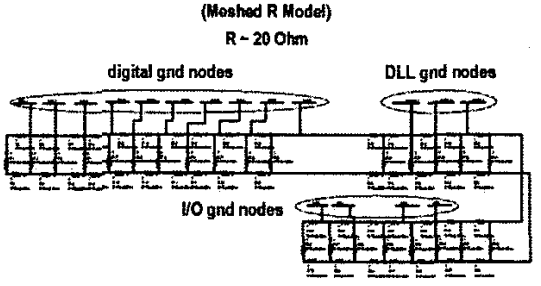


Fig. 2(c) Substrate coupling model

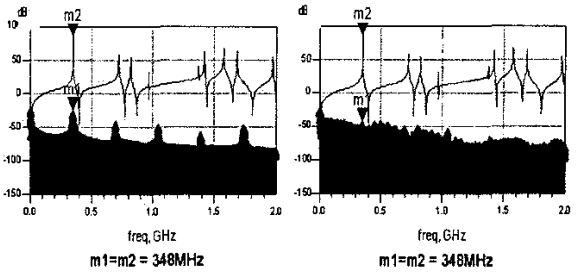
Fig. 2. Power Hierarchy Model

A few circuit models are used in this simulation model. All of them have as simple form as possible but enough to show proper results to evaluate power/ground effects. Variable delay line of a DLL consists of inverter chains which are controlled by charge pump output. To generate digital power noise, inverter chains consuming 200mA are used and CMOS inverter works as an I/O(transmitter) circuit. DLL and I/O circuits are connected to digital noise generation circuit through silicon substrate. Among many kinds of substrate coupling models, resistive mesh model is applied to this simulation. Figure 2 (c) shows the substrate coupling model.

To reduce simulation time, board TLM model was substituted by extracted S-parameters. This gives the same results with TLM circuit model. To observe skew generated by SSN, eight transmitters are used and all of them make the same transition except one transmitter. This kind of stimulus gives maximum skew.

3. Simulation Results

In this simulation, all effects of power/ground are observed at two points. One is transmitter data output for periodic/random stimulus and the other is DLL output clock. Figure 3 shows the impedance of the designed board and the current spectrum of operating circuits. Figure 3 (a) is for periodic stimulus and figure 3 (b) is for random stimulus. As shown in this figure, designed board has resonance frequency at 348MHz. This low frequency resonance is due to the power source and decoupling capacitors which make short nodes on the board. By meeting open end at the board edge, resonance point is generated at lower frequency than TM01 mode.



(a) (b)

Fig. 3. Circuit board resonance vs. signal current spectrum: (a) board impedance and current spectrum of periodic signal; (b) board impedance and current spectrum of random signal

If a periodic signal has the same frequency with the board resonance, board power noise is maximized and therefore it gives corrupted data output as shown in figure 4 (a). However, if a random signal is used as stimulus, there is no big difference independent of board resonance frequency as shown in figure 4 (b). This is because the random signal has spread current spectrum which has no specific current peak at the resonance frequency as shown in figure 3 (b). These results are under assumption that there are not on-chip decoupling capacitors at all. However, there are on-chip decoupling capacitors in real working chips. With the real working chips, that is, with enough on-chip capacitors, board resonance effects are dramatically reduced as shown in figure 4 (c). These results indicate that even though periodic signal has the same frequency with board resonance frequency, enough on-chip decoupling capacitors can cover that problem.

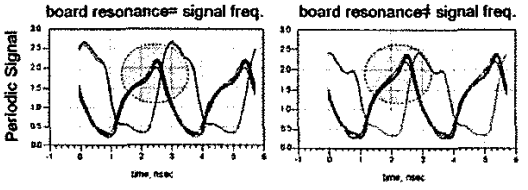


Fig. 4(a) board resonance effect on periodic signal

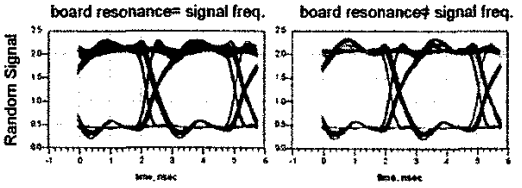


Fig. 4(b) board resonance effect on random signal

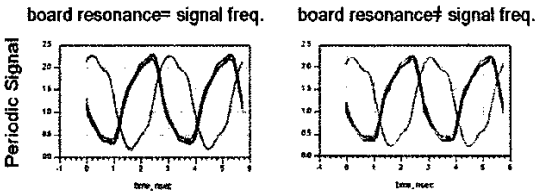


Fig. 4(c) board resonance effect on periodic signal with on-chip capacitors

Fig. 4. Relations of board resonance and on-chip decoupling capacitors

Figure 5 shows package inductance coupling effects on DLL output clock jitter. As shown in this figure, 10% coupling coefficient is endurable and this is not a dominant factor to make harm to the DLL output clock compared to substrate coupling noise that is shown below.

There is a quite interesting result about substrate coupling noise. That is, magnitude of digital power noise is decreased and that of analog and I/O power noise is increased by sharing their ground pins through substrate. Therefore better noise immunity is expected in digital circuit part. However, analog and I/O parts are damaged by substrate coupling and it is more critical.

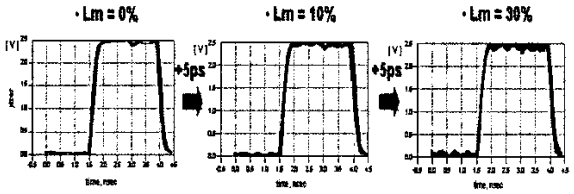


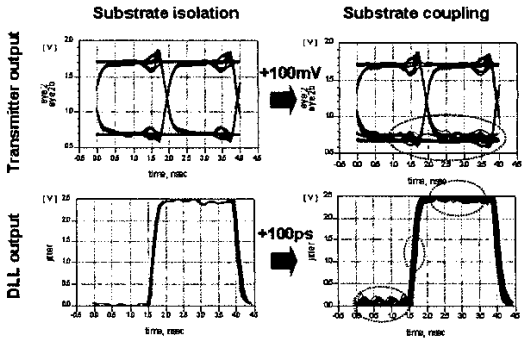
Fig. 5. Package inductance coupling effect on clock jitter

Figure 6 (a) shows that how substrate coupling noise hurts DLL clock jitter and transmitter random data output. In this simulation model, there was about 100ps increase in clock jitter and about 100mV additional noise in random data output by substrate coupling noise. However, substrate coupling problem can also be covered by on-chip decoupling capacitors as shown in figure 6 (b). Especially, on-chip decoupling capacitors for digital circuit part are more dominant because they reduce noise source itself.

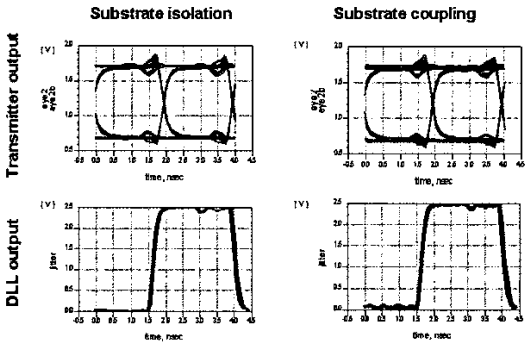
According to the results of this simulation, a partial solution only for a specific part such as a board, a package, on-chip can be meaningless without considering all of them at the same time.

4. Conclusions

In this paper, board power resonance, package inductance coupling, on-chip silicon substrate coupling problems and their relations were considered at the same time and the simulation results show that enough on-chip decoupling capacitors can reduce board resonance noise and silicon substrate coupling noise dramatically.



(a)



(b)

Fig. 6. Relations of substrate coupling noise and on-chip decoupling capacitors: (a) substrate coupling effects on periodic and random signal; (b) substrate coupling effects on periodic and random signal with on-chip decoupling capacitors

Acknowledgments

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