AIP Applied Physics Letters

Solid phase epitaxial growth of GaAs on Si substrates

K. I. Cho, W. K. Choo, S. C. Park, T. Nishinaga, and B.T. Lee

Citation: Appl. Phys. Lett. **56**, 448 (1990); doi: 10.1063/1.102761
View online: http://dx.doi.org/10.1063/1.102761
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v56/i5
Published by the American Institute of Physics.

Additional information on Appl. Phys. Lett.

Journal Homepage: http://apl.aip.org/
Journal Information: http://apl.aip.org/about/about_the_journal
Top downloads: http://apl.aip.org/features/most_downloaded
Information for Authors: http://apl.aip.org/authors

ADVERTISEMENT

Downloaded 16 Apr 2013 to 143.248.118.122. This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://apl.aip.org/about/rights_and_permissions

Solid phase epitaxial growth of GaAs on Si substrates

K. I. Cho, W. K. Choo, and S. C. Park
Korea Advanced Institute of Science and Technology, Seoul, and Electronics and Telecommunications Research Institute, Daejeon, Korea

T. Nishinaga and B.-T. Lee
The University of Tokyo, Tokyo, Japan, and Chonnam University, Kwangju, Korea

(Received 15 August 1989; accepted for publication 20 November 1989)

Thin films of GaAs on Si were grown by molecular beam epitaxy, which involves the solid phase epitaxial (SPE) growth of the amorphous GaAs buffer layer. A Rutherford backscattering minimum channeling yield of ~9.4% has been obtained for a 0.8-μm-thick GaAs film. Cross-sectional transmission electron micrographs and reflection high-energy electron diffraction results have revealed that misfit dislocations are mostly confined to what used to be the buffer layer of ~300 nm in thickness, and that the microtwins (and/or stacking faults) are mostly originated from the GaAs/Si interface and are generated during SPE growth.

GaAs layers grown on Si substrates provide a promising opportunity to combine the best features of Si and GaAs technologies. However, such thin-film growth has faced two major problems: antiphase domain disordering and 4% lattice mismatch between the Si and GaAs layers. Many studies have already been performed on this topic.[1] The most successful results have been obtained on a tilted substrate by the "two-step" process,[2] in which a thin GaAs buffer layer is deposited at lower temperatures (~300–400 °C) with the low growth rate (~0.1 μm/h) on Si substrates misoriented 2°–6° from the (001) orientation. Subsequently, the substrate is heated to ~580 °C and the main GaAs layer is deposited with a higher growth rate (~1 μm).

In this letter we report the characteristics of GaAs layers grown on Si (001) substrates by a molecular beam epitaxy (MBE) process, in which an amorphous GaAs buffer layer is deposited instead of a crystalline one, at low temperatures. We then let the amorphous film be crystallized by heating the substrate [i.e., a kind of solid phase epitaxy (SPE)]. This SPE growth technique is attracting increasing attention as a means to explore the growth mechanism involved and at the same time as a potential candidate for the low-temperature film growth process in semiconductor technology. It was previously reported that the SPE crystallization of implanted amorphous Si proceeded in a planar mode,[3] and that the initial stages of SPE growth of GaAs on Si preferably proceeded via a two-dimensional nucleation instead of a three-dimensional one.[4] It is therefore expected that a higher quality buffer layer can be obtained through the SPE method rather than through the conventional two-step growth method, because the defects due to coalescence of three-dimensional islands would not be incorporated.[5] Also, the mechanism of misfit dislocation introduction could be operating differently in the specimens prepared, respectively, by the conventional and SPE methods, because of the difference in growth mechanisms. In fact, the use of amorphous GaAs film as a buffer layer was previously attempted by Nishi *et al.*[6] in the growth of GaAs on Si, but the detailed analysis of the crystalline quality of the resultant films was not made yet.

Three kinds of Si (001) substrates were used in the present experiment: nontilted substrates and substrates tilted ~3°, respectively, towards the [110] and [100] directions. After the Si substrates were chemically cleaned by using a modified Ishizaka method,[7] they were immediately loaded into the MBE system and preheated to an elevated temperature above 850 °C in order to desorb silicon oxide on the substrate. Once a (2×1) reconstructed surface had been observed with reflection high-energy electron diffraction (RHEED), GaAs growth was undertaken using solid Ga and As sources. In the present modified two-step process, an amorphous GaAs film of about 12 nm in thickness first was deposited at a substrate temperature of 80 °C with an As_4/Ga flux ratio of ~17. In this case, we have found by x-ray photoelectron spectroscopy that the amorphous GaAs film has a composition of As/Ga$\simeq$1.7. Then the substrates were heated above ~400 °C while the RHEED pattern was being observed. After the crystallization of the amorphous phase, the main crystalline GaAs layer was grown at ~580 °C at the rate of 0.53 μm/h with an As_4/Ga flux ratio of ~4.

RHEED with a 20 keV electron beam, incident on the samples along the [110] azimuth direction at a glancing angle of a few degrees, was used for *in situ* monitoring of the surface structure during preheating and crystal growth. Figure 1 shows a series of RHEED patterns obtained during the growth of GaAs on (001) Si substrate tilted ~3° toward the [110] direction. When the GaAs films were deposited at ~80 °C on the (2×1) reconstructed Si substrates, the RHEED showed halo patterns [Fig. 1(a)] indicating that the buffer films were amorphous. As the amorphous samples were heated continuously with the heating rate of ~50 °C/min above 420 °C, diffraction spots as shown in Fig. 1(b) began to appear. Normally, two sets of diffraction patterns were observed during this crystallization step, one of which was the spots corresponding to the bulk GaAs crystal and the other was the much weaker twin spots. This result agrees with the work of Nishi *et al.*,[6] but disagrees with the work of Castagne *et al.*,[4] who reported that no twin pattern was observed in the SPE-grown GaAs on Si. This discrepancy may be ascribed to our higher deposition temperature and/or larger thickness of amorphous GaAs film. As the sample was

Downloaded 16 Apr 2013 to 143.248.118.122. This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://apl.aip.org/about/rights_and_permissions

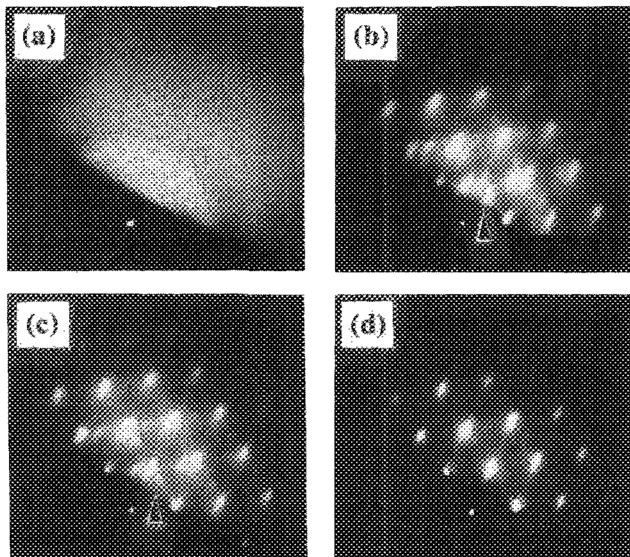

FIG. 1. Series of the RHEED patterns obtained during growth of GaAs on Si. (a) is a diffraction pattern of amorphous 12 nm buffer layer just after deposition at 80 °C, (b) and (c) are those of the buffer layer obtained after annealing the amorphous layers at 500 °C for 10 s and 580 °C for 9 min, respectively, and (d) is that of a 90-nm-thick GaAs film sequentially grown on the buffer layer at 580 °C. The arrows show two of the twin spots.

heated continuously until 580 °C, twin spots usually began to disappear and fundamental GaAs diffraction spots were elongated. The twin spots often disappeared before the streaking patterns appeared, but in some occasions they persisted even after the streaking patterns appeared. Even when the RHEED twin spots remained during heating alone, they soon disappeared after the main (second) GaAs layers were deposited on top of the buffer layer as shown in Figs. 1(c) and 1(d). As the main GaAs layer grew on the crystallized buffer GaAs layer continuously, the RHEED twin patterns [Fig. 1(c)] gave way to the usual streaking pattern [Fig. 1(d)] as in the case of the conventional MBE process. The other samples [Si (001) substrates nontilted and tilted ~3° towards the [100] directions] showed nearly the same RHEED characteristics as shown in Fig. 1, irrespective of substrate tilting.

We have used Rutherford backscattering (RBS) of 2.75 MeV $^{4}He^{+}$ ions in the channeling mode to check the crystal quality of GaAs films. Figure 2 shows the random and aligned RBS spectra for GaAs films grown on Si substrates. Sample A is a 0.8-μm-thick GaAs film on (001) Si substrates tilted 4° toward [100] direction growth by the modified two-step process, in which an amorphous buffer layer was annealed at 580 °C for 33 min. Sample B is a 0.7-μm-thick GaAs film grown by the direct method, in which the GaAs layer was grown at the conventional growth temperature of 580 °C, but with a slow growth rate of 0.25 μm/h and an As_4/Ga flux ratio of ~9. This RBS result shows that the films give the minimum channeling yields of ~9.4% (sample A) and ~9.2% (sample B) near the surface. Tsaur and Metze[8] have reported the minimum channeling yield of ~6% for a 0.9-μm-thick GaAs layer grown by the direct method (i.e., without the GaAs buffer layer). Varrio *et al.*[9] have reported RBS yield values of 7.3% and 3.8% for 0.48 and 1.06-μm-thick films, respectively, grown by the conventional two-step process. In terms of the minimum channeling yield, the crystalline quality of our films is somewhat poorer than that so far reported, and sample A grown by the modified two-step process has a poorer crystalline quality than sample B which is grown by the direct method. However, this difference is not so large and it is expected that the quality of our films (especially the film grown by the modified two-step process) would have been improved by proper control of the amorphous GaAs film thickness and by an appropriate heat treatment.[10]

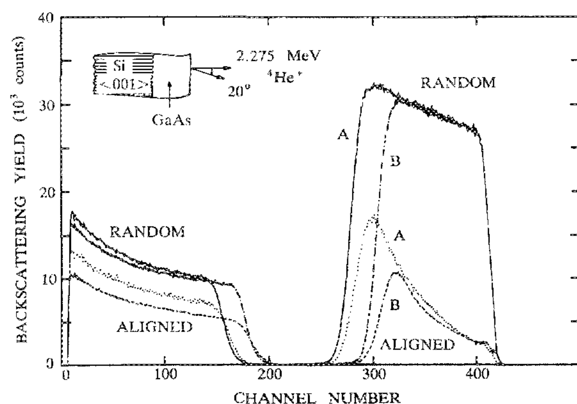

FIG. 2. Rutherford backscattering spectra for GaAs films grown by MBE on Si (001) substrates. Sample A is a 0.8-μm-thick GaAs film grown by the modified two-step process and sample B a 0.7-μm-thick GaAs film grown by the direct method.

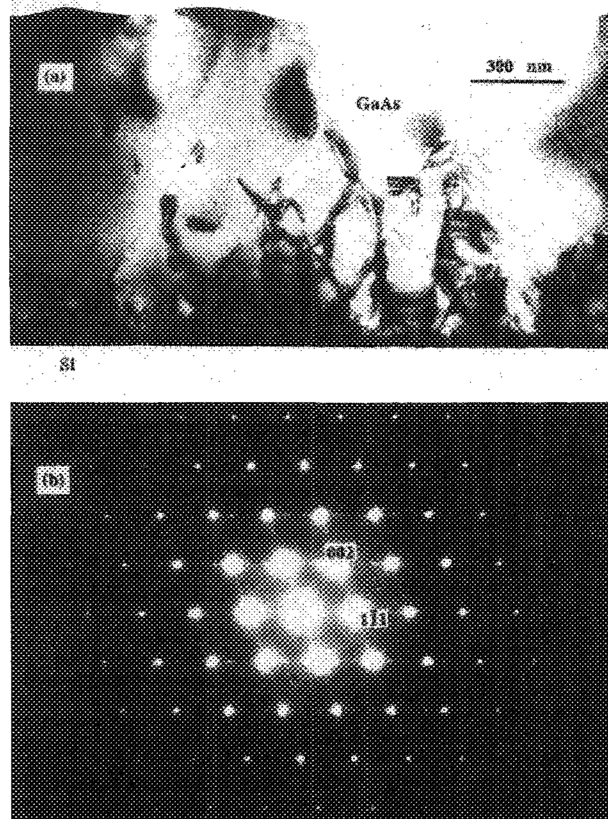

FIG. 3. Cross-sectional TEM bright field micrograph of GaAs/Si interface in [110] zone (a), and the corresponding diffraction pattern (b). The annealing of amorphous buffer layer was done at 580 °C for 17 min until the RHEED twin spots disappeared completely. The arrows show two of the twin spots.

Downloaded 16 Apr 2013 to 143.248.118.122. This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://apl.aip.org/about/rights_and_permissions

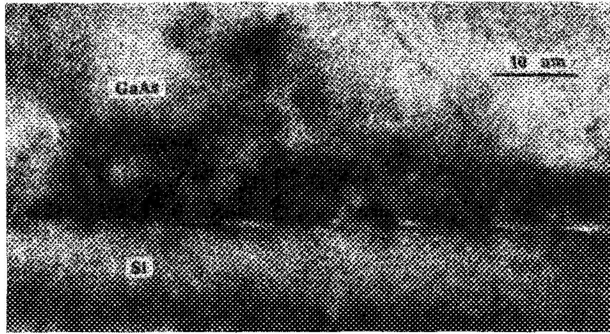

FIG. 4. High-resolution TEM micrograph of the same sample of Fig. 3, also [110] zone.

Figure 3(a) shows a cross-sectional transmission electron microscopy (TEM) micrograph around the interface in the [110] zone and the corresponding diffraction pattern (b) of a normal-GaAs($1\,\mu$m)/SPE-GaAs(12 nm)/Si structure grown by the modified two-step process. The lattice corresponding between Si and GaAs is apparent from the diffraction pattern of the GaAs/Si interface region. The inner set of diffraction spots is due to the GaAs film layer and the outer set to the Si matrix. The GaAs pattern shows streaks along the ⟨111⟩ and twin diffraction spots due to the presence of the stacking faults and/or microtwins. In the micrograph, dislocations and apparent edge-on microtwins (and/or stacking faults) are observed in the GaAs layer. In this GaAs/Si system, the amorphous GaAs buffer layer of 12 nm would be thick enough to accommodate the misfit strain due to the lattice mismatch between GaAs and Si.[11] In the micrograph, a rather high density of dislocations and microtwins is localized in the region near the GaAs/Si interface, the thickness of which is ~ 300 nm. Beyond this region, the GaAs layer becomes free of dislocations, but some twins still extend to the free surface. In the micrograph, microtwins are mostly originated from the GaAs/Si interface and are running from the interface to the bulk of the GaAs layer, with the angle of $\sim 54.7°$ with the interface. We also can see that most twins are virtually annihilated in the region near the free surface. It is reminded herein that the sample under the TEM observation is the one that was annealed at 580 °C for 17 min until most twin spots of the RHEED pattern disappeared. From the high-resolution TEM micrograph (Fig. 4) we have found that the dominant planar defects in the GaAs layers are the {111} microtwins that extend to the surface and the multiple stacking faults that are primarily localized near the interface.

In the present study, the quality and defects of GaAs MBE films grown on top of the amorphous GaAs buffer layer of Si (001) substrates have been compared with those prepared by other MBE methods. A RBS minimum channeling of $\sim 9.4\%$ has been obtained for a 0.8-μm-thick GaAs film. From the RHEED and TEM results it has been found that the microtwins are mostly originated from the GaAs/Si interface, and these twins are formed during SPE growth. Although most of the dislocations and twins are localized around the interface, some twins continue to grow to the free surface. The crystal quality in the vicinity of the free surface draws the immediate attention in the applications area. Therefore, to make SPE GaAs films on the Si substrate more useable, we need to devise a process to eliminate the microtwins that extend from the interface to the free surface.

[1]See, for example, *Materials Research Society Symposium Proceedings on Heteroepitaxy on Silicon*, edited by J. C. C. Fan and J. M. Poate (Materials Research Society, Pittsburgh, PA, 1986), Vol. 67, and references contained therein.

[2]R. Fischer, D. Neuman, H. Morkoç, C. Choi, and N. Otsuka, Appl. Phys. Lett. **48**, 1220 (1986).

[3]F. Priolo, J. L. Batstone, J. M. Poate, J. Linnros, D. C. Jacobson, and Michael O. Thompson, Appl. Phys. Lett. **52**, 1043 (1988).

[4]J. Castagne, C. Fontaine, E. Bedel, and A. Munoz-Yague, J. Appl. Phys. **64**, 2372 (1988).

[5]D. K. Biegelsen, F. A. Ponce, A. J. Smith, and J. C. Tramontana, *Materials Research Society Symposium Proceedings on Heteroepitaxy on Silicon*, edited by J. C. C. Fan and J. M. Poate (Materials Research Society, Pittsburgh, PA, 1986), Vol. 67, p. 45.

[6]S. Nishi, H. Inomata, M. Akiyama, Jpn. J. Appl. Phys. **24**, L391 (1985).

[7]A. Ishizaka and Y. Shiraki, J. Electrochem. Soc. **133**, 666 (1986).

[8]B.-Y. Tsaur and G. M. Metze, Appl. Phys. Lett. **45**, 535 (1984).

[9]J. Varrio, H. Asonen, A. Salokatve, and M. Pessa, Appl. Phys. Lett. **51**, 1801 (1987).

[10]See, for example, H. Okamoto, Y. Watanabe, Y. Kadota, and Y. Ohmachi, Jpn. J. Appl. Phys. **26**, L1950 (1987).

[11]See, for example, P. M. J. Maree, J. C. Barbour, J. F. van der Veen, K. L. Kavanagh, C. W. T. Bulle-Lieuwma, and M. P. A. Viegers, J. Appl. Phys. **62**, 4413 (1987).

Downloaded 16 Apr 2013 to 143.248.118.122. This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://apl.aip.org/about/rights_and_permissions