FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering

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Abstract

Process refinements to improve the performance of FinFETs are described. Hydrogen annealing is shown to provide high surface quality on etched fin sidewalls for improved drive current and noise performance. Appropriate V_t is achieved in lightly doped p-channel FinFETs using Molybdenum (Mo) as the gate-electrode material for the first time. Multiple values of V_t are achieved via gate work function engineering by selective implantation of Mo.

Introduction

The FinFET offers the superior scalability of a double-gate MOSFET structure together with a process flow and layout similar to that of the conventional MOSFET. Hence, it has been investigated recently by several groups [1-3]. In order for a CMOS FinFET technology to provide maximum performance benefit over bulk-Si CMOS technology, various issues must be resolved. These include the formation of Si fins with high surface quality for high carrier mobilities, and the development of a tunable-work-function gate technology for threshold-voltage (V_t) control.

In this work, the effect of hydrogen annealing after fin patterning on device performance is studied. During the anneal in a pure hydrogen ambient, the surface (*vs.* bulk) silicon migration rate is enhanced [4]. Thus, line edge roughness caused by lithography and sidewall surface roughness caused by reactive-ion etching are reduced.

Ideally, the FinFET body should be lightly doped in order to achieve high carrier mobility for high transistor drive current, as well as immunity to dopant-fluctuation-induced variations in V_t. A major technological challenge, then, is V_t adjustment by gate work-function engineering. The required range of gate work functions for a fully-depleted CMOS FinFET technology is 4.4-5.0V [5], which precludes poly-Si as a gate material. Molybdenum (Mo) has a high work function (~5V), which makes it suitable as a gate material for p-channel FinFETs. It has been reported that nitrogen implantation into Mo films followed by thermal annealing can be used to controllably lower the Mo gate work function to values as low as 4.4V [6], to make it suitable for n-channel FinFET application as well. In this work, Mo gate technology is applied for the first time to p-channel FinFETs. The capability to achieve multiple V_t values (for high-performance *vs.* low-power applications) by selective high-dose nitrogen implantation is demonstrated.

Device Fabrication and Characterization

In this work, FinFETs were fabricated with either *in-situ*-doped poly-Si or Mo capped with *in-situ*-doped poly-Si as the gate material, using a process similar to that described in [1] and [7]. The Si fins (with (110) surface orientation) were patterned by lithography and reactive-ion etch (RIE) processes, resulting in sidewall roughness (line-edge roughness) from the lithography and damage from the RIE.

A. Hydrogen annealing study

Pure hydrogen annealing was performed on selected samples after the fin etch, before the sacrificial oxidation step, in an ASM Epsilon II single-wafer Epitaxial Reactor at 1 atm pressure and 900°C for 5 min. Poly-Si test structures were used to determine the optimal annealing temperature. After the hydrogen anneal, the surface roughness was verified to be significantly improved (Fig. 1) due to the high surface Si migration rate. Poly-Si-gated hydrogen-annealed FinFETs show higher on-state current and lower off-state current, as well as lower $|V_t|$ due to reduced trap density (Fig. 2). The electron mobility is more sensitive to surface roughness than the hole mobility, because the inversion-charge centroid for electrons is closer to the Si-SiO_2 interface than for holes [7]. Thus, at high gate voltages, the NMOS drive current is degraded more severely (29% *vs.* 19%) by surface roughness than the PMOS drive current (Fig. 3).

The mobility degradation due to surface roughness can be derived as follows. When the interface in a region of the channel is shifted by Δ from its average position, the average potential seen by the inversion-layer charge is changed by $\delta V = E_{eff}\Delta$, where E_{eff} is the average transverse electric field [8]. The scattering rate is proportional to the square of the perturbing potential, according to Fermi's Golden Rule. Thus, mobility degradation due to surface roughness scattering is represented by $\mu_{SR} \propto (E_{eff}\,\Delta)^{-2}$, where Δ is the root-mean-square value of surface roughness [9]. For a lightly doped channel, $E_{eff} \cong \eta Q_{inv}/\varepsilon_{Si} = \eta C_{ox}(V_g - V_t)/\varepsilon_{Si}$, where $\eta = 0.5$ for an NMOS device and $\eta \cong 0.33$ for a PMOS device [10]. Mobility degradation by surface roughness scattering is severe for large Δ and increases with increasing gate bias.

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To investigate the quality of the Si-SiO_2 interface, low-frequency noise was measured over the range from 1 Hz to 10 kHz with a BTA 9812B standard noise analyzer at room temperature. Output drain current noise (S_I) was normalized by the transconductance (g_m) to obtain the equivalent gate voltage noise $S_{VG} = S_I / g_m^2$. Fig. 4 and Fig. 5 show that hydrogen annealing provides for lower S_{VG} in both NMOS and PMOS devices, respectively. At low current levels (weak inversion regime) the noise characteristic is flat, and is attributed to carrier-number fluctuations due to traps at the Si-SiO_2 interface. At high current levels (strong inversion regime) the noise increases quadratically, and is attributed to mobility fluctuations. The noise level and dependence on the drain current are comparable and similar for the poly-Si-gated hydrogen-annealed FinFETs as for bulk-Si MOSFETs [11]. Therefore, the hydrogen annealing process is effective for achieving high-surface-quality fins.

Relatively high PMOS and low NMOS drive currents for FinFETs as compared to bulk-Si MOSFETs have been reported [1]. This is expected because of the anisotropy of carrier mobilities in silicon [12]. It is known that hole mobility is enhanced, while electron mobility is degraded, for a (110) surface as compared to a (100) surface in Si. The field-effect mobilities for holes and electrons were extracted from FinFET C_g-V_g and I_{ds}-V_{gs} measurements, and are plotted in Fig. 6 and Fig. 7, respectively. The hole mobility surpasses the universal mobility curve for (100) bulk-Si PMOSFETs (Fig. 6). However, the electron mobility is lower than the universal curve for (100) bulk-Si NMOSFETs (Fig. 7). These results are expected, and are consistent with the previous report of FinFET g_m dependence on crystal orientation [2].

B. Molybdenum gate technology demonstration

In order to demonstrate the capability for a multiple-V_t technology, Mo-gated PMOS FinFETs were fabricated as follows. After gate oxidation, 40 nm of Mo was sputter deposited at 200°C using a DC-magnetron system (10^{-7} Torr base pressure). The Mo was then capped with 45 nm of *in-situ* doped (n-type) poly-Si, deposited by LPCVD. The purpose of the poly-Si was to prevent oxidation of Mo during the subsequent removal of photoresist (used to selectively mask the nitrogen implant) in an oxygen plasma. The poly-Si also helped to reduce ion channeling during the nitrogen implantation. 20 keV $^{14}N^+$ was selectively implanted at a tilt angle (60°) on both sides of the Si fins, as shown in Fig. 8 (gate layer not shown, for clarity). The nitrogen dose was split to $5.0x10^{15}$ cm^{-2} and $1.0x10^{16}$ cm^{-2}. Afterwards, an additional 0.6 μm of *in-situ* doped poly-Si was deposited, and the gate was planarized by CMP (Fig. 9). Fig. 10 is a scanning electron micrograph which shows that the Mo was successfully etched (in a Cl_2 + O_2 plasma, with 70:1 etch selectivity to SiO_2) without any residue or stringers. Gate-sidewall spacers were then formed and source/drain ion implantation was performed. The implanted dopants (boron) were activated by RTA at 900°C for 1 min. This anneal also served to diffuse the imlplanted nitrogen to the Mo-SiO_2 interface, to effect a change in the gate work function. Device fabrication was completed with a 30-min. forming gas anneal at 400°C. Note that hydrogen annealing was not employed for the devices in this demonstration.

Fig. 11, 12 and 13 are cross-sectional transmission electron micrographs of a 10 nm-wide Si fin with 20 nm-thick Mo gate at the sidewalls. An unimplanted Mo-gated PMOS FinFET shows –0.2V V_t (defined at 100nA/μm I_{ds}). Nitrogen-implanted Mo-gated devices exhibit a V_t which is shifted in the negative direction, with $|\Delta V_t|$ increasing with implant dosage (Fig. 14). This V_t shift is also observed in C_g-V_g measurements made on a multiple-fin device (Fig. 15). It should be noted that no special post-nitrogen-implant annealing step was performed in this study, and that larger V_t shifts can be attained by adding such a step, as well as by using higher implant doses [6]. These would be needed in order to achieve the low gate work function values required for NMOS devices. Fig. 16 shows the output characteristics of a Mo-gated PMOS FinFET. The drain current was found to be limited by parasitic series resistance for this initial study. (Neither raised-source/drain nor silicidation processes were used.)

Summary

Process refinements to improve the performance of FinFETs are described. Hydrogen annealing is shown to provide high surface quality on etched fin sidewalls for improved drive current and noise performance. Appropriate V_t is achieved in lightly doped, high-mobility p-channel FinFETs using Mo as the gate-electrode material, for the first time. The work function of Mo can be engineered by selective implantation of nitrogen, to attain multiple values of V_t (*e.g.* for high-performance *vs.* low-power applications) on a single chip. This technique can be used to achieve the low gate work function needed for n-channel FinFETs, so that Mo is an attractive candidate for single-metal, dual-work-function gate technology for CMOS FinFETs.

Acknowledgements

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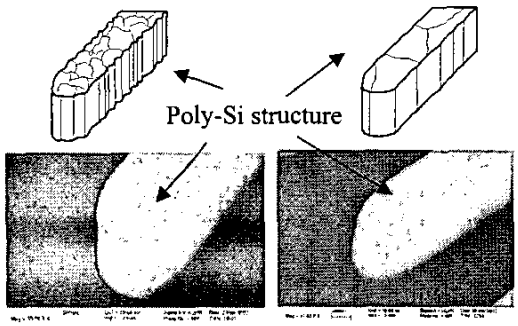

(a) Before annealing (b) After annealing (100% H_2,900°C,5min)

Fig.1 SEM photographs of poly-Si structures before hydrogen annealing (a) and after hydrogen annealing (b). Grain roughness on the top and line edge roughness at the sidewall are smoothed by hydrogen annealing.

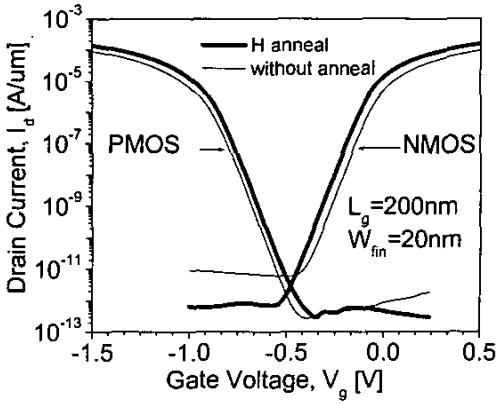

Fig. 2. I_d-V_g characteristics of FinFETs. NMOS and PMOS V_t are lowered and both drive currents are increased with hydrogen annealing (N+ poly-Si gate).

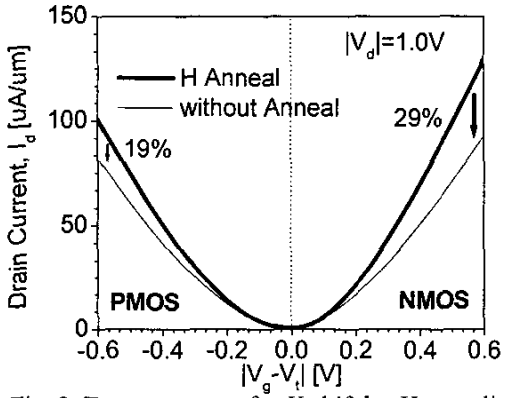

Fig. 3. To compensate for V_t shift by H annealing, $|V_g-V_t|$ is plotted on the x-axis. It shows NMOS drive current is more sensitive to sidewall roughness than PMOS current (N+ poly-Si gate).

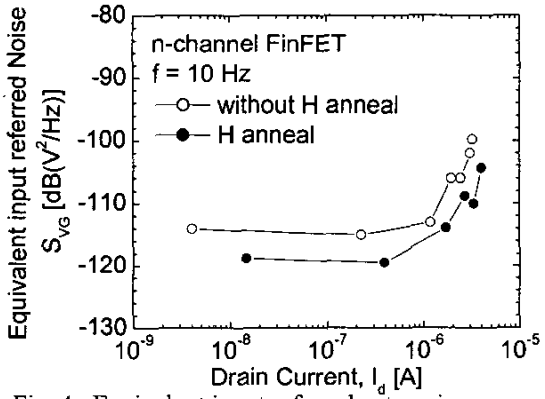

Fig. 4. Equivalent input referred gate noise power as a function of drain current in NMOS FinFET. Hydrogen annealing results in lower noise.

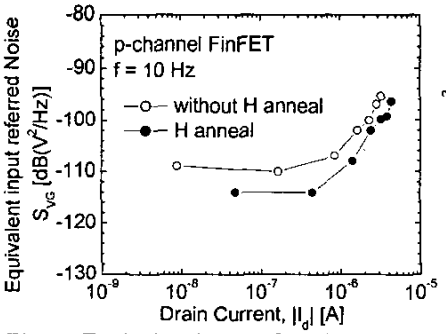

Fig. 5. Equivalent input referred gate noise power as a function of drain current in PMOS FinFET. Hydrogen annealing results in lower noise.

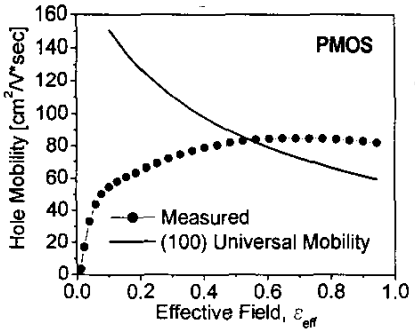

Fig. 6. Hole mobility of FinFETs. Measured mobility of holes is higher for (110) sidewall Si than for (100) plane bulk-Si.

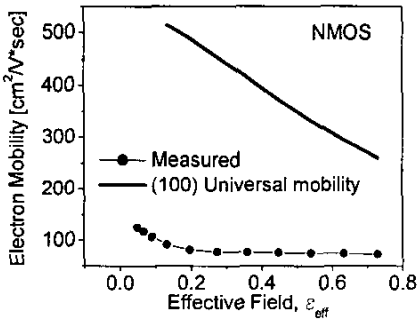

Fig. 7. Electron mobility of FinFETs. Measured mobility of electrons is lower for (110) sidewall Si than for (100) plane bulk-Si.

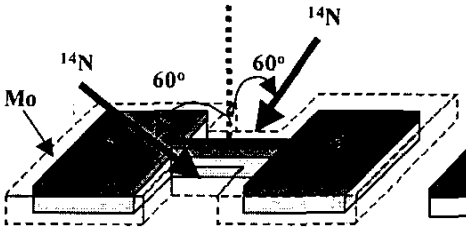

Fig. 8. Schematic of nitrogen implantation with 60° tilt into Mo-gate at both sides of fin.

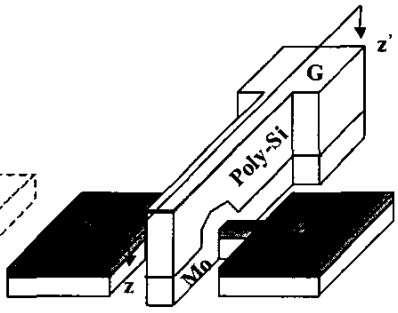

Fig. 9. Schematic of a FinFET with planarized poly-Si and Mo-gate.

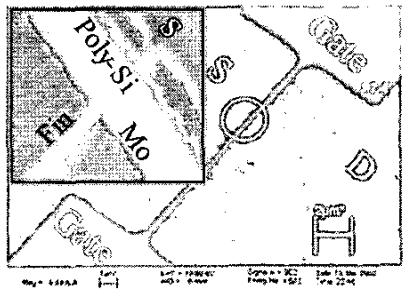

Fig. 10. Tilted SEM view of Mo-gate FinFETs. Mo-gate was etched by Cl_2 and O_2 plasma without residues and stringers.

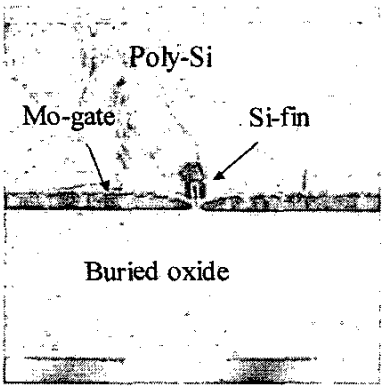

Fig. 11. Cross-sectional TEM photograph along z-z' direction in Fig. 9 shows a 40nm Mo-gate with a planarized 400nm cap poly-Si by CMP.

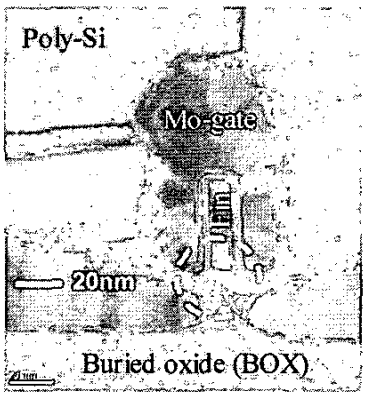

Fig. 12. Close-up of Fig. 11.

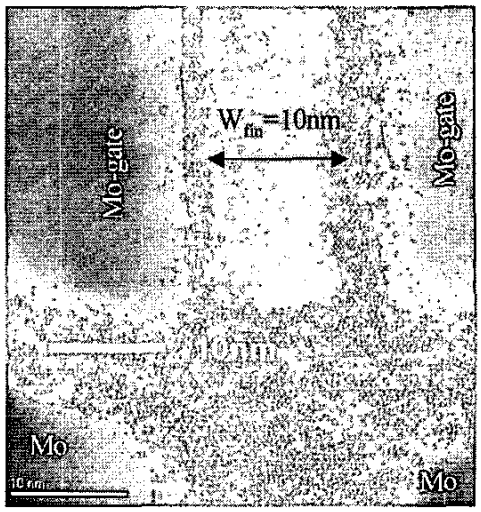

Fig. 13. Close-up of circle in Fig. 12. Fin width is 10nm. PVD Mo is discontinuous due to a undercut of buried oxide, which is caused by over-etching of sacrificial oxide with HF.

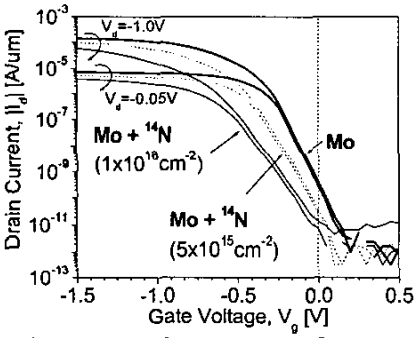

Fig. 14. I_d-V_g characteristics of *Mo*-gate FinFETs (L_g=*80nm*, W_{fin}=*10nm*). *−0.2V* threshold voltage at 100nA/μm is achieved without body doping with pure PVD Mo-gate. Multiple threshold voltages are demonstrated by nitrogen implantation for a change of gate work function.

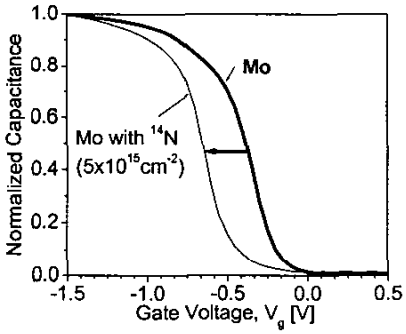

Fig. 15. C_g-V_g characteristics of *Mo*-gate FinFETs. Capacitance was measured for L_g=*50μm*, W_{fin}=*16nm*, and *18* fins of large transistors. The gate work function is changed by nitrogen implantation (*20keV*, 5x10^{15}cm^{-2}, 60°, both sides) and ΔV_t is *0.3V*.

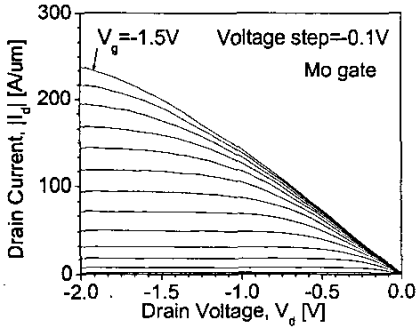

Fig. 16. I_d-V_d characteristics of *Mo*-gate FinFETs (L_g=*80nm*, W_{fin}=*10nm*). No raised S/D process and metallization were used in this experiment. Due to the high parasitic series resistance, drive current is not high.