A Miniaturized K- Band Balanced Frequency Doubler Using GaAs/InGaP HBT Technology

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***Abstract* — A K band balanced frequency doubler using InGaP HBTs is presented, which features high conversion gain, wide bandwidth and high rejection of fundamental signal. To obtain the balanced signal, a differential amplifier with a base-collector feedback resistor is utilized. The push–pull doubler operates in a near class B region for good efficiency. This circuit has a conversion gain of 6dB over the output frequencies from 14Ghz to 24Ghz. The fundamental frequency suppression is better than 17dB. The MMIC chip size is 0.6 X 0.7 mm^2.**

***Index Terms* — Frequency doubler, MMIC, balanced topology, HBT, Frequency multiplier**

I. INTRODUCTION

Frequency doublers are widely used to achieve high frequency sources with low phase noise. Active frequency doublers provide conversion gain over broadband frequencies and require small input power. The high frequency doublers have been realized using GaAs MESFET or HEMT. FET doublers have good isolation between input and output terminals. Due to the square law relation, the FET doublers are an attractive feature for generating second harmonic signals.[1] However, HBT devices exhibit lower phase noise and higher order harmonic generation than FET devices.[2] The balanced frequency doubler using FET have provided conversion loss or small gain. [3,4]. To enhance conversion gain, it is necessary to use high f_T device. Recently, GaAs HBTs are popular microwave or millimeter MMIC circuits. HBT frequency doubler could be integrated with VCOs or frequency synthesizer, which is based on HBT technology. A frequency multipliers using HBT were recently reported.[2,5,6] . But most of the circuits operate low frequency range. The X band doubler did not have good fundamental suppressions and exists some resonances. [7]

This paper presents balanced frequency doubler using InGaP HBT which has high conversion gain at K band, wide bandwidth, and high fundamental suppression. InGaP HBT has a measured f_T of approximately 60GHz. Circuit measures 0.6 x 0.7 mm^2.

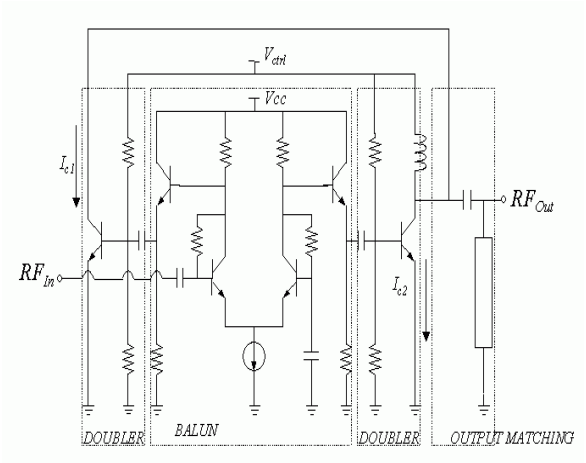


Fig. 1. Frequency doubler circuit schematic

II. CIRCUIT DESIGN

The frequency doubler is based on Knowledge*on InGaP HBT Technology with an f_T of 60GHz and fmax of 75Ghz. As shown in the schematic of the MMIC doubler in Fig. 1, The circuit comprises a differential amplifier which provides 180 phase shift, buffer amplifiers, and push - pull doubler cores which operate at near class B region. It is analyzed and designed using harmonic balance simulator.

The differential amplifier with base-collector feedback resistor provides broadband amplification and easy biasing and can avoid stability problems. The doubler cores are accomplished by setting the bias of the class B mode. This stage generates as much power at the second harmonic as possible and low dc currents. Their biasing is controlled by adjustable dc power supply to find optimum bias point. At the output load, the odd harmonics are 180 degrees out of phase and cancelled at the output port. The even harmonics at the output load are in phase and added in power. The current from each device at the output load are similar to the equation given by (1) and (2) [8]

$$I_{C1} = \frac{I_{max}}{\pi} + \frac{I_{max}}{2}\cos(\omega t) + \frac{2I_{max}}{3\pi}\cos(2\omega t) + \cdots \quad \cdots(1)$$

$$I_{C2} = \frac{I_{max}}{\pi} + \frac{I_{max}}{2}\cos(\omega t + \pi) + \frac{2I_{max}}{3\pi}\cos(2\omega t + 2\pi) + \cdots \quad \cdots(2)$$

It is difficult to show the each collector current because each collector is tied to output load. The collector current waveform is similar to the emitter current wave form. Figure 2 shows the each emitter current wave of the doubler core transistor. A 180 degree phase shift between each waveform is seen. Therefore one can obtain full-wave rectifier.

A short circuit at the fundamental frequency provides maximum conversion gain. It is necessary to find the

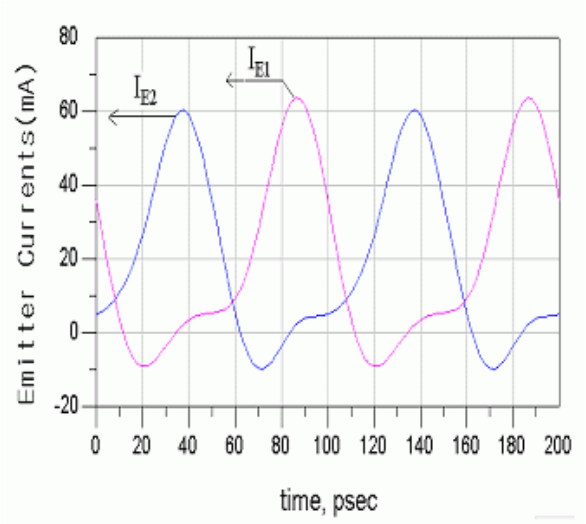


Fig. 2. . Simulated emitter currents of the double stage

optimum load impedance at the second harmonic frequency for the high conversion gain and to guarantee the stability of the doubler. The stability of the doubler was analyzed by means of studying input impedance Zin. The resistor part of Zin has to be positive. The harmonic load impedance Zn is then calculated from

$$Z_n = \frac{U_n}{I_n}$$

Where Un is the n_{th} harmonic load voltage and In is the n_{th} harmonic load current. [9,10]

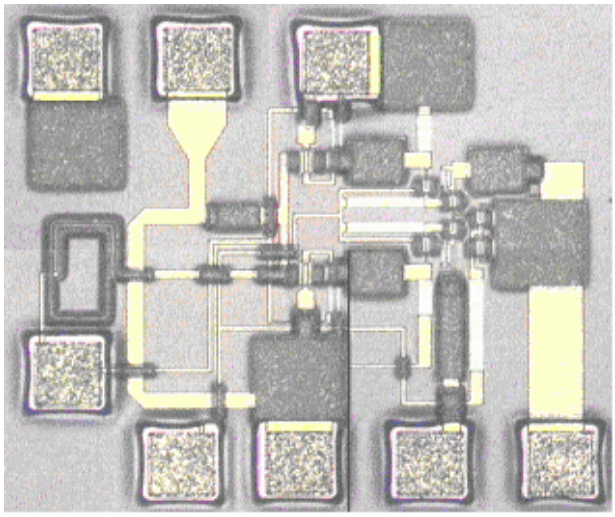


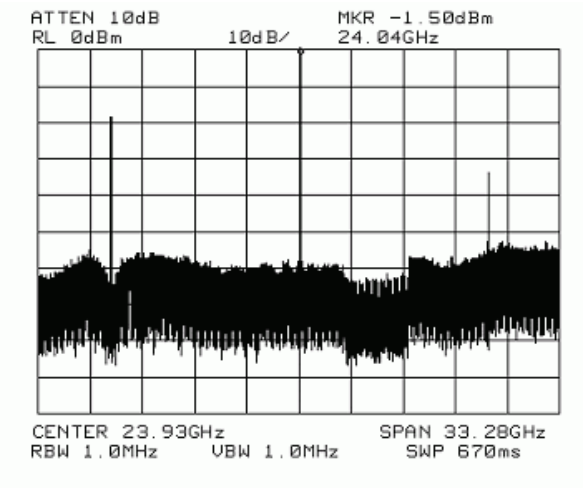
Fig. 3. Microphotograph of the balanced frequency doubler .

Input matching networks consist of MIM series capacitor and differential amplifier feedback resistors. Theses resistors can control input impedance of the differential amplifier. The input impedance is controlled by series capacitor and feedback resistors. The output matching networks consist of MIM series capacitor and short–circuited stub. They have a high pass filter characteristic and the optimum load impedance.

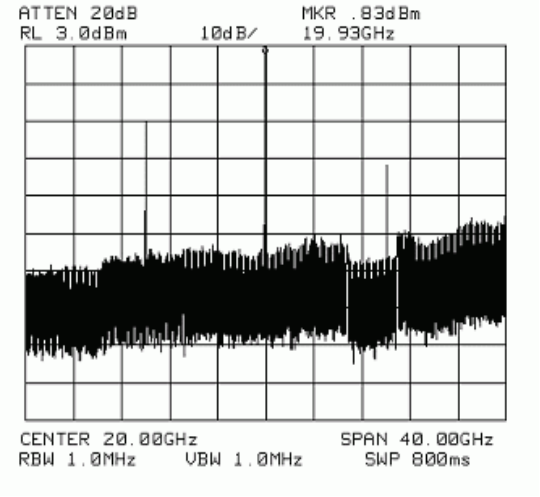
III. EXPERIMENTAL RESULTS

The doubler chip size is 0.6 x 0.7 mm^2 and shown in Figure 3. The doubler is measured using on-wafer probing system. 8 bonding pads are used for on-wafer probing and bias lines. The circuit was biased with 5V collector-to-emitter voltage on the both differential amplifier and buffer amplifier. The optimum base voltage of the doubler stage is found be 1.2V. The optimum bias point is sensitive to the base bias voltage. The total DC power consumption was approximately 200mW. The input CW signal was provided by an HP83712B signal generator. The fundamental and second harmonic was measured using HP 8564E spectrum analyzer. The losses of cables and probes are measured by a power meter.

In Figure 4, measured spectrum indicates the doubler exhibits 7.5 dB conversion gain and 17 dB fundamental suppression with –5dBm input power at 12 GHz. The fundamental frequency suppression at 10Ghz input is approximately 20dB.



(a)



(b)

Fig 4. The harmonic characteristics of frequency doubler with (a) 24Ghz output (b) 20Ghz output frequency , input power is - 5dBm

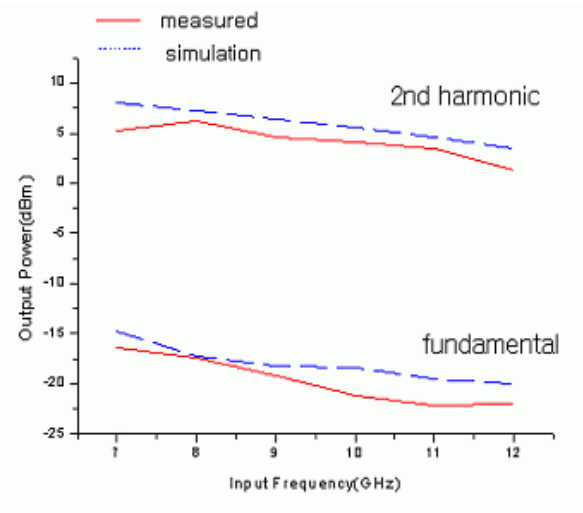


Fig. 5 measured and simulated doubler output power Versus frequency. Input power is –5dBm

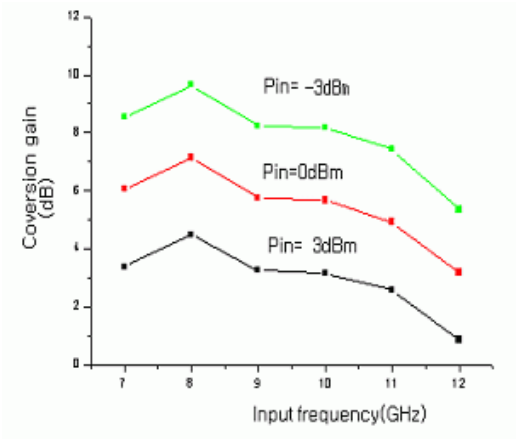


Fig. 6. Measured doubler conversion gain versus frequency with different input powers

The figure 5 shows the measured and simulated output power as a function of input frequency for –5dBm input power. There are some differences between simulation and measured data due to cable and probe tip loss. The averaged conversion gain is 10dB and the suppression of fundamental frequency is better than 17dBc from 7Ghz to 14Ghz input frequencies.

The figure 6 shows the measured conversion gain versus frequency with various input powers. The conversion gain is 6 to 9 dB with the –3dBm input power. As the input power increases, the conversion gain decreases because of output power saturations.

IV. CONCLUSIONS

The miniaturized K band frequency doubler using InGaP HBT was designed and tested . The circuit size is as small as 0.6 x 0.7 mm^2. Despite of the small area, the doubler has over 6dB conversion gain and the 3-dB bandwidth is between 14GHz and 24Ghz output. The fundamental frequency suppression is better than 17dB.

V. ACKNOWLEDGEMENT

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