SDL8.5 Fabrication of Top Electrode Front Surface Emitting Laser Diode (FSELD) Using HBT Process

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Surface emitting laser diodes are of interest for optoelectronic integrated circuits because they can be fabricated using planar technology which makes it possible to fabricate two-dimensional array and new functional devices. Recently, there have been several reports of low threshold current operation using vertical cavity surface emitting laser diodes comprising a quantum well active region, high reflectance mirrors and tight current confinement.[ref.1]

In this talk we will discuss the process compatibility between HBT's[ref. 2] and VC-SELD in order to study its optoelectronic integrated circuit and optical computing applications. In addition, we will demonstrate succesful fabrication of a new SELD in which both the p-electrode and n-electrode, of the laser diode, are placed on the top surface and the total step height of the device is less than 1μm. It has a low series resistance and the potential advantage of less absorption because the multilayer semiconductor mirror can be undoped. Its laser light emits from the front surface leading to the possibility of having emission wavelength that are not restricted by the bandgap of the substrate. If a semi-insulating wafer is used as the substrate, device isolation can be easily obtained without deep groove etching.

The semiconductor layers that were used to form the top electrode FSELD[ref.3] were grown by MBE and comprised a stack of AlAs/GaAs bottom DBR mirrors doped n-type, an AlGaAs lower cavity layer, an InGaAs strained quantum well active region, an AlGaAs upper cavity layer and a p-type GaAs/AlAs top DBR mirror. The top electrode FSELD was fabricated by performing a double ion implant into the device epi-layer that was patterned with 25μm diameter dots of a Si/Al_2O_3 dielectric stack using the emitter mask of an HBT. The dielectric stack initially functions as the implant mask but will eventually act as the top DBR mirror. An O^+-implant was first perfomed to create a buried insulating layer. Following this, a heavy Be-implant was undertaken to form a low resistance p-ohmic side contact to the active region. The p-electrode was patterned using the base mask. After revealing n-DBR layers by wet chemical etching, Ni/Ge/Au/Ag/Au was deposited on the n-DBR layers to make an n-ohmic contact.

The top electrode FSELD had a current/voltage characteristic that showed significantly less series resistance than a device fabricated from the same wafer having both top and bottom semiconductor mirror/contact stacks. In addition, the threshold current of the top electrode FSELD was 6mA for a 25μm diameter device which compares favorably with the mesa etched SELD that had a threshold current of 15mA.The top electrode FSELD had an emission wavelength of 971nm and a spectral width above threshold of 5Å. Only single mode operation was observed because the mode spacing is large in these short cavity lasers.

The top electrode FSELD has a low operating voltage, small series resistance and low threshold current. In addition, since both the n-electrode and p-electrode are on the top surface of the wafer and the total step height of the device is relatively low, this structure is attractive for optoelectronic integrated circuit applications.

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