Differential HBT Power Cell and its Model Parameter Extractions

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A class-B push-pull power amplifier offers high PAE, linear operation, and a larger impedance transformation ratio than parallel in-phase combining [1]. The ground-bouncing effect caused by the parasitic components is very small in a differential amplifier. It results in gain boosting and high immunity against bond-wire variations. Also, it gives less injection of common mode noise into a substrate. Due to the symmetry in the circuit, there is an additional benefit that even harmonics are suppressed at a load, easing the task of filtering the output. HBTs showed a thermal runaway due to the positive feedback effect between the current and the junction temperature [2]. The current is crowded at a small hot region at which the transistor becomes destroyed. To avoid this phenomenon, ballast resistors are inserted in each emitter and base as shown in Fig. 1(a), and the resistors cause negative feedback effects and the thermal runaway is prevented. Evidently, this approach degraded the HBT properties. Another method is differentiating the ac path and the dc bias path by introducing capacitors as shown in Fig. 1(b) [3]. Since the capacitors cannot be large enough due to limit of chip area, the bandwidth of the power cell is limited.

A proposed differential power cell solves the problems. The ballast resistors are inserted in the common emitter as shown in Fig. 2. Then, the ballast resistors don't degrade the gain even with additional bond-wire inductors. Besides, broadband operation can be achieved because there are no additional capacitors. The differential power cell was fabricated using InGaP/GaAs HBT process in Fig. 3. The 64-finger $2\times20\text{-}\mu m^2$ device is expected to reach the peak output power of 29 dBm at 1.95 GHz. The multi-finger device needs a large-signal model including self-heating effect and parasitics for accurate simulation. Fig. 4 illustrates the proposed patterns for the model extraction. Gummel-Poon model parameters including self-heating and ambient temperature effects are extracted from measured I-V data and Gummel plots of the common mode pattern in Fig. 4(a) at various ambient temperatures [4]. Junction capacitance and parasitic parameters are extracted from S-parameters measured from the half circuit pattern, which is shown in Fig. 4(b), at cutoff and offset bias conditions [5]. The complete model is obtained by combining two kinds of extractions. Finally, differential S-parameter measurement of the differential power cell can be achieved using a 4-port network analyzer and it helps to extract exact emitter ballast resistance and to verify the complete model.

The differential power cell has a number of advantages, such as high gain, high efficiency, small ground-bouncing effect, and less injection of common mode noise. Also, using the proposed extraction pattern, a complete model including thermal effects can be achieved. The concept of the differential power cell can be applied to the any other bipolar power transistors.

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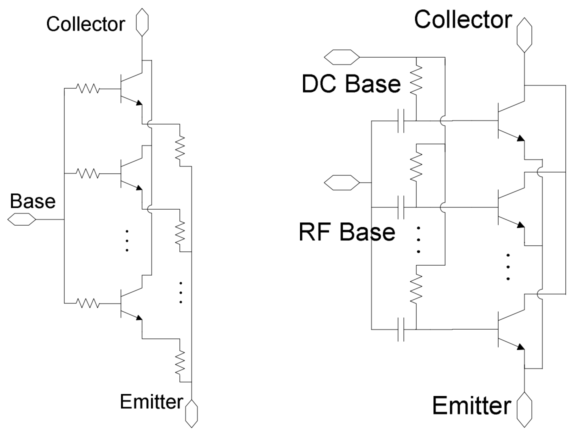


(a) (b)

Fig. 1. (a) Power cell with emitter and base ballast resistors. (b) Power cell with segmented capacitors at base.

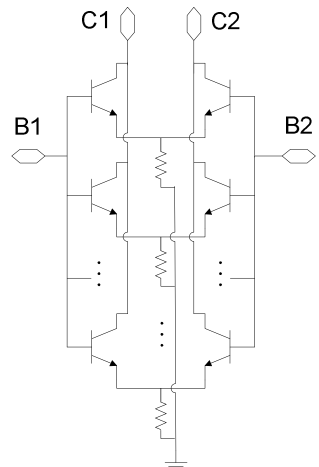
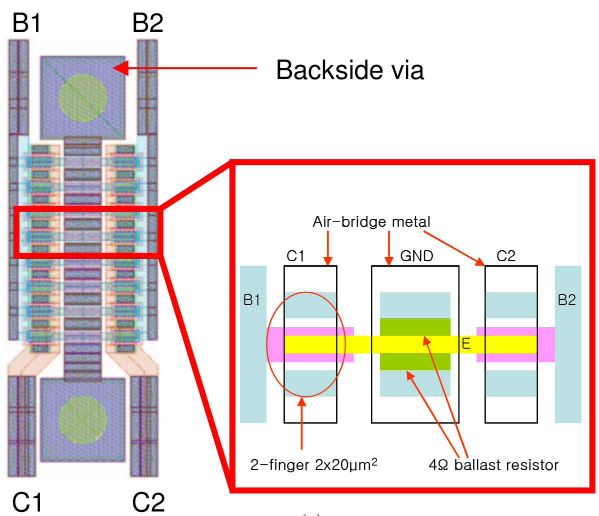
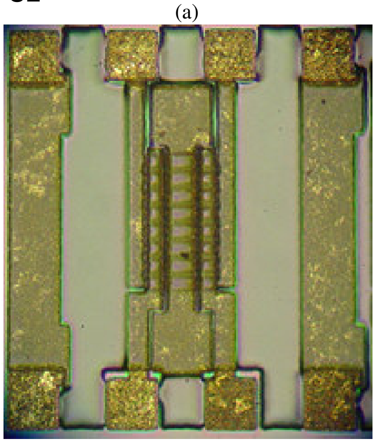


Fig. 2. The proposed differential power cell.

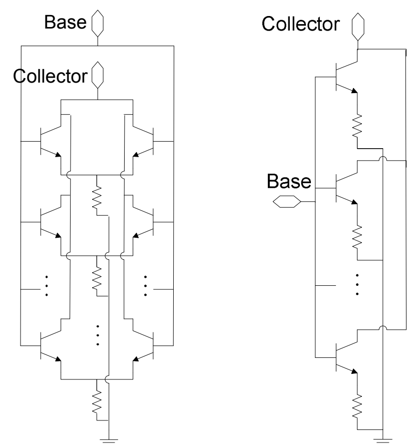


(a)



(b)

Fig. 3. (a) Layout of the differential power cell (64-finger 2x20-μm² device, 160x470-μm² area). (b) Microphotograph of the differential power cell.



(a) (b)

Fig. 4. The proposed model parameter extraction patterns. (a) Common mode pattern of the differential power cell. (b) Half circuit pattern of the differential power cell.

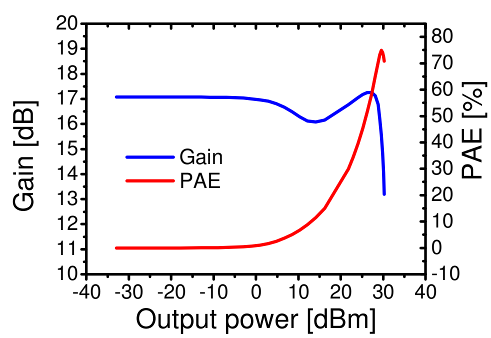


Fig. 5. Simulated results using a parallel-combined model of 2-finger unit transistor models at 1.95 GHz.