A LOW POWER CHARGE-RECYCLING ROM ARCHITECTURE

Byung-Do Yang and Lee-Sup Kim
Department of EECS, KAIST,
373-1 Kusong-dong, Yusong-gu, Taejon, 305-701, KOREA

ABSTRACT

A new low power charge recycling ROM (CR-ROM) architecture is proposed. The CR-ROM uses charge-recycling method [4] in bit lines of ROM to save the power consumption. About 90% of the total power used in the ROM is consumed in bit lines [1]. With the proposed method, power consumption in ROM bit lines can be reduced asymptotically to zero if the number of bit lines is infinite and the sense amplifiers detect infinitely small voltage difference. However, the real sense amplifiers cannot sense very small voltage difference. Therefore, reduction of power consumption is limited. The simulation results show that the CR-ROM only consumes 13% ~ 78% of the conventional low power contact programming mask ROM [1].

1. INTRODUCTION

As mobile systems such as PDA, cellular phone, and notebook computers are very popular, power consumption has become a major concern for VLSI chip designs. ROMs (Read Only Memory) are an important part of VLSI chips, especially for digital filters and signal processors. ROMs are very busy parts in the chips and the size of ROMs continues to be lager, so that a number of techniques to reduce power consumption in ROMs have been proposed [1]-[3]. The power consumption in the ROM core is about 90% of total ROM power consumption [1]. The bit lines in the ROM core dissipate most of the power because bit lines have large capacitance and a lot of bit lines are selected per an access. Therefore, most of low power techniques for ROMs have focused to reduce the power consumption in ROM core.

In this paper, a low power charge-recycling ROM architecture is proposed to reduce the power consumption of ROM bit lines. The charge-recycling ROM (CR-ROM) uses the charge recycling method [4]. The CR-ROM can save the most of the power dissipated in the conventional ROM bit lines. The larger number of bit lines are selected in the ROM core, the more power can be saved in the CR-ROM.

In section 2.1, we explain the concept of charge recycling operation in the ROM bit lines. The charge recycling operation reduces the voltage swing in the bit lines and saves the power dissipated. In section 2.2, we describe sense amplifiers used in the CR-ROM for sensing small swing in the ROM bit lines. In section 2.3, we propose CR-ROM architecture. In section 2.4, an effective layout of CR-ROM core cells is proposed. In section 3, we represent simulation results and comparisons. This paper is finished with the conclusion in section 4.

2. CHARGE RECYCLING ROM ARCHITECTURE

2.1 Concept of Charge Recycling ROM

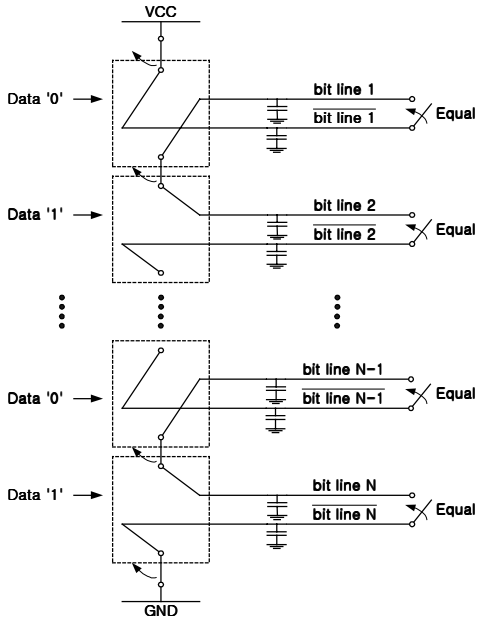


Figure 1. Concept of charge recycling ROM.

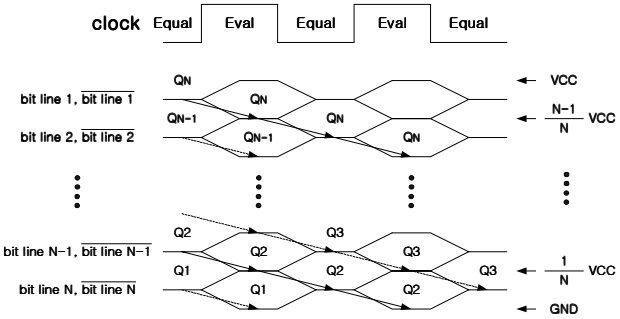


Figure 2. Concept of charge recycling operation.

Fig. 1 and Fig. 2 show the concept of charge recycling ROM. Conventional ROMs have one bit line to get one data, but the proposed CR-ROM uses two lines to get one data like DRAM in which the two bit lines have small voltage swing. All bit lines have almost the same capacitance because they are connected to exactly the same number transistors and have the same length.

All bit lines are grouped to 2N bit lines. Two bit lines in one group recycle the charge used in the previous two bit lines in the same group. Fig. 1 shows a group of bit lines and transistor connections programmed by ROM data. Data '0' or data '1' programs the connections between two bit lines and the neighbor bit lines. When the bit line has higher voltage than the complementary bit line, the ROM data is '1' and when the complementary bit line has higher voltage than the bit line, the ROM data is '0'. From Fig. 1, we know that the connections by the ROM data are very simple. When the ROM data is '1', the bit line is connected to the next bit line with higher voltage and the complementary bit line is connected to the next bit line with lower voltage. The bit line, which is in the top bit line pair in a group and must be connected to the next bit line with higher voltage, is connected to the supply voltage 'VCC'. On the contrary, the bit line, which is in the bottom bit line pair in a group and must be connected to the next bit line with lower voltage, is connected to the ground 'GND'.

The programmed bit line connections are made of transistors. When ROM is in 'equalization' mode, all programmed connections between bit line pairs are disconnected and all bit line pairs are connected by 'Equal' signal such that two bit lines having voltage difference share their charge and have the average voltage of the two bit lines in a bit line pair. M*th* bit line pair in a group having N bit line pairs has the voltage '(2N-2M+1)/(2N+2)•VCC'. When ROM is in 'evaluation' mode, all programmed connections are connected and all bit line pairs connected by 'Equal' signal are disconnected. Two bit lines in Mth bit line pair have different voltages by connecting two bit lines to the next bit lines. A bit line and the connected next bit line, which have voltage difference '1/(N+1)•VCC', share their charge and have the average voltage of the two bit lines. As a result, Mth bit line pair has voltage difference '1/(N+1)•VCC'. We can get the programmed data in ROM by detecting which bit line of a bit line pair has higher voltage than the other bit line.

Through the charge sharing in bit line pairs or in bit lines of different bit line pairs during the 'equalization' and 'evaluation', the charges used in the upper bit lines are recycled in the lower bit lines in the next clock cycle, as shown Fig. 2. Charge Q_N used in bit line 1 pair in the first clock cycle is used in bit line 2 pair in the second clock cycle. The Q_N is recycled N times through N bit line pairs from VCC to ground.

When one group has N bit line pairs and each bit line capacitance is C_{BL}, the N bit line pairs consume the power '$1/N \bullet C_{BL} \bullet VCC^2$' per a clock cycle instead of '$N \bullet C_{BL} \bullet VCC^2$'. As the number of N increases, power saving in the ROM core becomes salient.

2.2 Sense Amplifier

To detect the small voltage difference in two bit lines, sense amplifiers shown in Fig. 4 are used. Two types of sense amplifiers are needed for sensing a wide range of voltage swings in Fig. 3. The NMOS type sense amplifier is needed to sense the small voltage difference of two bit line voltages over half VCC and the PMOS type sense amplifier is needed to sense under half VCC.

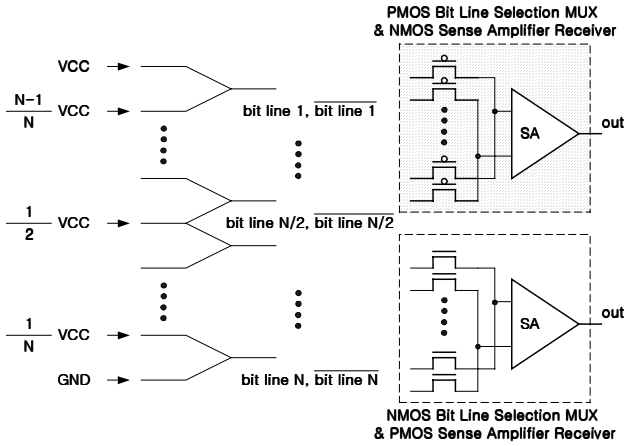


Figure 3. Bit line selection and sense amplifier

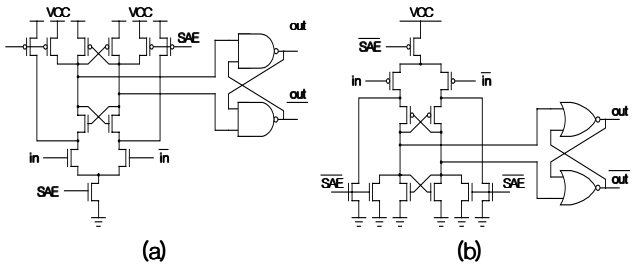


Figure 4. Sense amplifiers used in CR-ROM (a) NMOS type sense amplifier (b) PMOS type sense amplifier

When the input voltages are under half VCC, the NMOS transistors connected to input wires in NMOS type sense amplifier turn on slightly or turn off. So the NMOS type sense amplifier cannot detect small voltage difference of two bit lines having voltage under half VCC. Also, the PMOS type sense amplifier cannot detect the input voltages over half VCC.

Not all bit line pairs are sensed because the number of output bits is fewer than the number of total bit line pairs in ROMs. So, the required sense amplifier number is fewer than the number of total bit line pairs and MUXs are needed to select which bit line pair is connected to the sense amplifier to be a ROM output.

To provide select signals of MUXs, the column decoder used in conventional ROM can be used except that the select signals of MUXs in CR-ROM need additionally complementary select signals for PMOS type MUXs in Fig. 3. Two types of MUXs are used to pass the voltage of bit lines to sense amplifiers like two type sense amplifiers. PMOS type bit line selection MUX is used to make that the selected bit line voltages over half VCC and the input voltages of the sense amplifier are the same. NMOS type bit line selection MUX is used for bit lines in which the voltages are under half VCC.

The required MUX number in a group is varied according to output bits per a group. When the bit line pair number N in a group is 8 and output bits per a group are 4, the two PMOS type 4-to-2 MUXs and two NMOS type 4-to-2 MUXs are required. And two NMOS type sense amplifiers and two PMOS type sense amplifiers are also used.

The minimum number of the required MUXs and sense amplifiers per a group are one PMOS type MUX, one NMOS type MUX, one NMOS type sense amplifier, and one PMOS type sense amplifier, even though just one output bit per a group or one output bit per several groups is necessary.

2.3 Charge Recycling ROM Architecture

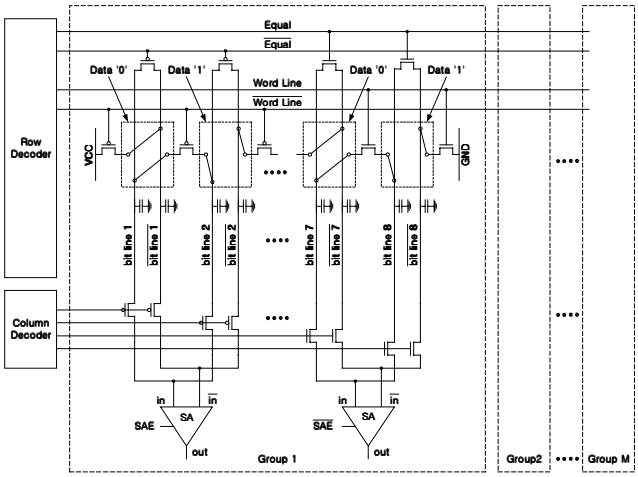


Figure 5. Charge recycling ROM architecture

Fig. 5 shows the CR-ROM architecture with 8 bit line pairs, an NMOS type sense amplifier, and a PMOS type sense amplifier in a group. Half of ROM bit line pairs are connected to PMOS transistors which are used for equalizing each bit line pair by the reverse equal signal and for connecting each bit line to the next bit line or supply voltage 'VCC' by the reverse word line signal. The other half of ROM bit line pairs is connected to NMOS transistors which are used for equalizing each bit line pair by the equal signal and for connecting each bit line to the next bit line or ground by the word line signal.

The required equal lines and word lines are two times as many as the conventional ROM's. But the number of transistors connected to each equal line and word line is a half of the conventional ROM's, so that the total number of the transistors used for equalization and for ROM cells to store data is the same as the total number of the transistors used in conventional ROM.

There are a little area and power penalties for two equal lines and two word lines. Two global equal lines and each two word lines can be drawn over one transistor space so that no extra space is needed. Also, the additional power consumption in equal lines and word lines is quite small compared to total power consumption because the gate capacitance of transistors is much bigger than the capacitance of the metal line. The proposed CR-ROM has a small area overhead but a significant power saving in bit lines in which most of power is consumed in the ROM.

2.4 ROM Cell Structure

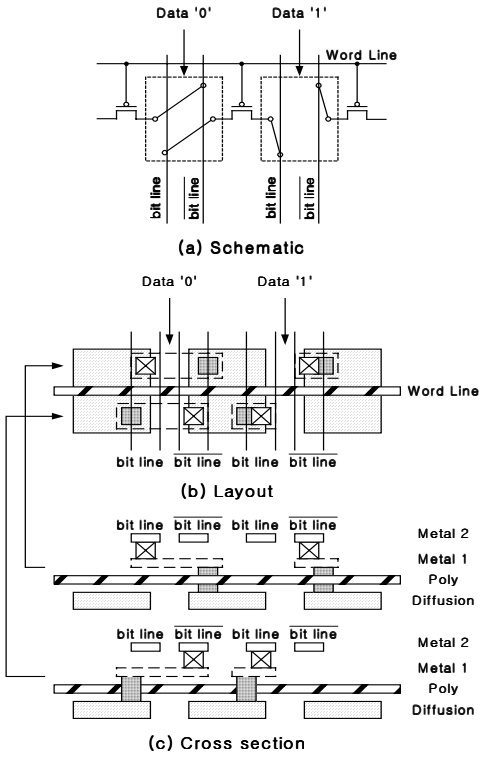


Figure 6. Charge recycling ROM cell schematic and layout

The programmed cell structures in the proposed CR-ROM are shown in Fig. 5. Fig. 5(a) is the schematic of programmed cell connections. Fig. 5(b) and Fig. 5(c) are the layout of the schematic and the cross sections of the layout. The simple connections to store data can be easily drawn in layout.

The layout shows that the transistors are not minimum size. The transistor gate width is about 2 times as wide as the minimum transistor gate size. But the space between transistors is the same. As a result, the ROM core size overhead is about 1.5 times compared to the ROM core having minimum transistor size.

3. SIMULATION RESULTS AND COMPARISONS

Table 1 shows the performance comparison of each type of ROM. 32Kbit ROMs (256cells x 128cells, 1K x 32 bits) with minimum cell transistors are implemented for comparison. All circuit simulations are based on 0.25um CMOS process parameters and HSPICE models. Parasitic capacitances are included in the simulations. Powers are measured at 100MHz clock frequency with VCC = 2.5V.

The conventional ROM (CV-ROM) [1] uses the low power techniques; hierarchical word line, selective precharge, NMOS precharge, and etc. We controlled 300mV swings in bit lines of ROM using HiCapCS (CS-ROM) [3]. The proposed CR-ROM has 8 bit line pairs to make the voltage difference 300mV. The waveforms in the CR-ROM are presented in Fig. 7. The charge recycling operations are shown.

As the output bits in ROM increases without increasing the ROM core size (256cellsx128cells), the power consumption increase of the CR-ROM becomes slower than other ROMs shown in Fig. 8. The simulation results show that the CR-ROM only consumes 13% ~ 78% power of the CV-ROM. Therefore, the CR-ROM is more efficient when large output bit width is required.

Power consumptions in each part of the ROMs are measured in Fig. 9. The results show that the power consumption in cell and SA are dramatically reduced in the proposed CR-ROM. The simulated ROMs are 32Kbit ROMs (256cells x 128cells, 1K x 32 bits).

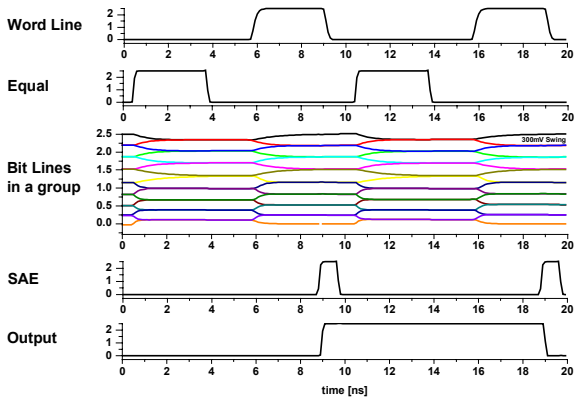


Figure 7. Simulated waveforms of the CR-ROM

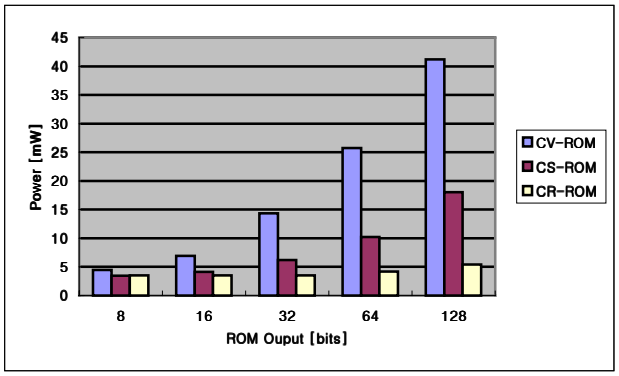


Figure 8. Power consumption vs. output bit number

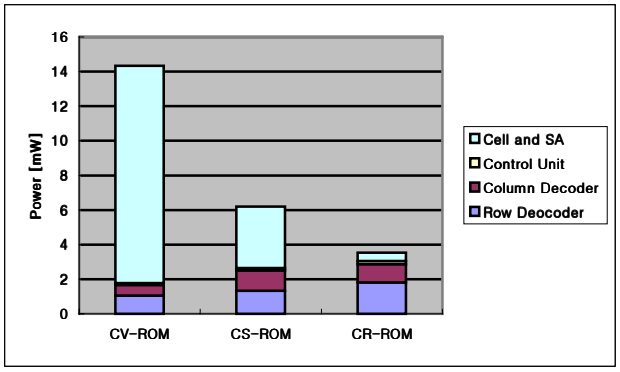
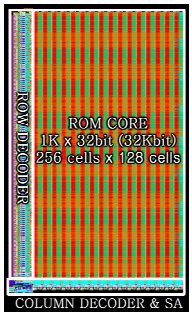


Figure 9. Power consumptions in ROMs (1K x 32 bits)

	Power [mW]	Area [mm^2]	Delay [ns]
Conventional ROM [1] (CV-ROM)	**14.33**	**0.0978 (0.19mmX0.42mm)**	**2.6**
ROM using HiCapCS [3] (CS-ROM)	**6.20**	**0.1302 (0.31mmX0.42mm)**	**3.2**
Charge Recycling ROM (CR-ROM)	**3.53**	**0.1512 (0.27mmX0.56mm)**	**6.0**

Table 1. Comparisons of ROM (1K x 32 bits) performance



Technology	0.25um CMOS
Supply Voltage	2.5V
Clock Frequency	100MHz
Organization	1K x 32 bits
ROM Size	0.27mm x 0.56mm
Power	3.53mW

Figure 10. Layout

4. CONCLUSIONS

This paper proposes a new low power charge recycling ROM architecture. The simulation results shows that the CR-ROM achieves up to 13% power consumptions compared to the conventional low power ROMs. The CR-ROM is more attractive for ROMs having a lot of output bits. Although the CR-ROM requires about 1.5 times area overhead and 2.3 times speed overhead compared to the conventional ROM with minimum size transistor ROM core cells, the CR-ROM is suitable for digital filters or DSPs having large output bit width.

5. ACKNOWLEDGMENT

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6. REFERENCES

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