A 1.8V-Input 0.2-to-1.5V-Output 2.5A 930mA/mm^3 Always-Balanced Dual-Path Hybrid Buck Converter with Seamlessly All-VCR-Coverable Tri-Mode Operation

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Abstract

This paper presents an always-balanced dual-path hybrid buck converter capable of covering all conversion ratios with high efficiency. The proposed tri-mode operations ensure seamless, defect-free dynamic voltage scaling (DVS). Fabricated in 180nm, the chip outputs voltages ranging from 0.2 to 1.5V with a 1.8V input. It achieves a peak efficiency of 94.2%, even with compact-volume *LC* parts. Its current density was measured to be 930mA/mm^3 at 2.5A load current.

Introduction

In the design of PMICs for mobile computing systems, the emphasis has increasingly shifted toward achieving both high efficiency and high power density. These goals, however, often conflict due to the elevated parasitic resistance (DCR) that comes with using a compact inductor. To address this challenge, recent research has explored hybrid converters [1-6] that employ flying capacitors (C_F). Such hybrid converters effectively lower the inductor current (I_L), thereby minimizing the DCR-related losses, P_{DCR} (= DCR·I_L^2). Despite these advances, supporting a wide range of dynamic voltage scaling (DVS) poses a significant challenge. This encompasses low-voltage operation as low as V_O = 0.2V, suitable for subthreshold computing, to high-voltage scenarios up to V_O = 1.5V for high-performance modes, with V_{IN} = 1.8V. Although a PMIC capable of covering these broad V_{IN}-to-V_O voltage conversion ratios (VCRs) is highly desirable, previous hybrid converters have limitations. Specifically, topologies in [1-6] fall short in covering the full scope of VCRs, and those in [1-5] suffer from exceedingly high capacitor currents at certain VCRs, leading to a drastic drop in efficiency. Furthermore, studies [1-4], which involve multi-mode operations to extend the available VCR range, face issues such as discontinuities in the C_F voltage during mode transitions, posing a risk of excessive inrush current.

Fig. 1 shows the basic concept used in most hybrid converters. During a switching cycle of T_{SW}, the hybrid converter operates in two phases: Φ_S (= D_S·T_{SW}) in which C_F and the inductor (L_O) are connected in series, and Φ_P (= D_P·T_{SW}) in which they are connected in parallel. In this traditional approach, the normalized inductor current, I_{NL} (= I_L/I_O, where I_O is the load current), is highly dependent on D_S (or VCR). If $D_S >> D_P$, the I_L-reduction is maximized, but the C_F-current at Φ_P, $I_{CF,\Phi P}$, surges excessively due to C_F being overly charged during a prolonged Φ_S. This $I_{CF,\Phi P}$ surge results in considerable conduction loss.

In this paper, we present a 1.8-V_{IN}, 0.2-to-1.5-V_O, tri-mode hybrid buck converter designed to always balance both inductive and capacitive currents across all VCRs. It also supports seamless mode change.

Proposed ABDP Hybrid Buck Converter

The top of Fig. 2 shows our proposed always-balanced dual-path (ABDP) hybrid buck converter. It comprises one L_O, two flying capacitors (C_{F1} and C_{F2}), and eight switches (S_1–S_8), featuring three distinct switching nodes: V_{XH}, V_{XM}, and V_{XL}. This design aims to maintain both the normalized I_{NL} (= I_L/I_O) and I_{NCF} (= $I_{CF,\Phi P}/I_O$) at a constant 2/3 by always ensuring $\Sigma D_S = \Sigma D_P = 0.5$ (top-left of Fig. 2). As shown at the middle of Fig. 2, there are five behavioral phases (Φ_1–Φ_5) in the ABDP converter. Specifically, $\Phi_{1,3,5}$ and $\Phi_{2,4}$ connect L_O and C_F in series and parallel, respectively. The duty-cycle ratios for Φ_1–Φ_5 are denoted as D_1–D_5. During the *LC*-series phase Φ_1 (or Φ_5), activating S_5 (or S_2) sets $V_{XL} = V_{IN}$ (or $V_{XH} = 0$) and the C_{F2} (or C_{F1}) charged to $V_{IN} - V_O$ (or V_O) energies (or de-energizes) L_O by $V_{XM} = 2V_{IN} - V_O$ (or $-V_O$). In the *LC*-parallel phase Φ_2 (or Φ_4), the activation of S_3 and S_8 (or S_4 and S_7) yields $V_{XM} = V_{IN}$ (or 0) and V_{XL} (or V_{XH}) = V_O, thus setting V_{CF2} (or V_{CF1}) to $V_{IN} - V_O$ (or V_O). During this phase, a dual-path power delivery mechanism is established, involving both the magnetizing (or de-energizing) I_L and the capacitive current, $I_{CF,\Phi P}$, discharged from C_{F2} (or C_{F1}). In another *LC*-series phase, Φ_3, the activated S_1 and S_6 set $V_{XH} = V_{IN}$ and $V_{XL} = 0$, ensuring $V_{CF1} + V_{CF2} = V_{IN}$. At this phase, the I_L is sourced from both C_{F1}-current [= $(1 - 2D_2)$·I_L] and C_{F2}-current (= $2D_2$·I_L). In the proposed ABDP converter, three operational phases are chosen from Φ_1–Φ_5, in accordance with the target VCR. The aim is to maintain ΣD_S (*LC*-series phase) = ΣD_P (*LC*-parallel phase) = 0.5, thereby guaranteeing an always-balanced dual-path power delivery across all VCRs. In the high-VCR (HV) mode, covering the range of 2/3 < VCR_{HV} < 1, a switching cycle (T_{SW}) is executed in the sequence of Φ_1-Φ_2-Φ_3-Φ_2. At this mode, D_2 is fixed at 0.5, and $D_3 = 0.5 - D_1$, thus balancing the *LC*-series phase ($D_1 + D_3$ = 0.5) and the *LC*-parallel phase (D_2 = 0.5). This balanced dual-path power delivery consistently equalizes I_{NL} and I_{NCF} to 2/3, regardless of D_1. This offers the optimum point at which the total conduction loss (P_{COND}) reaches its minimum, enhancing efficiency. Despite the fixed I_{NL}, VCR_{HV} is controllable, given by $(2 + 2D_1)/3$. For the mid-VCR (MV) mode ($1/3 < VCR_{MV} < 2/3$), T_{SW} consists of the sequence Φ_2-Φ_3-Φ_4-Φ_3. In this mode, D_3 = 0.5 and $D_4 = 0.5 - D_2$, resulting in $VCR_{MV} = (1 + 2D_2)/3$ and $I_{NL} = I_{NCF} = 2/3$. In the low-VCR (LV) mode ($0 < VCR_{LV} < 1/3$), the T_{SW} sequence is Φ_3-Φ_4-Φ_5-Φ_4. In the LV mode, $D_4 = 0.5$ and $D_5 = 0.5 - D_3$, leading to $VCR_{LV} = 2D_3/3$. Again, I_{NL} and I_{NCF} are all maintained at 2/3. Note that VCR_{HV}, VCR_{MV}, and VCR_{LV} are seamlessly transitional, and all modes include the Φ_3-phase, which ensures $V_{CF1} + V_{CF2} = V_{IN}$. Thus, the flying capacitor voltages can be stably sustained, with $V_{CF1} = V_O$ and $V_{CF2} = V_{IN} - V_O$, across all VCRs.

Fig. 3 provides theoretical comparisons between the proposed ABDP design and prior hybrid converters. In the top-left of Fig. 3, this work stands out as the only design that maintains a constantly-reduced I_L (= 2/3·I_O) for the full VCR range. The top-right of Fig. 2 delves into the normalized capacitor current (I_{NCF}). In contrast to [2-4], where I_{NCF} values tend to diverge to infinity as they approach specific VCRs, the ABDP converter consistently offers I_{NCF} = 2/3 irrespective of the VCR. Assuming that all switches have identical R_{ON} and that the inductor's DCR = 3·R_{ON}, the bottom-left of Fig. 3 focuses on the comparison of normalized conduction loss (P_{NC}). The P_{NC} values in prior works [2-4] fluctuate significantly due to VCR-dependent I_{NL} and I_{NCF}. On the other hand, the proposed ABDP converter consistently achieves a 33-to-36% reduction in P_{NC} across all VCRs. The bottom-right of Fig. 3 shows the flying capacitor voltages with respect to the VCR. In multi-mode converter [4], discontinuity in V_{CF} can be observed at certain VCRs, potentially impeding seamless transitions between VCRs. In contrast, the ABDP converter is designed to stably maintain $V_{CF1} = V_O$ and $V_{CF2} = V_{IN} - V_O$, thereby facilitating seamless mode changes.

Fig. 4 shows the design details of the ABDP hybrid converter chip. Five operational phase signals (Φ_1–Φ_5) for tri-mode operations are generated by comparing the error-signal (V_E) with four distinct triangular waves (V_{RP1}–V_{RP4}). The interval of V_{RP1}–V_{RP4} are set to implement the 50%-fixed duty-cycles D_2, D_3, and D_4 in the HV, MV, and LV modes, respectively. To promote seamless mode changes, the upper-vertex of V_{RP4} (V_{RP3}) is designed to coincide with the lower-vertex of V_{RP2} (V_{RP1}). In the proposed ABDP design, dynamic voltage switching necessitates sophisticated gate and body driving techniques. Instead of resorting to extra bootstrapping capacitors, this work employs a Φ-adaptive gate and body driver that leverages multi-level voltages (V_{IN}, V_{XH}, and V_{XL}) that are inherently given in the ABDP converter.

Measurement Results

The proposed converter was fabricated in a 180nm CMOS (Fig. 8). The chip able to supply I_O up to 2.5A operates with V_{IN} = 1.8V and F_{SW} = 1MHz. Tests were performed with L_O = 470nH and $C_{F1} = C_{F2} = C_O$ (output cap) = 10μF. Fig. 5 shows the measured steady-state waveforms for V_O = 1.5V, 0.9V, and 0.2V. It is observed that I_L was consistently reduced by 31~36% compared to I_O = 1A. Fig. 5 also demonstrates seamless V_O coverage across a wide VCR range. Note that any defective voltage or current is invisible in V_O, V_{XM}, or I_L. The top of Fig. 6 shows the load-transient and DVS responses. The bottom of Fig. 6 displays the measured efficiency curves. Using compact-volume passive components, a peak efficiency of 94.2% was achieved at V_O = 1.2V and I_O = 0.4A. Fig. 7 summarizes the performance. This work is the first buck converter capable of seamless coverage across all VCRs, while maintaining a consistent balance between inductive and capacitive currents. As a result of these innovations, this work achieves a current density of 930mA/mm^3, which outperforms [2-6].

References

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[2] Y. Huh *et al.*, JSSC 2019.
[3] J. Ko *et al.*, VLSI 2021.
[4] G. Cai *et al.*, JSSC 2023.
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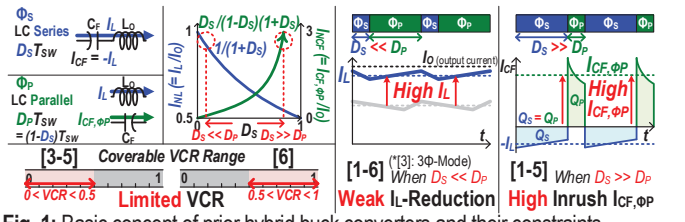


Fig. 1: Basic concept of prior hybrid buck converters and their constraints.

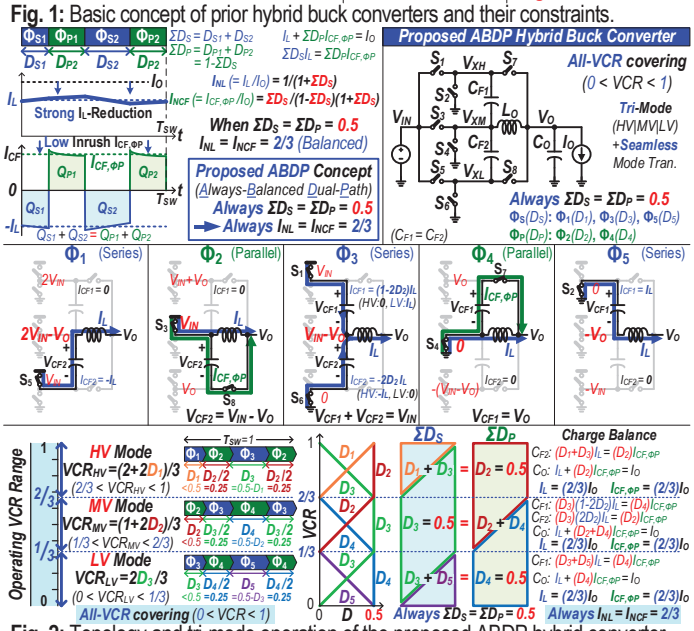


Fig. 2: Topology and tri-mode operation of the proposed ABDP hybrid converter.

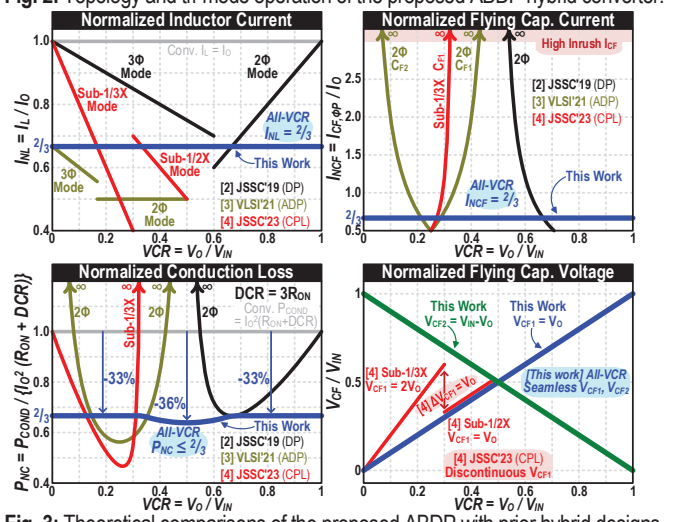


Fig. 3: Theoretical comparisons of the proposed ABDP with prior hybrid designs.

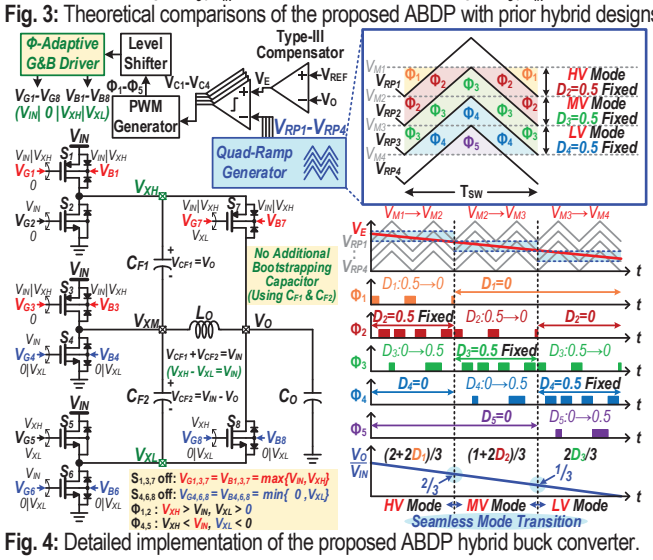
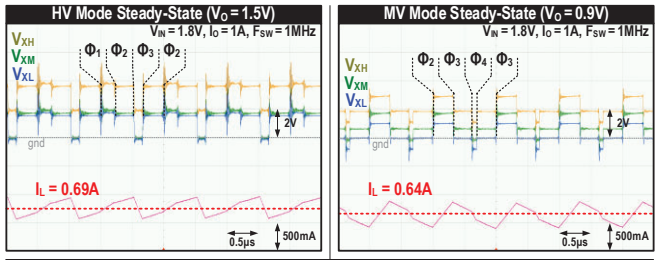


Fig. 4: Detailed implementation of the proposed ABDP hybrid buck converter.



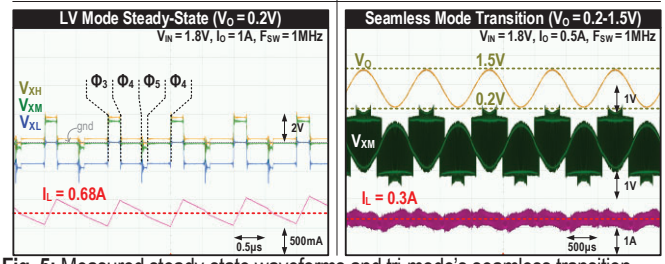
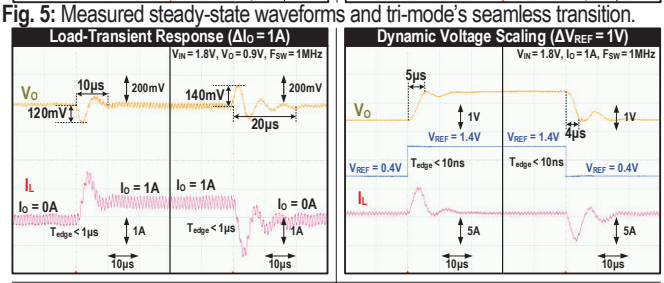


Fig. 5: Measured steady-state waveforms and tri-mode's seamless transition.



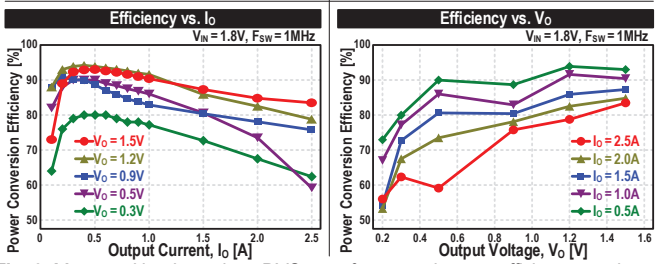


Fig. 6: Measured load transient, DVS waveforms, and power efficiency graphs.

	[2]JSSC'19	[3]VLSI'21	[4]JSSC'23	[5]TPE'24	[6]VLSI'23	This Work
CMOS Process	180nm	180nm	65nm	130nm	180nm	**180nm**
Topology	DP	ADP	CPL	ADPR	OISC	**ABDP**
V_{IN} [V]	4.5	3.4 - 4.5	3 - 4.2	2.8 - 4.2	1.5 - 3.3	**1.8**
V_O [V]	0.8 - 4	0.3 - 1.7	0.6 - 1	0.7 - 1.1	0.8 - 1.8	**0.2 - 1.5**
$I_{O,MAX}$ [A]	1.6	1.6	1.2	0.8	3.1	**2.5**
F_{SW} [MHz]	1	1	2	1	0.5	**1**
Chip Area [mm²]	3.24	4.08	2.72	12.6	7.63	**4**
L_O [µH] @ Vol. [mm³]	4.7 @5	4.7 @4	0.47 @1	4.7 @3.2	1x2 @1x2	**0.47 @1**
C_F [µF] @ Vol. [mm³]	10 @1*	10x2 @0.25x2	4.7x2 @0.25x2	4.7x2 @2.9x2	4.7x4 @0.25x4	**10x2 @0.25x2**
Total Volume [mm³] **	6.97	5.72	2.32	12.8	5.29	**2.7**
PE [%] @VCR, I_O [mA]	96.2 @0.71, 400	91.5 @0.38, 400	92.9 @0.27, 400	95.4 @0.28, 75	97.3 @0.55, 500	**94.2 @0.67, 400**
CD [mA/mm³] @ $I_{O,MAX}$	230	280	520	63	585	**930**
CD [mA/mm³] @ PE	57	70	170	6	94	**150**
Coverable VCR Range	0 - 1	0 - 0.5	0 - 0.5	0 - 0.5	0.5 - 1	**0 - 1**
Normalized I_{NL} (= I_L / I_O)	0.5 - 1	0.5	1/3 - 1	1/3 - 1	0.5 - 1***	Fixed **2/3**
Normalized I_{NCF} (= $I_{CF,\Phi P}$ / I_O)	0 - ∞	0 - ∞	0 - ∞	0 - ∞	0 - 0.5***	Fixed **2/3**

* Estimated from the reported data ** L_O + C_{FS} + Chip (0.3mm die height estimation) *** [6] Single Branch

PE = Peak Efficiency CD = Current Density (= I_O / Total Volume) VCR = Voltage Conversion Ratio (=V_O/V_{IN})

Fig. 7: Performance summary in caparison with previous state-of-the-arts.

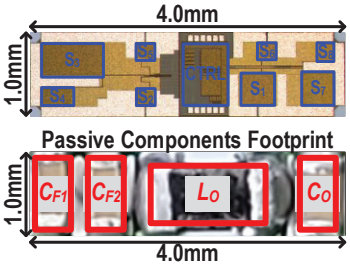


Fig. 8: Die and PCB photos.

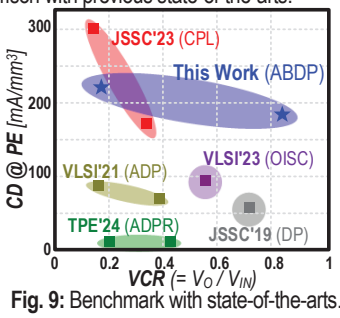


Fig. 9: Benchmark with state-of-the-arts.