Introduction to the Special Issue on the 2020 IEEE International Solid-State Circuits Conference (ISSCC)

I. Introduction

THIS Special Issue of the IEEE Journal of Solid-State Circuits is dedicated to a collection of the best papers selected from the 2020 IEEE International Solid-State Circuits Conference (ISSCC) that took place on February 16–20, 2020, in San Francisco, CA, USA. This issue covers papers from the Analog, Power Management, Data Converters, RF, and Wireless committees.

II. Analog Papers

In the analog circuits category, three articles from two sessions were selected, each tackling a different challenge in this field. The first paper presents a current-domain analog frontend for an automotive Lidar system using optical sub-pulses. This enables $>10\times$ lower peak transmit power compared to conventional single-pulse approaches. The second paper is also in the area of automotive applications and presents a Class-D amplifier which uses a hybrid $\Delta\Sigma$M-pulsewidth modulation (PWM) scheme. This approach results in high linearity over a wide output power range and reduced AM-band electromagnetic interference (EMI) in order to meet automotive standards. The third paper presents a low-noise transimpedance amplifier designed for miniature ultrasound probes. It provides continuously variable gain to compensate for the time-dependent attenuation of the received echo signal resulting in reduced output dynamic range and saving power.

III. Power Management Papers

Four articles have been selected from three sessions of power management, including dc–dc converters, USB charging, and wireless power transfer. A monolithic 400-V offline buck converter with an integrated power stage and controller using e-mode GaN FETs provides a peak power efficiency of 95.6% and a power density of 44 W/in^3. A monolithic resonant switched-capacitor converter with integrated *LC* resonator and output regulation delivers 0.87 W output power with 85.5% peak power efficiency in a 0.18-μm bulk CMOS. A flyback converter with zero-voltage switching and integrated controllers enables USB Type-C power delivery and charging with a maximum efficiency of 93.5%. A current-mode wireless power and data receiver charges the battery with a peak efficiency of 92.6% at 13.56 MHz and allows energy-shift keying data transmission with a data rate of 100 kb/s.

IV. Data Converter Papers

Six data converter articles from two sessions were selected. The first two articles present time-interleaved analog-to-digital converters (ADCs). The first article interleaves 12-bit pipelined ADCs using a frontend track-and-hold amplifier and extensive digital calibration to achieve high accuracy at 18 GS/s. The second article proposes interleaving time-domain ADCs which have a robust interpolation-based architecture to achieve area and power efficiency at 10 GS/s. The next two articles focus on the emerging noise-shaping SAR ADC architecture with an emphasis on increased resolution and robustness to process, and voltage and temperature variations. One article proposes a cascaded fourth-order architecture to achieve these goals, while the other uses a closed-loop dynamic amplifier to ensure a sharp and stable noise transfer function. The fifth article uses a double-sampling technique to reduce the required input capacitance of a SAR ADC. The final paper proposes a switched-capacitor technique to improve the uncalibrated interstage gain accuracy of a pipelined ADC.

V. Radio Frequency Papers

Six articles have been selected from three sessions on RF, and they include various topics such as RF frequency synthesizers, millimeter-wave (mm-wave) power amplifiers (PAs), and emerging RF and THz techniques. Jain *et al*. presented a terahertz-source system-on-a-chip (SoC) that was designed for computational imaging with a single-pixel camera (SPC). Renukaswamy *et al*. presented a 10-GHz low-noise subsampling phase-locked loop (SSPLL) that was capable of wideband frequency modulation for frequency-modulated continuous-wave (FMCW) radar applications. Nagulu *et al*. presented the design of a 1-GHz passive, nonmagnetic, switched CMOS circulator. Yoo *et al*. presented a 30.0-dBm polar digital PA based on a switched-capacitor PA (SCPA) and multiple efficiency-enhancement techniques such as Class-G, Doherty, and time interleaving. Mannem *et al*. presented a reconfigurable hybrid series/parallel Doherty PA with a 90° coupler-based active load modulation network to address the problem of antenna load impedance variations. Santiccioli *et al*. presented a fast-settling fractional-*N* phase-locked loop (PLL) that overcame the limits of conventional bang-bang-phase detector (BBPD)-based architectures.

VI. Wireless Papers

Five articles have been selected from the wireless subcommittee's three sessions focusing on transceivers with low power consumption, high integration, and wide bandwidth operation. In the first paper, Li *et al*. describe a 4.8-dB NF,

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2.2-dBm IIP3, *E*-band LNA with on-chip multifeed antenna-based noise cancellation and antenna-circuit co-design. In the second paper, Tamura *et al*. present a BLE transceiver with an on-chip transformer-based LNTA and an asynchronous SAR-ADC-based ADPLL that achieves 1.9-mW Rx with −96.4-dBm sensitivity under 0.5-V operation. In the third paper, Qi *et al*. describe an FDD SAW-less transmitter with a bandwidth-extended *N*-path filter modulator and a transimpedance amplifier-based PA. In the fourth paper, Lee *et al*. present a fully integrated, low-cost NB-IoT and GNSS SoC that uses a DCXO and a temperature sensing unit to eliminate a TCXO. Finally, Ben-Bassat *et al*. describe a dual-band 27-dBm polar transmitter achieving –35-dBm EVM over 80-MHz bandwidth using digitally controlled two-point edge interpolation.

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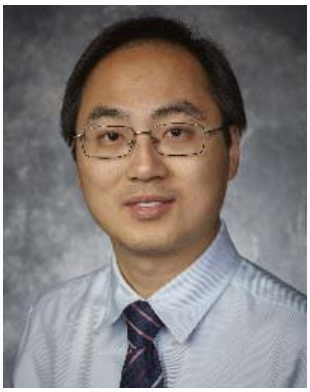
Until August 2001, he worked for Motorola, Inc., Austin, TX, USA, where he was the Manager of the High Performance Design Technology Group. Since August 2001, he has been on the faculty of the University of Michigan, Ann Arbor, MI, USA, where he is currently the Kensall D. Wise Collegiate Professor of EECS. He is also the Director of the Michigan Integrated Circuits Lab. He has published over 600 articles. He holds 65 patents. He has performed extensive research in ultralow-power computing using subthreshold operation and analog circuits for millimeter sensor systems, which was selected by the MIT Technology Review as one of the year's most significant innovations. For high-end servers, his research group introduced the so-called near-threshold computing, which has become a common concept in semiconductor design. Most recently, he has pursued research in cognitive computing using analog, in-memory neural networks for edge devices and genomics acceleration for precision health.

Dr. Blaauw received numerous best paper awards. He received the Motorola Innovation Award. He was the General Chair of the IEEE International Symposium on Low Power and the Technical Program Chair of the ACM/IEEE Design Automation Conference. He serves on the Technical Program Committee of the IEEE International Solid-State Circuits Conference. He received the 2016 SIA-SRC Faculty Award for lifetime research contributions to the U.S. semiconductor industry.



Hoi Lee (Senior Member, IEEE) received the B.Eng., M.Phil., and Ph.D. degrees in electrical and electronic engineering from The Hong Kong University of Science and Technology, Hong Kong, in 1998, 2000, and 2004, respectively.

Since January 2005, he has been with the Department of Electrical and Computer Engineering, The University of Texas at Dallas, Richardson, TX, USA, where he is currently a Full Professor. His research interests include power management integrated circuits, power converter topologies and control methodologies, wireless power and energy-harvesting technologies, and low-power analog and mixed-signal integrated circuits.

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Jaehyouk Choi (Senior Member, IEEE) was born in Seoul, South Korea. He received the B.S. degree *(summa cum laude)* in electrical engineering from Seoul National University, Seoul, in 2003, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2008 and 2010, respectively.

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Dr. Choi has been a member of the Technical Program Committee of the IEEE International Solid-State Circuits Conference (ISSCC) since 2017 and the IEEE European Solid-State Circuits Conference (ESSCIRC) since 2016. He was a recipient of the IEEE/IEIE Joint Award for IT Young Engineer Award in 2020. He is also a Distinguished Lecturer of the IEEE Solid-State Circuits Society. He was the country representative of Korea for the ISSCC Far-East region in 2018.

Sudhakar Pamarti (Senior Member, IEEE) received the Bachelor of Technology degree from IIT Kharagpur, Kharagpur, India, in 1995, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at San Diego, La Jolla, CA, USA, in 1997 and 2003, respectively.

He is currently a Professor of electrical and computer engineering with the University of California at Los Angeles, Los Angeles, CA, USA. He has either worked for, or consulted with, both leading software and hardware companies on various aspects of wireless and wireline communications, and analog, mixed-signal, and RF integrated circuit (IC) design. His research focuses on developing various techniques, especially signal processing ones, to overcome common impairments in ICs. This includes both establishing the theoretical basis of such techniques as well as demonstrating their efficacy using record-setting prototype ICs. He is the (co)author of more than 100 conference and journal papers and eight patents.

Dr. Pamarti was a recipient of the National Science Foundation's CAREER Award. He currently serves as an IEEE Solid-State Circuits Society Distinguished Lecturer. He is on the Technical Program Committee of the IEEE Custom Integrated Circuits Conference and the IEEE International Solid-State Circuits Conference. He has, in the past, served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS and the IEEE TRANSACTIONS ON CIRCUITS ANDSYSTEMS—II: EXPRESS BRIEFS.