A 13 dB IIP3 improved Low-power CMOS RF Programmable Gain Amplifier using Differential Circuit Transconductance Linearization for Various Terrestrial Mobile D-TV Applications

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Abstract

A CMOS RF digitally programmable gain amplifier, covering various terrestrial mobile Digital TV standards (DMB, ISDB-T, and DVB-H) is implemented. 13 dB IIP3 improvement is attained without losing out on other performance criteria like gain, NF, CMRR, etc. at similar power consumption. This is achieved by applying a newly proposed differential circuit gm″ cancellation technique. The IC exhibits 55 dB gain range with 0.25 dB resolution, 4.5 dB NF, a -4 dBm IIP3 (maximum 30 dBm) and 25 dB gain at 16mW power consumption.

***Index Terms* — CMOS, Digital TV, IIP3, Linearity.**

Introduction

Various mobile Digital TV (D-TV) standards such as, Digital Multimedia Broadcasting (DMB) in Korea, Integrated Service Digital Broadcasting-Terrestrial (ISDB-T) in Japan and Digital Video Broadcasting-Handheld (DVB-H) in Europe make it possible to watch TV in a mobile environment. CMOS is believed to be the most promising technology for mobile tuner IC, with low cost and also System On a Chip (SOC) capability with digital circuits. In the integration of tuner front-ends with CMOS for SOC, there exist several stringent requirements, such as, immunity to digital circuitry noise and power consumption. Power consumption which is directly related to linearity should be minimized in order to extend the battery time. Thus, it is important to have a high rejection to digital circuitry noise, and maximize linearity/(power consumption). Also, a large gain range with fine resolution and a low NF in a RF domain, are still challenging on a single CMOS substrate [1].

In order to maximize linearity/power, linearity improvement technique should be employed. Previous linearity improvement technique [2] for CMOS is only for single-ended topology, which is not appropriate for SOC because of its bad common mode noise rejection. Also differential circuit linearity improvement techniques, described in [3], [4] are for a pseudo-differential amplifier based circuit. This is also weak for common-mode noise disturbances which will be discussed later. The other technique [5] consumes too much power and is weak for mismatches.

In this paper, we propose a CMOS RF digitally programmable gain amplifier (RFPGA), for various terrestrial D-TV standards, with a technique to improve differential circuit linearity without losing other performances and consuming extra power. This paper firstly introduces a new differential circuit linearity improvement technique and then, discusses RF programmable gain amplifier.

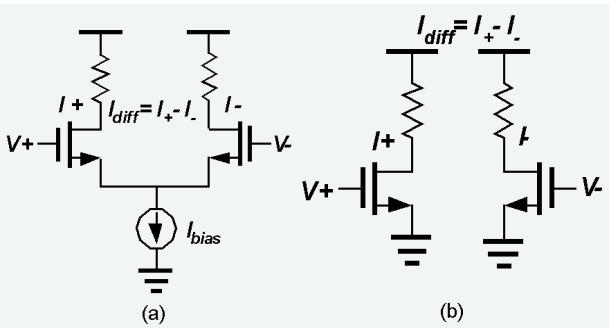

Fig. 1. There exist two topologies in differential circuits such as (a) Fully Differential Amplifier (FDA) and (b) Pseudo Differential Amplifier (PDA).

Differential Multiple Gated Transistor (DMGTR) Amplifier

A differential topology is one of the best ways to reject digital circuitry noise, which usually acts as common mode disturbance in a SOC. There are two kinds of differential circuits. One is a Fully Differential Amplifier (FDA) and the other is a Pseudo-Differential Amplifier (PDA) as shown in Fig. 1. It is better for the SOC to use FDA which has a higher common mode noise rejection than a PDA. Because FDA has well defined current source which plays as large feedback impedance over common mode signal, while ground over differential signals. The FDA's current (I+, I-), differential current [(I+)-(I-)], and the first and third derivative (gm, gm″) of differential current are shown in Fig. 2-A. As it is widely known, gm″ is major dominant factor for third order nonlinearity (IIP3) in CMOS RF amplifier [2]. Thus, the negative excursion of gm″ from zero degrades IIP3. The PDA's current, differential current and gm, gm″ of differential current of PDA are shown in Fig. 2-B. The major difference between the two circuits lies in gm″. Fig. 3 shows gm″ behaviors of FDA and PDA. Both a high bias and a low bias cases are compared. In FDA, the

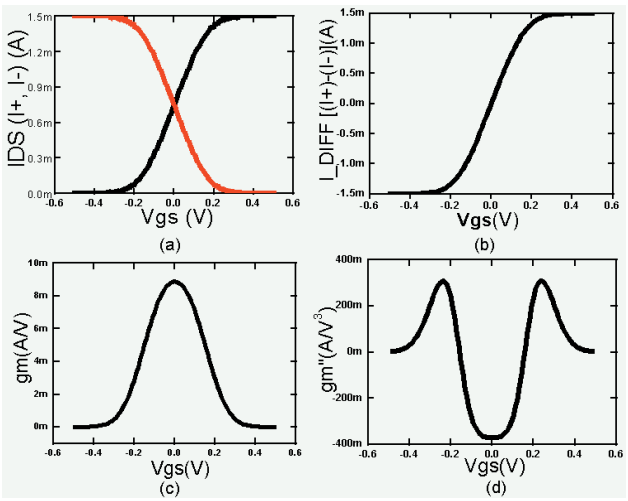

Fig. 2-A FDA current and its derivative's behaviors. (a) FDA branch currents, I+, I-, (b) differential current, [(I+)-(I-)], (c) gm of differential current, (d) gm″ of differential current.

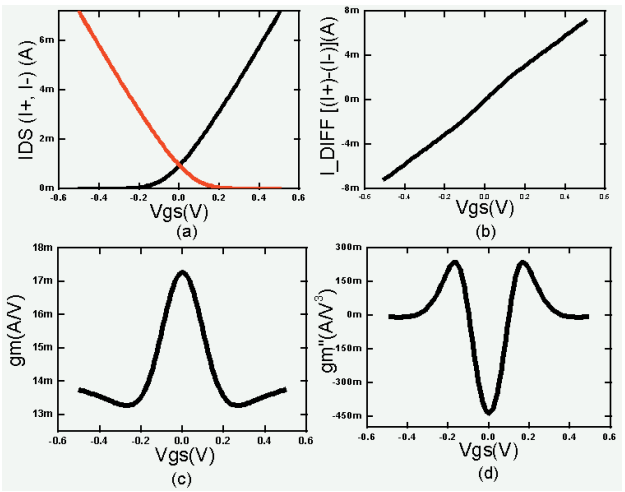

Fig. 2-B PDA current and its derivative's behaviors. (a) PDA branch currents, I+, I-, (b) differential current, [(I+)-(I-)], (c) gm of differential current, (d) gm″ of differential current.

negative value of gm″ can not be moved to positive value by changing the bias condition as shown in Fig. 3 (a), (b). However, in the case of PDA case it can be moved to positive value by changing the bias voltage as shown in Fig. 3 (c), (d). Because in FDA, two branch currents (I+, I-) always meet at the center of the I-V curve irrespective of the bias condition of tail current source as shown Fig. 3 (a), (b). While in PDA, those two currents can meet at any point, depending on the bias voltage as shown Fig. 3 (c), (d). That means in PDA, its negative value of gm″ of differential current can be moved to a positive value by changing the bias voltage from saturation to near

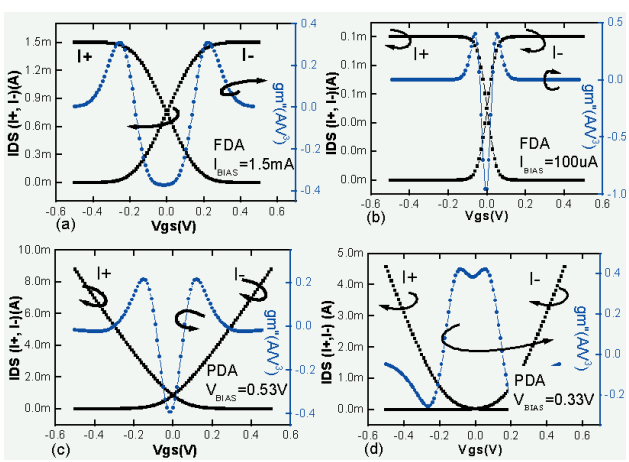

Fig. 3. (a) FDA current and gm″ at high current bias region. (b) FDA current and gm″ at low current bias region. (c) PDA current and gm″ at saturation region. (d) PDA branch current and gm″ at weak inversion region.

threshold regime. From the above consideration, the negative value of gm″ which degrades linearity in FDA can be compensated with a positive value of gm″ in PDA by adjusting the bias and transistor size of PDA. This method does not require extra power consumption, as the PDA for compensating gm″ is biased at near threshold voltage regime. Here, we propose a new high linearity differential amplifier, Differential Multiple Gated (DMGTR) amplifier using FDA as the main amplifier and PDA as the auxiliary amplifier. Because most of the signal is amplified by main amplifier, the benefit of differential circuits like high CMRR, is still maintained. Also the RF characteristics, like NF, gain are not degraded in proposed amplifier. Fig. 4 shows (a) the DMGTR amplifier and (b) gm″ linearization by the proposed method. Linearization window is wide enough to cover possible mass production variations such as process, temperature and supply voltage.

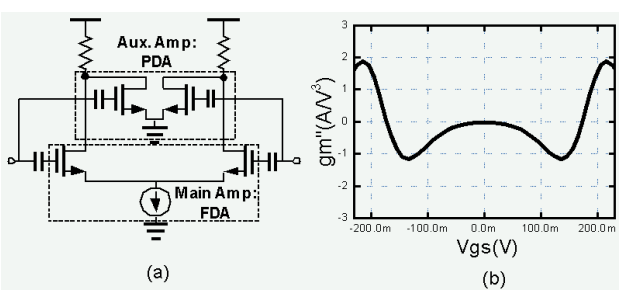

Fig. 4 (a) Proposed DMGTR amplifier schematic diagram. (b) Linearized gm″ range of DMGTR.

RF Programmable Gain Amplifier Architecture

To cover large gain range with fine resolution in RFPGA, gain attenuation is divided into 4 parts as shown in Fig. 5. A 13-bit gain control word is directly assigned to RFPGA and it comprises of a linear 55 dB gain range with 0.25dB resolution. In the first stage, to attain a large gain range, resistive attenuator is used. Previous variable gain amplifiers use a single amplifier with switches [6] or multiple amplifiers without switches [1][7]. The first one requires an input switch even at the highest gain mode, which results in high a NF. And the second one suffers from bandwidth limitation, because of the multi-amplifier configuration. Thus, we find a compromise between both structures using only two amplifiers. Here, we separate the high gain mode amplifier from the low gain mode amplifier, using same amplifier, and with the switch moved back after the amplifier as shown in the resistive attenuator block of Fig. 5. Those first stage amplifiers also perform single to differential conversion, thus removing the off chip balun. This is achieved by combining common source and common gate amplifier as shown in the first amplifier of Fig. 5. Also common gate amplifier provides 50 ohm input impedance. The DMGTR amplifier is used at second stage amplifier which determines overall RFPGA linearity. First and second amplifier have a digitally controlled gain range, to cover the previous gain step, using load impedance switching. Third stage amplifier delivers signal to next stage effectively using source follower.

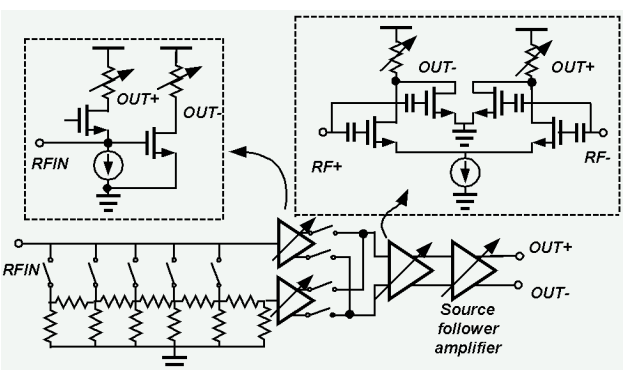

Fig. 5 Proposed RFPGA schematic diagram. To cover large gain range, gain control is divided into 4 parts. For seamless gain rage, previous gain step is covered by the sum of the next gain range.

Measurement Results

A. DMGTR amplifier

Figure 6 shows the photograph of the evaluation board of DMGTR amplifier and RFPGA. 4:1 transformer is used to convert differential input/output into single-ended one for measurement instrument. Figure 7 shows the IIP3 measurement result of conventional FDA and DMGTR amplifier. Input power is –25 dBm and frequency is around 500MHz. With a similar fundamental power, DMGTR decreases third order intermodulation distortion (IMD3) power upto 26 dB, corresponding IIP3 improvement is 13 dB. As a result, FDA shows IIP3 of –3 dBm at 2.8 mA current consumption while DMGTR amplifier shows IIP3 of 10 dBm at 2.9 mA current consumption. NF is 5.7 dB both for FDA and DMGTR amplifier. Gain of FDA is 10 dB and that of DMGTR is 10.1 dB. CMRR of DMGTR amplifier is 23.5 dB while conventional FDA is 28.5 dB. DMGTR improves 13 dB IIP3 at similar power consumption, without sacrificing NF, gain and similar CMRR. Figure 8 shows IIP3 measurement result versus auxiliary amplifier bias current, 40~90 uA bias current of auxiliary amplifier ensure at least 10 dB IIP3 improvement. This shows large enough windows to cover possible mass production variations.

B. RFPGA

Both VHF and UHF RFPGA are implemented using 0.18μm 1P 6M CMOS process and occupies a die area of 0.52 mm^2 (excluding pads). All pins are ESD-protected using the PN diode. As common gate amplifier in first stage amplifier provides 50 ohm input impedance, S11 is under –10 dB over all frequency band. Figure 9 shows full range gain step of 670 MHz. Gain step covers total 55 dB gain range seamlessly with 0.25 dB resolution. Table 1 shows the measurement results of VHF and UHF RFPGA and comparison with VGLNA of previous work, [7]. NF of UHF RFPGA is 4.5 dB and its voltage gain is 25 dB and IIP3 is –4 dBm at 16 mW. In the lowest gain, IIP3 reaches +30 dBm. This work shows 10 dB higher IIP3 at even much lower power consumption (65%) than previous work [7], even though, that work was implemented by bipolar in SiGe BiCMOS technology.

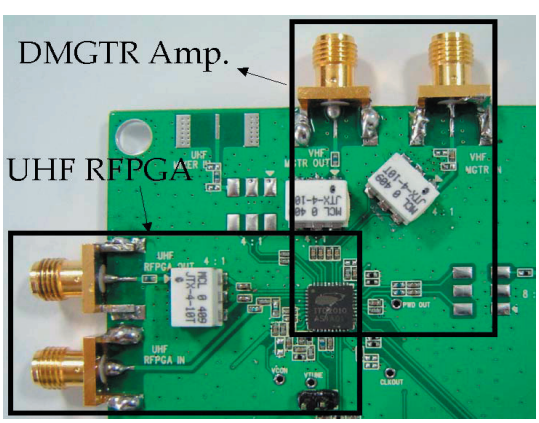

Fig. 6 Measurement board of DMGTR Amplifier and RFPGA.

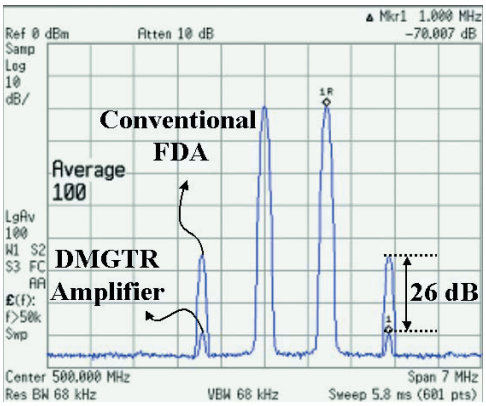

Fig. 7 IIP3 measurement result comparison between conventional FDA and DMGTR amplifier.

Conclusion

A new differential circuit linearity improvement technique, DMGTR is newly proposed, based on analysis of the characteristics of differential current and its derivatives of FDA and PDA, and verified with measurement. Measurement results of DMGTR amplifier show maximum 13 dB improvement of IIP3 without sacrificing other characteristics such as gain, NF and CMRR with wide linearization window. Also, this method does not require extra power consumption.

Employing DMGTR, a low power, low noise and highly linear RFPGA for terrestrial D-TV applications is designed and measured. Also, to cover large gain range with fine step resolution over wide frequency range, new gain control methods are proposed and verified by measurement.

Acknowledgement

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Refereneces

[1] G. Retz and P. Burton, "A CMOS Up-conversion receiver Front-End for Cable and Terrestrial DTV Application." *ISSCC Dig. Tech. Papers*, pp. 442-443, Feb. 2003.

[2] T. Kim, et al., "Highly Linear Receiver Front-End Adopting MOSFET Transconductance Linearization by Multiple Gated Transistor", *IEEE Journal of Solid State Circuits*, No. 1, pp. 223-229, Jan. 2004.

[3] A. Behazad, et al., "A 4.92-5.845 GHz Direct-Conversion CMOS Tranceiver for IEEE 802.11a Wireless LAN" Dig. of papers, *IEEE RFIC symposium*, pp.335-338, Jun. 2004.

[4] Y. Youn, et al. " A 2GHz 16 dBm IIP3 Low Noise Amplifier in 0.25um CMOS Technology," *ISSCC Dig. Tech. Papers,* pp. 452-453, Feb. 2004.

[5] Yongwang Ding et al., "+18 dBm IIP3 LNA in 0.35um CMOS," *ISSCC Dig. Tech. Papers pp.* 162-163, 2001.

[6] B. Gilbert, "A Low-Noise Wideband Variable-Gain Amplifier Using an Interpolated Ladder Attenuator," *ISSCC Dig. Tech. Papers*, pp. 280-281, Feb. 1991.

[7] Shin'ichiro Azuma, et al. "A Digital Terrestrial Television (ISDB-T) Tuner for Mobile Applications," *ISSCC Dig. Tech. Papers*, pp. 278-279, Feb. 2004.

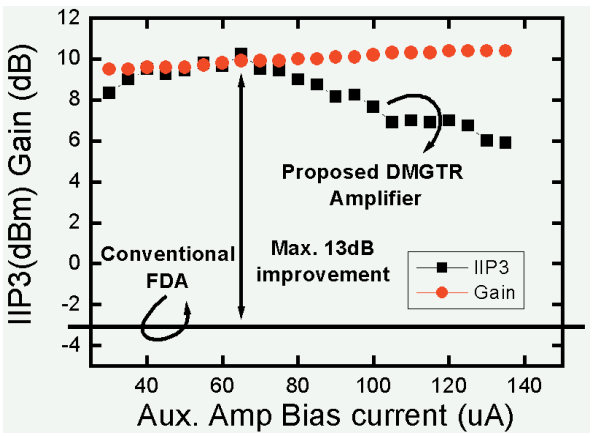

Fig. 8 DMGTR IIP3 measurement result vs. auxiliary amplifier bias. It shows wide linearization window.

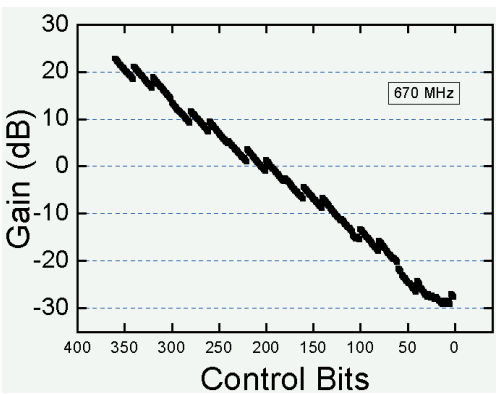

Fig. 9 Gain range measurement result of proposed RFPGA, it covers 55 dB with 0.25 resolution seamlessly.

Table 1. Performances summary of RFPGA and comparison with previous work.

This work, 0.18μm CMOS						
Band	Standard (Frequency, MHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Gain range (dB)	Power (mW)
VHF	DAB/DMB (174~245) ISDB-T 3seg. (190~220)	28	3.0	-5	55	16
UHF	ISDB-T 1seg. (470~770) DVB-H (450~860)	25	4.5	-4	55	16
VGLNA of previous work [7], Bipolar in SiGe BiCMOS						
UHF	ISDB-T 1seg. (470~770)	19	2.7	-14	60	25.23