# Fabrication and characterization of sol-gel-derived zinc oxide thin-film transistor

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(Received 23 November 2009; accepted 1 February 2010)

Thin-film transistors (TFTs) with zinc oxide channel layers were fabricated through a simple and low-cost solution process. Precursor solution concentration, annealing temperature, and the process were controlled for the purpose of improving the electrical properties of ZnO TFTs and analyzed in terms of microstructural scope. The fabricated ZnO films show preferential orientation of the (002) plane, which contributes to enhanced electron conduction and a dense surface. The results show that the TFT characteristics of the film are clearly affected by the microstructure. The optimized TFT operates in a depletion mode, shows *n*-type semiconductor behavior, and is highly transparent (>90%) within the visible light range. It exhibits a channel mobility of 9.4 $cm^2/V{\cdot}s$, a subthreshold slope of 3.3 V/decade, and an on-to-off current ratio greater than $10^5$. In addition, the result of $N_2$ annealing shows the possibility of improvement in electrical property of the ZnO TFTs.

## I. INTRODUCTION

Transparent thin-film transistors (TTFTs) with oxide active channel layers are presently attracting strong interest, from both basic research and industrial fields, in relation to transparent electronics applications, such as flat-panel displays, flexible displays, radiofrequency identification tags, and smart windows.[1–3] TTFTs are considered excellent candidates for the backplane of active-matrix organic light-emitting diodes (AMOLEDs) and active-matrix liquid-crystal displays (AMLCDs), where Si-based materials, which suffer many problems involving stability and large area uniformity, are currently used.[4]

Metal oxide semiconductors offer many advantages such as transparency originating from their large band gap, high uniformity, environmental stability, and high mobility compared with conventional amorphous silicon and organic materials. Many transparent oxide semiconductors (TOSs), such as zinc oxide (ZnO), zinc–tin oxide, indium–zinc oxide, and indium–gallium–zinc oxide, have been reported for transparent channel layers in TTFTs.[2,5–7] They exhibit mobility and an on-to-off current ratio in the range of 5 to 100 $cm^2/V{\cdot}s$ and $10^6$ to $10^7$, respectively. Traditionally, deposition of TOSs relies on vacuum deposition processes such as RF-magnetron sputtering and pulsed laser deposition, which enable a low-temperature process (even at room temperature), but require expensive equipment and incur high fabrication cost.

The sol-gel method, a representative solution-based thin-film deposition technique, offers many benefits over vacuum-based processes: simplicity, high throughput, and low-cost.[8–10] In addition, it enables direct patterning, which could replace conventional photolithographic techniques through ink-jet printing and a roll-to-roll process. Recently, several solution-processed oxide TFTs that showed mobility as high as 16 $cm^2/V{\cdot}s$ and ink-jet printability with an on-to-off current ratio of $10^6$ were reported.[11–13] However, they usually include indium, a rare and expensive material, used for the purpose of improving the electron conduction property.

ZnO is a nontoxic material that has many interesting characteristics, such as piezoelectricity, ferroelectric property, and *n*-type conductivity.[14–16] Because of these properties, it is the one of the most widely used oxide materials in various active and passive devices, including piezoelectric devices, gas sensors, surface acoustic wave devices, and transparent electrodes.[17,18] Furthermore, ZnO has been studied as a semiconducting material and is currently attracting significant attention.[19,20] For TFT applications in displays, the wide band gap of ZnO offers additional benefits. Because ZnO does not interact with visible light due to its wide band gap, i.e., more than 3.2 eV, it is expected that the characteristics of ZnO TFTs will not be degraded upon exposure to visible light, whereas amorphous Si TFTs deteriorate.[21,22] Therefore, an additional shield for the active channel layer from visible light is not required, thereby making possible a transparent TFT having a simple structure. In turn, it allows a higher aperture ratio of active matrix arrays.

In the present study, intrinsic ZnO, one of the most abundant materials, is studied as a channel layer. The ZnO film is prepared by a sol-gel process, a cost-effective method for preparing large-area uniform films. Various

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DOI: 10.1557/JMR.2010.0103

  

conditions are carefully controlled and systematically studied, from synthesis of the precursor solution to annealing processes, to investigate the effects of each process. The effects of the process conditions are studied from the viewpoint of the electrical properties and structure of the film.

## II. EXPERIMENTAL PROCEDURE

The metal precursor solution for the ZnO channel layer was prepared by dissolving zinc acetate dihydrate [$Zn(CH_3COO)_2{\cdot}2H_2O$, Aldrich, St. Louis, MO] in 2-methoxyethanol [$CH_3OCH_2CH_2OH$, Aldrich], where the concentration of zinc acetate was 0.3 M (except for effects of precursor concentration section). To form a stable solution, the zinc acetate precursor was chelated with ethanolamine (MEA, $NH_2CH_2CH_2OH$, Aldrich). The solution was stirred at room temperature for 2 h to make a transparent and homogeneous solution. After sufficient reaction, the solution was filtered through a 0.22 μm syringe filter [poly(tetrafluoroethylene), GE] and spin coated at a speed of 5000 rpm atop a $SiO_2$/Si substrate ($\langle 100 \rangle$ orientation) for 30 s. The oxygen plasma treatment was applied immediately before the spin coating to remove unnecessary organics. A 100 nm thick $SiO_2$ layer, which serves as a gate dielectric, was thermally grown on the top of a heavily boron (p+) doped silicon wafer. After film deposition, two-step annealing processes were followed. The films were heat treated at 200 °C for 3 min to evaporate residual solvent, and the main annealing process was then applied. After annealing, 100 nm thick Al source/drain electrodes was deposited using e-beam evaporator under a pressure of $1 \times 10^{-6}$ Torr.

The structural and electrical properties of the ZnO thin films were characterized using various analyzing tools. An x-ray diffractometer (XRD; Rigaku, Tokyo, Japan) with θ–2θ mode was used to investigate the crystallinity and crystal orientation of the film. The electrical property of ZnO TFTs was analyzed using a HP 4145B semiconductor parameter analyzer and probe station.

## III. RESULTS AND DISCUSSION

### A. Themogravimetric analysis

Investigation of the proper heat treatment temperature was performed by a thermogravimetric analysis (TGA; TA Instrument Q50, New Castle, DE) under air at a heating rate of 5 °C/min. The resultant TGA curve of the metal precursor solution, dried at 135 °C to remove the solvent, is displayed in Fig. 1. The initial weight loss below 150 °C originates from evaporation of the residual solvent (i.e., 2-methoxyethanol). The abrupt weight loss around 200 to 300 °C is attributed to decomposition of zinc acetate dihydrate, and the thermal decomposition was completed before 350 °C was reached. This suggests that 400 °C would be a sufficient temperature for thermal decomposition of the metal–organic precursor and to fabricate ZnO film.

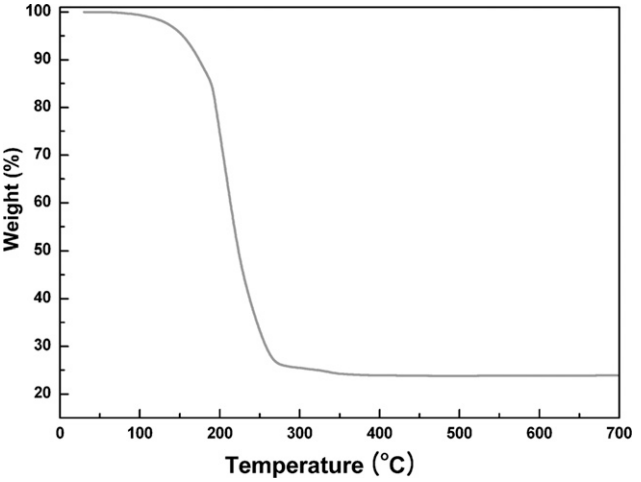


FIG. 1. TGA of ZnO precursor solution under air at a heating rate of 5 °C/min.

### B. Effects of precursor concentration

To investigate the effects of the concentration of the zinc acetate dihydrate precursor in the precursor solutions, the concentration was controlled at 0.3, 0.5, 0.7, and 1.0 M, and the spin-coated film was annealed at 500 °C for 1 h under ambient surroundings. Figure 2(a) shows the drain current versus drain-to-source voltage ($I_D$–$V_{DS}$) output characteristic of the ZnO TFT with a concentration of 0.3 M at various gate voltages ($V_G$). The transfer characteristic, $I_D$ versus $V_G$ at a fixed $V_{DS}$ = 40 V, is displayed in Fig. 2(b). As the concentration of the precursor increases the on current and off current increase in the cases of 0.3, 0.5, and 0.7 M. In the case of 1.0 M, however, the transfer curve shows abnormal behavior: a decrease of the on current and off current was observed. Switching devices such as TFTs require several specificities for better performance, such as a high on-to-off current ratio for precise operation and reducing error, high mobility for faster device operation, and low off current to reduce the power consumption at the off state.[23] In the transfer curve, the case of 0.3 M concentration showed the best switching property with reasonable on current. Thus, it is natural to conclude that 0.3 M is a suitable concentration in terms of TFT applications.

Figure 3 shows the XRD patterns obtained with different concentrations of the precursor in the solutions. The peak shown at ~33° is attributed to the silicon substrate. In the cases of 0.3, 0.5, and 0.7 M concentration, a (002) plane peak appearing at 34.4° is dominant. As the concentration increases, the intensity of the peak increases since thickness of the film gets thicker, in the case of 0.3, 0.5, and 0.7 M concentration. It is believed that the increase of the on and off current are attributed to thicker

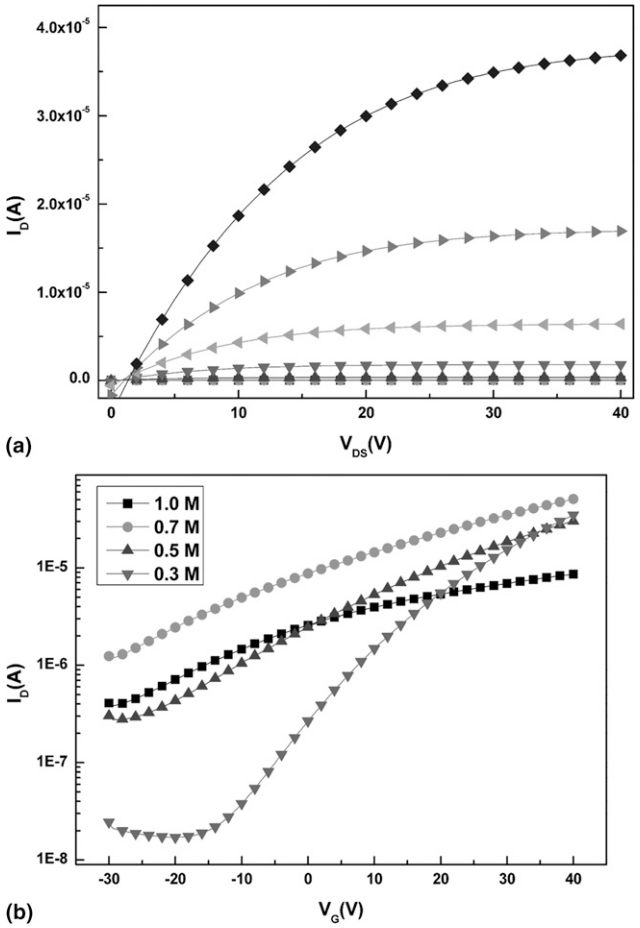


FIG. 2. (a) Plot of drain current, $I_D$, versus drain voltage, $V_D$, of the ZnO TFT using 0.3 M precursor solution with various gate voltages, $V_G$. (b) Plots of drain current, $I_D$, versus drain voltage, $V_G$, of the ZnO TFT with various precursor concentration for $V_{DS}$ = 40 V with structure of $L$ = 120 μm and $W$ = 1000 μm.

film, which has larger amount of carrier than thinner film. The abnormal behavior observed for the case of 1.0 M concentration can also be explained by the XRD pattern. In the case of 1.0 M, preferential orientation of the (002) plane was broken and growth of a (101) plane, shown at 36.3°, was observed. The results indicate that the film's microstructure (i.e., crystallinity and crystal orientation), originating from the concentration of precursor in the precursor solution, clearly affects the electrical property.

### C. Effects of annealing temperature

Figure 4(a) shows the output characteristics of a ZnO TFT annealed at 600 °C. The transfer characteristics of ZnO TFTs obtained using a 0.3 M precursor solution with different annealing temperatures, i.e., 400, 500, and 600 °C, for 1 h in an oxygen atmosphere are displayed in Fig. 4(b). In the cases of 400 and 500 °C annealing, both the on current and off current are

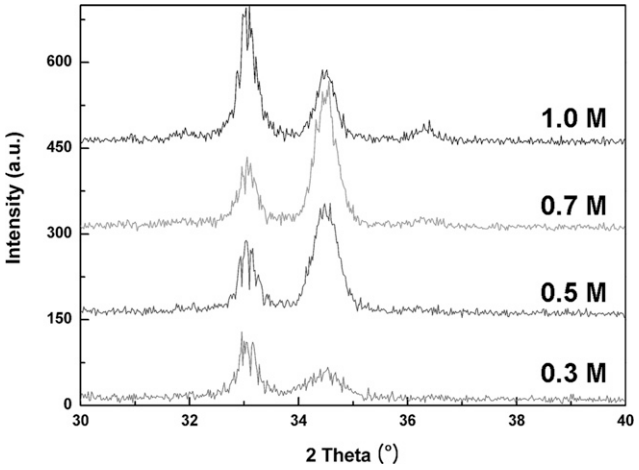


FIG. 3. θ–2θ XRD analysis of ZnO thin films with various precursor concentration on $SiO_2$/Si substrate.

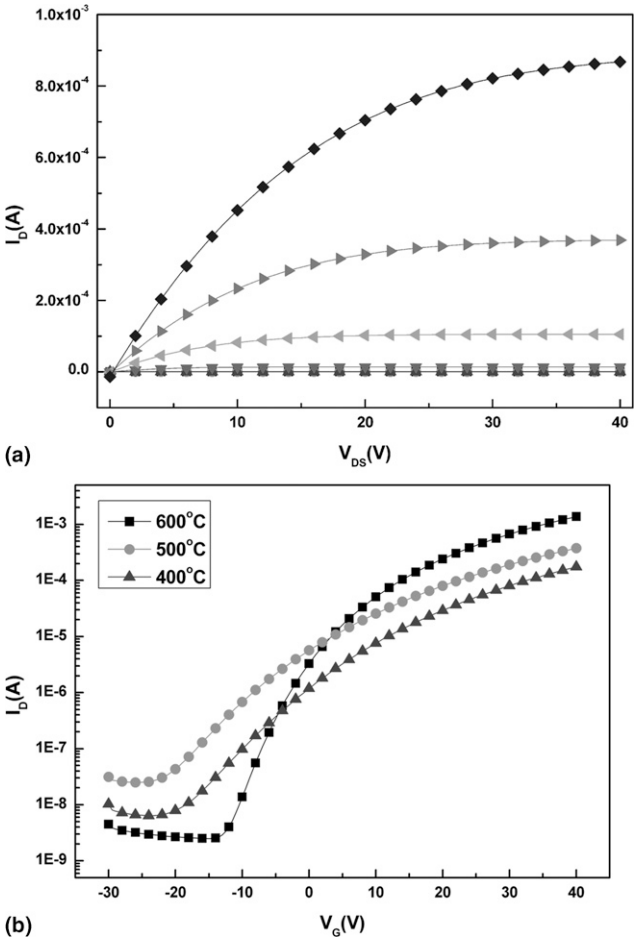


FIG. 4. (a) Plot of drain current, $I_D$, versus drain voltage, $V_D$, of the ZnO TFT annealed at 600 °C with various gate voltages. (b) Plots of drain current, $I_D$, versus drain voltage, $V_G$, of the ZnO TFTs annealed at different temperature for $V_{DS}$ = 40 V with structure of $L$ = 120 μm and W = 1000 μm.

increased with similar subthreshold slopes. It is known that the subthreshold slope is generally related to defects of the film and the interface property between the semiconductor and gate dielectric.[6] The XRD patterns displayed in Fig. 5 indicate that all the films show preferential orientation of the (002) plane, which contributes to enhanced electron conduction.[20] The increasing intensity of XRD peak at 34.4° with higher annealing temperature indicates that the crystallinity is improved as the annealing temperature is increased. Therefore, it is reasonable to conclude that the property of films and the interface are similar for both cases and the better on current in the 500 °C annealed film is attributed to the superior crystallinity of the film. However, the 600 °C annealed film shows higher on current, lower off current, and a lower subthreshold slope at the same time, features that are preferable for TFT application. The abrupt improvement of the electrical properties in terms of mobility and subthreshold slope of the film annealed in a temperature range between 500 and 600 °C reflects improvements of the interface between the semiconductor and gate dielectric and the defect level in the film as well as better crystallinity.[6]

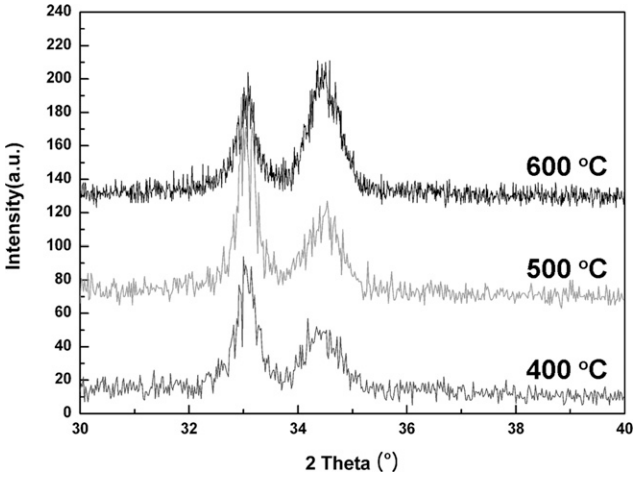


FIG. 5. θ–2θ XRD analysis of ZnO thin films on $SiO_2$/Si substrate annealed at different temperature.

TABLE I. Electrical properties of ZnO TFTs annealed at different temperature.

| Temperature (°C) | μ ($cm^2$/V·s) | $I_{on}/I_{off}$ | $V_{th}$ (V) | $S$ (V/dec) |
|---|---|---|---|---|
| 400 | 1.44 | $\sim 10^4$ | ~8 | ~7 |
| 500 | 2.55 | $\sim 10^4$ | ~6 | ~7 |
| 600 | 9.40 | $5.5 \times 10^5$ | 7.19 | 3.29 |

The electrical properties of the devices were analyzed using a HP 4145B semiconductor parameter analyzer in a dark room at ambient conditions. The channel length and width were 120 and 1000 μm, respectively. The electrical parameters that characterize TFTs are typically channel mobility, threshold voltage, subthreshold slope, and on-to-off current ratio. Channel mobility and threshold voltage are derived from a linear fitting to the plot of the square root of drain current, $I_D$, versus drain voltage, $V_G$, using the following equation in the saturation region.

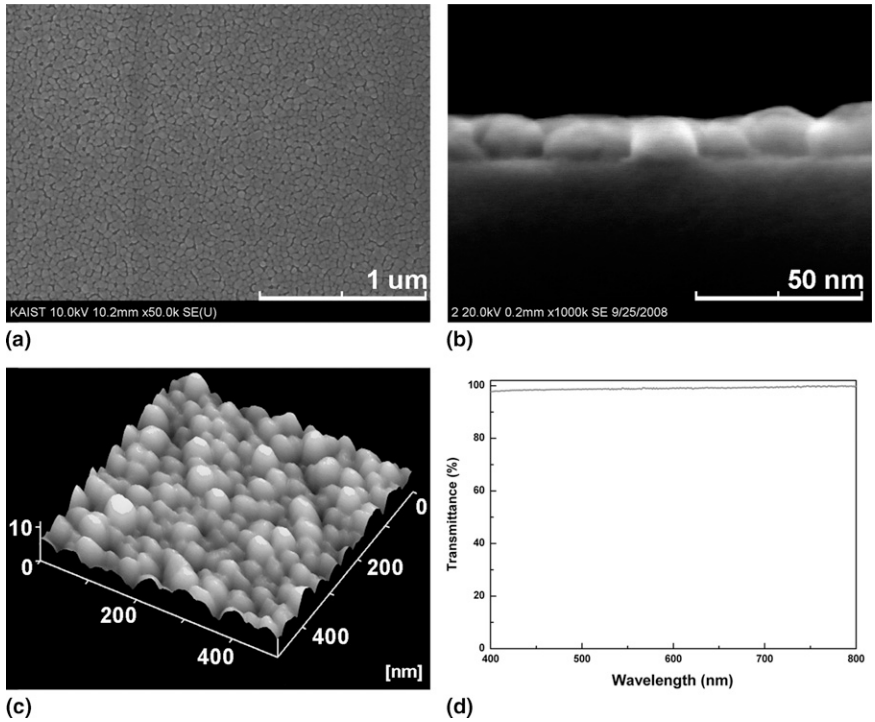


FIG. 6. SEM image of (a) surface and (b) cross section of ZnO thin film. (c) AFM image of ZnO thin film. (d) Transmittance spectra of ZnO thin film deposited on quartz substrate.

$$I_D = \frac{WC_i}{2L}\mu(V_G - V_{th})^2 \quad ,$$

where $W$ and $L$ are the channel width and length, respectively, $\mu$ is the channel mobility, $C_i$ is the capacitance per unit area of a $SiO_2$ gate insulator (dielectric constant $\approx 3.9$), and $V_{th}$ is the threshold voltage.

In quantifying the performance of a semiconductor channel layer, specifically in terms of current-driving capability and switching frequency, the most important TFT electrical property is channel mobility. The optimized resulting channel mobility is $\mu = 9.40$ cm$^2$/V·s and shows *n*-type semiconductor behavior. The threshold voltage is 7.2 V, the subthreshold slope is 3.3 V/decade, and the on-to-off current ratio is about $5.5 \times 10^5$, which is comparable to results obtained with vacuum processing with a low off current of $4.5 \times 10^{-9}$, as seen in Table I. The results suggest that high-temperature annealing over 500 °C is required for better TFT performance in solution processed ZnO thin films.

The SEM and AFM images, displayed in Figs. 6(a)–6(c), show that the fabricated ZnO film is dense and well crystallized with 600 °C annealing. The cross-sectional view of the film indicates that the thickness of the film is ~15 nm. The UV–vis spectra, displayed in Fig. 6(d), shows that the resultant film is transparent (>90%) within the visible region.

### D. Effects of postannealing

The *n*-type conductivity in nonstoichiometric ZnO is known to originate from oxygen vacancies and zinc interstitials.[17] Oxygen vacancies act as shallow *n*-type dopants in ZnO materials and increase electron conduction ability. In the case of solution-processed ZnO, oxygen vacancies are usually controlled by additional annealing or plasma treatment.[24] An additional post-heat-treatment process was performed in a nitrogen atmosphere at 500 °C for 1 h for the purpose of improving the electron conduction property of the ZnO thin film by increasing the amount of oxygen vacancies. The transfer curves, presented in Fig. 7(a), show the decisive effect of heat treatment in a $N_2$ environment. Increase of the on and off current with similar subthreshold slope (i.e., ~8 V/decade) is observed compared with the result without a post-heat-treatment process. The calculated channel mobility and on-to-off current ratio are $\mu = 6.40$ cm$^2$/V·s and ~$10^3$, respectively. The similar subthreshold slope indicates that the defect level of the film and the interface property between the semiconductor and gate dielectric is similar for both cases. The XRD patterns, displayed in Fig. 7, indicate that the post-heat-treated thin film shows slightly higher crystallinity that can be judged by higher XRD peak intensity than untreated thin film. The result explains the reason of

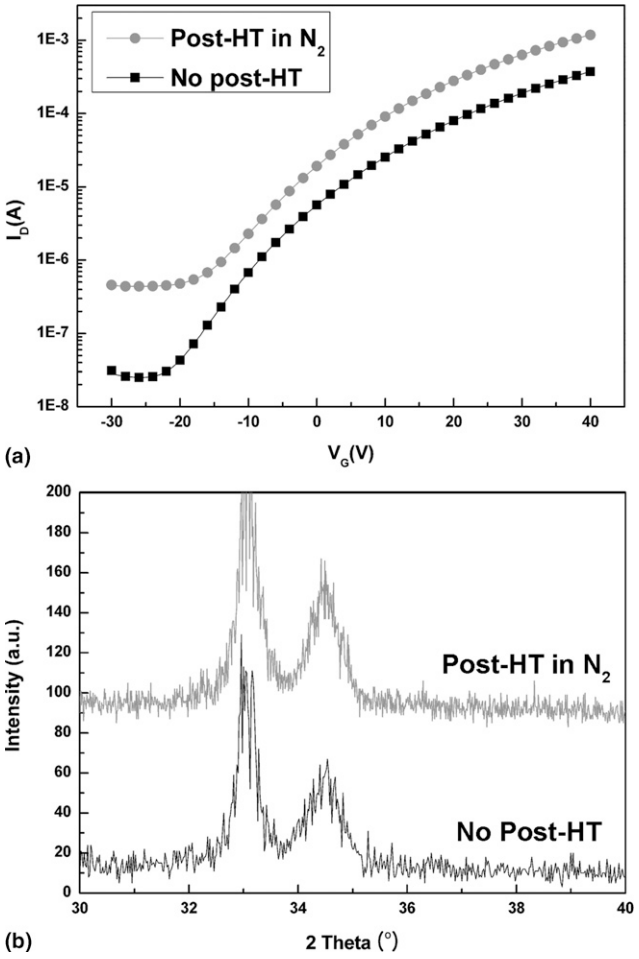


FIG. 7. (a) Plot of drain current, $I_D$, versus drain voltage, $V_D$, of the ZnO TFTs with $N_2$ postannealing and no post-heat-treatment for $V_{DS}$ = 40 V with structure of $L$ = 120 μm and $W$ = 1000 μm. (b) θ–2θ XRD analysis of ZnO thin films with $N_2$ heat treatment and no post-heat-treatment on $SiO_2$/Si substrate.

higher conductivity with post heat treatment. The better crystallinity of the post-heat-treated film indicates that the crystallinity is improved with longer annealing at the same temperature. However, postannealing under a $N_2$ atmosphere generates additional oxygen vacancies and increases the carrier concentration at the top region of the channel, resulting in a high off current. The results reflect the possibility of improving the conductivity of the film by postannealing under a $N_2$ atmosphere.

## IV. CONCLUSIONS

We have investigated highly transparent ZnO TFTs fabricated via a simple and low-cost solution process. The optimized conditions were 0.3 M concentration of precursor solution and 600 °C annealing. The fabricated films show preferential orientation of the (002) plane, which contributes to enhanced electron conduction and a dense surface. The results show that the microstructure

of the film is clearly related to the electrical property. Improvements of the film crystallinity and the interface between the semiconductor and gate dielectric are observed at high annealing temperature. It is shown that an additional postannealing process in $N_2$ surrounding can improve the electron conduction property of the film. The optimized ZnO TFT shows sufficient electrical properties to drive various display devices, such as AMLCDs and AMOLEDs.

## ACKNOWLEDGMENTS

This research was financially supported by the Ministry of Knowledge Economy (MKE) and Korea Institute for Advancement of Technology (KIAT) through the Human Resource Training Project for Strategic Technology. This work was also supported by Basic Science Research Program through National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (Grant No. R11-2007-045-03002-0).

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