A Wide-Band CMOS Variable-Gain Low Noise Amplifier for Multi-Standard Terrestrial and Cable TV Tuner

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Abstract **— A CMOS wide-band low noise amplifier (LNA) based on the current amplification for the multi-standard terrestrial and cable tuner is proposed. Conventional wide-band LNAs suffer from the tradeoff between noise figure and wide-band input matching. By adopting the structure combined the common source (CS) amplifier with the common gate (CG) amplifier by the current amplification, the noise figure does not have any influence on wide-band input matching so that we can achieve low noise figure by the noise canceling and excellent wide-band input matching at the same time while allowing some variable gains. The proposed LNA is fabricated in 0.18-μm CMOS process and achieves a power gain of +15.5~-5.5 dB, an average noise figure of 3.6 dB, an IIP3 of -1 dBm at the maximum gain, and S11 of -15 dB. The power consumption is 50.4 mW and chip area is 0.54 mm².**

Index Terms **— Terrestrial, cable, tuner, common gate amplifier, common source amplifier, low noise amplifier, current amplification, wide-band, noise canceling**

I. Introduction

Modern TV receivers (called tuner) and set-top boxes require universal tuners capable of processing analog and digital, terrestrial, and cable broadcast [1]. The required tuner needs to handle signals with input frequency from 54 MHz to 880 MHz, because the cable standard have up to 137 analog and digital channels with channel spacing of 6 MHz within the frequency band.

For high integrated tuners, wide-band LNAs not only require sufficiently high gain and low noise figure (NF) but also high linearity and flat frequency response over 54~880 MHz. Also the input impedance must be well matched to the source impedance within the frequency range of interest to transfer the maximum power and avoid the signal reflection on a cable. In case of the cable system (without a tracking filter), because hundreds of broadcast channels are coming into the LNA without any filtering, it must have high linearity and its linearity specification is represented by the Composite Triple Beat (CTB) and Composite Second Order (CSO) distortion [2]. These requirements should be achieved over a wide range of frequency while allowing some variable gain to handle interferes generated by strong adjacent channels [3].

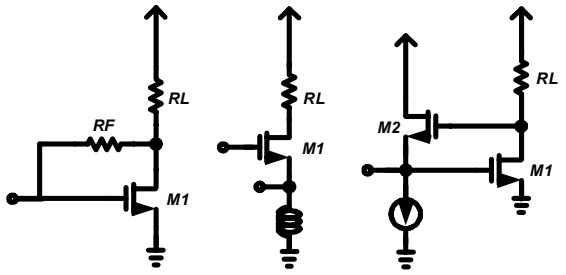

Fig. 1. (a) Resistive shunt feedback amplifier. (b) Common gate amplifier. (c) Common drain feedback amplifier.

In this paper, a CMOS wide-band LNA suitable for the analog and digital terrestrial and cable tuner is presented.

By adopting the structure combined the CS amplifier with the CG amplifier by the current mirror, the proposed differential LNA has low noise figure by the noise canceling [3] and excellent wide-band input matching at the same time while allowing the three step variable gains.

II. Review of Conventional Wide-Band LNAs

The widely used amplifier that can achieve the wide-band input matching as well as flat and moderate gain over a wide operating frequency is the resistive shunt feedback amplifier, common gate amplifier, and common drain feedback amplifier.

Although the CG amplifier (Fig. 1.b) can achieve wide-band 50 ohm input impedance, its noise figure easily goes beyond 4 dB due to the short channel device. For the Gm-boosted CG LNA [4], its noise factor is reduced by 1/(1+A) compared to the conventional CG LNA. Since the amplifier with gain A may also introduce noise, the Gm-boosting technique is only useful in the differential topology that A=1 is easily achieved by just cross-coupling the inputs.

In case of the resistive shunt feedback amplifier (Fig. 1.a) [5] [6], its noise factor (ignoring the noise contributed by R_F and R_L) is

$$F = 1 + \frac{R_S}{R_F}\left(1 + \frac{1}{g_{m1}R_S}\right)^2 + \frac{\gamma}{\alpha g_{m1}R_S}. \quad (1)$$

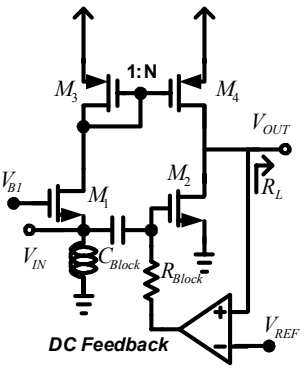

Fig. 2. Schematic of the proposed LNA with the structure combined the common source amplifier with the common gate amplifier by the current mirror.

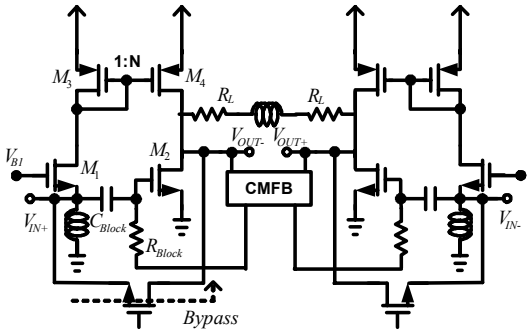

Fig. 3. Complete circuit schematic of the proposed LNA.

A large feedback resistor (R_F) is required for low noise. This can degrade the gain flatness and prevent moderate trade-off between the gain and linearity over the operating frequency range. The size of the capacitor used in the cascode shunt feedback becomes very large in the VHF-L region, so it becomes hard to integrate the feedback capacitor on the single chip. This is probably why the operating frequency of [5] begins at 500 MHz.

Another common method to implement a wide-band LNA is to use the common drain feedback (Fig. 1.c). Its input impedance is

$$Z_{IN} = \frac{1}{g_{m2}} \frac{1}{1+g_{m1}R_L} \tag{2}$$

and the noise factor is

$$F = 1+\frac{2}{3}g_{m2}R_S+(\frac{1}{R_L}+\frac{2}{3}g_{m1})\frac{(1+g_{m2}R_S)^2}{g_{m1}^2R_S}. \tag{3}$$

In order to achieve the input matching and low noise figure, g_{m2} should be decreased as much as possible and this degrades linearity considerably after all due to the nonlinearity of the transistor M2 as known in [7].

III. LNA Circuit Design

The proposed wide-band LNA combines the CS amplifier and the CG amplifier based on the current mirror. Its schematic is shown in Fig. 2.

A. Wide-Band Input Matching and Gain

The input impedance of the proposed LNA is determined as the trans-conductance of the input transistor M1 and can be approximately described as

$$Z_{IN} = \frac{1}{g_{m1}}. \tag{4}$$

The gain of the LNA shown in Fig. 2 is presented by the sum of the CG amplifier gain term and current mirroring ratio N, and the CS amplifier gain term. When the input impedance of the LNA is matched well to the source impedance ($Z_{IN} = R_S$), the gain can be obtained as

$$G|_{Z_{IN}=R_S} = -\frac{1}{2}(g_{m1}N+g_{m2})R_L \tag{5}$$

where g_{m2} is the trans-conductance of the transistor M2, R_L is the load resistor and N is the scaling ratio of the two current mirrors, M3 and M4. Note that by increasing g_{m2} or N, we can obtain a margin that boosts high gain of LNA and low noise figure without regarding the input matching condition compared to the conventional LNAs. Considering the limited bandwidth of the simple current mirror given by ω_T / N, where ω_T is the unit gain frequency of a current mirror transistor and N is the scaling ratio of the two current mirror [8], the proper scaling ratio value of N should be carefully selected and we use on-chip peaking inductor at output load to increase bandwidth.

B. Noise

The noise factor (only by M1, M2, M3 and M4) in input matched condition is represented as follows

$$F = \frac{(1+m^2)}{(1+m)^2}+\frac{(1+m^2)}{(1+m)^2}\frac{\gamma}{\alpha_1}+\gamma\frac{1}{N}(1+N\frac{g_{m3}}{g_{m1}}) \tag{6}$$

where m is $g_{m1}N/g_{m2}$, α_1 is g_{m1}/g_{do1}, γ is the transistor channel thermal noise factor, g_{m3} is the trans-conductance of the PMOS M3. In this equation, we can find that the thermal noise generated by the CG amplifier input transistor (M1) is cancelled by $(1+m^2)/(1+m)^2$ at the output node. This results from the feed-forward noise canceling [3] by the two paths, which are the CG and CS amplifier paths.

Since $(1+m^2)/(1+m)^2$ can be a minimum value of 1/2

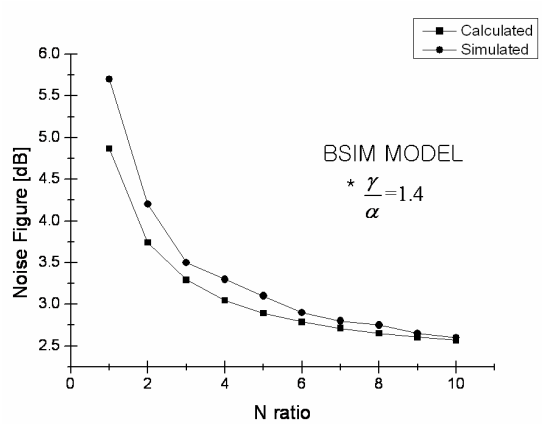

Fig. 4. Calculated noise figure Vs simulated noise figure of the proposed LNA on variable mirroring ratio N value.

at m=1, when the gain of CG amplifier with current amplification ($g_{m1}N$) is equal to the gain by the CS amplifier (g_{m2}), we can obtain the maximal noise canceling effect and at this time the noise factor of the proposed LNA is

$$F = \frac{1}{2} + \frac{1}{2}\frac{\gamma}{\alpha_1} + \gamma\frac{1}{N}\left(1 + N\frac{g_{m3}}{g_{m1}}\right). \quad (7)$$

Considering the mobility and width of the NMOS and PMOS, we can design such that the trans-conductance of M1 is almost three times larger than the trans-conductance of M3. Using the BSIM model, we can compare the calculated noise factor value with the simulated noise factor value by varying the current mirror ratio N as shown in Fig. 4, and show that these two results are almost similar. We set the maximum value of N as 6 because of the bandwidth of the current mirror mentioned above and DC power consumption.

C. Linearity

It is known that the differential topology can mitigate the effects of the common mode noise such as the clock switching noise and the LO spurs. Also, to meet the CSO specification of the cable system, the required second-order input-referred intercept point (IIP2) of the LNA is 40 dBm or higher at the gain mode of about 14 dB [2]. It is very hard to satisfy the above IIP2 specification in the single circuit structure as known in [3] [10]. Thus we choose the fully differential circuit structure as shown in Fig. 3, even if DC power consumption increases more than twice as much and the noise figure is slightly degraded. Although even-order distortions (IMD2) can easily be reduced by using the differential structure, it is difficult to reduce the third-order distortions (IMD3).

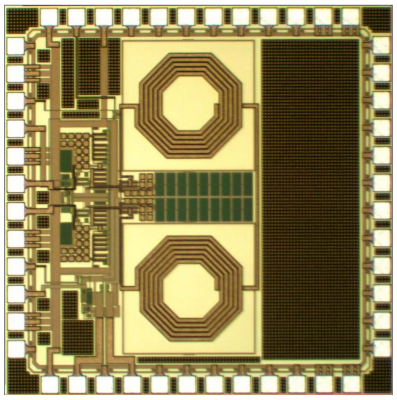

Fig. 5. Chip micro-photograph of the proposed LNA.

Many researches to increase IIP3 without extra power consumption were accomplished as reported in [9]. However, these researches were done only in narrow-band systems such as Zig-Bee, CDMA, and T-DMB and it is difficult to apply for the wide-band system because of the variation of frequency. We can have relatively high IIP3 over wide-band through the use of current amplification, which can eliminate V-I converters that result in non-linearity (IMD3). The acquired IIP3 is approximately between the IIP3 of the CG amplifier (M1) and that of the CS amplifier (M2).

D. Gain Control

In order to handle multiple distortions generated by strong adjacent channels, we have the three-step gain control. Since the fine gain step helps to relax other following stage's linearity burden [9], the next block of a wide-band LNA, which is the RF programmable gain amplifier, must fill the gap between the rough gain steps of wide-band LNA. Changing the current mirror ratio N by the switch control, we can make high and mid gain mode holding on the OIP3 of the LNA. In the case of signal coming into the system with average power over 0 dBm, the LNA should be operated as power down mode, and bypass the input signal into the next block, the RF programmable gain amplifier.

VI. Measurement Results

The circuit was implemented in the TSMC 0.18-μm CMOS technology. Fig. 5 shows the chip micro-photograph of the proposed LNA. Chip-on-board (COB) measurements were performed in the 54~880 MHz frequency band. Wide-band 1:1 baluns of M/A-COM's MABACT0060 are employed for the single-ended 50 ohm termination to differential transformation of the input and output. The power gain and input matching results of the

TABLE I
PERFORMANCE SUMMARY OF THE PUBLISHED WIDE-BAND LNAS AND PROPOSED WIDE-BAND LNA

	Bruccoleri [3]	Huang [6]	Shuzuo Lou [7]	Bruccoleri [10]	This Work
3-dB BW [MHz]	2 ~ 1600	40 ~ 900	54 ~ 880	50 ~ 900	54 ~ 880
Max Gain [dB]	13.7	20.3	22 ~ 10	11	15.5
NF @ Max Gain [dB]	2	4	4.2 ~ 6	4.4	3.6
IIP3 (IIP2) @ Max Gain [dBm]	0 (12)	-10.8 ~ -12.7	-21	14.7 (27.4)	-1 (38)
S11 [dB]	-8	-8.5	-8.2	1.6 (VSWR)	-10
Differential / Gain Control	No / No	YES / YES	YES / YES	No / YES	YES / YES
Area [mm^2]	0.075	0.57	0.7	0.06	0.54
Technology	0.25μm CMOS	0.18μm CMOS	0.18μm CMOS	0.35μm CMOS	0.18μm CMOS
Power Consumption	14mA @ 2.5V	24mA @ 1.8V	23mA @ 1.8V	1.5mA @ 3.3V	28mA @ 1.8V

proposed LNA are shown in Fig. 6 and 7, respectively. The input reflection coefficient is under -10 dB from 54 MHz to 880 MHz without regarding the gain control mode. After de-embedding of the balun, PCB, and interconnection loss, which is 0.5 dB at 54 MHz and 2.6 dB at 880 MHz, the 3-dB bandwidth of the proposed LNA is above 900 MHz. Fig. 6 shows the measured noise figure of the proposed LNA. The average noise figure from 54 MHz to 880 MHz is 3.6, 7.7, and 12.2 dB at the high, mid, and low gain mode respectively. The noise figure of high gain mode is slightly larger than the calculated and simulated noise figure by 0.8 dB and this discrepancy results from the output buffer added for testing.

The two-tone measurement for inter-modulation distortion is done for the proposed LNA over the operating frequency. The IIP3 is -1 dBm and the IIP2 is +38 dBm at high gain mode in the 460 MHz region. Although the IIP3 varies over the operating frequency and the gain mode, we can see that the OIP3 is almost constant. The measured performances of the LNA are summarized and compared with the previously reported wide-band LNAs in Table I.

V. CONCLUSION

A 54~880 MHz CMOS broadband differential LNA combining the CS amplifier and the CG amplifier based on the current amplification has been demonstrated. We can break the fundamental trade-off between the noise figure and the input matching of the traditional LNAs. This makes it possible to achieve low noise figure by noise canceling and excellent wide-band input matching at the same time while allowing the three step variable gains.

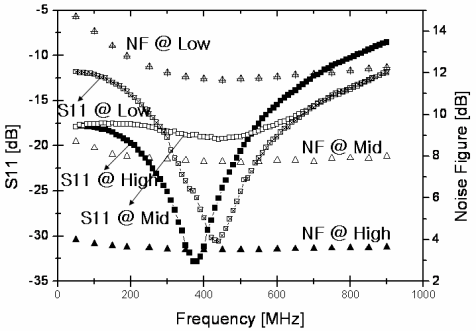

Fig. 6. Measured S11 and noise figure of the proposed LNA.

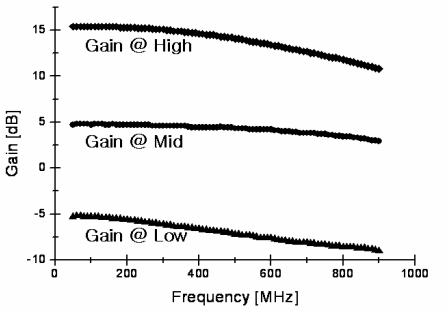

Fig. 7. Measured power gain of the proposed LNA.

The LNA shows a power gain of 15.5 ~ -5.5 dB, an average noise figure of 3.6 dB, and an IIP3 of -1 dBm at 50.4 mW power consumption and 0.54 mm^2 chip area.

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