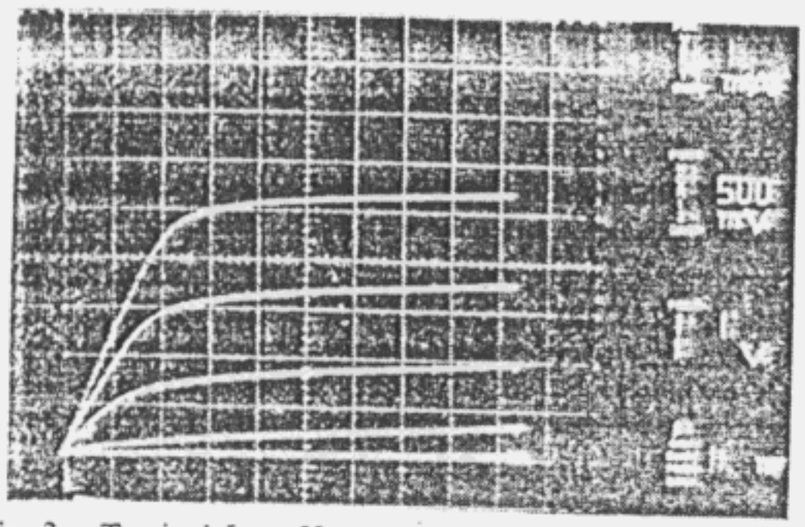

Fig. 3. Typical I_{DS}-V_{DS} curves of the fabricated FET.

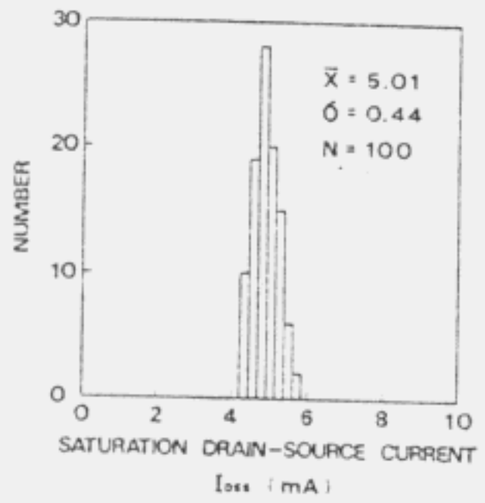

Fig. 4. Histogram of the saturation drain-source current of the experimental FET. L = 1.2 μm, W = 20 μm.

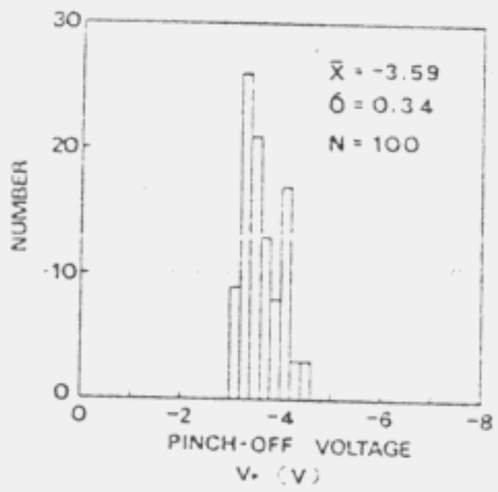

Fig. 5. Histogram of the pinchoff voltage of the experimental FET. L = 1.2 μm, W = 20 μm.

new structure possesses the MBE as-grown uniformity of the active layer thickness even after the gate recesses are formed.

The source resistance of a present experimental device is 56 Ω, namely 1.12 Ω/mm, which is about 50 percent smaller than that of the conventional recessed gate MESFET fabricated with the same design. Because the $Ga_{1-x}Al_xAs$ layer remaining for the sources and drains is so heavily doped that the sheet resistance in the source-gate region as well as the source metal cantact resistance has been effectively lowered. Further reduction of the source resistance will be obtainable by selective dry-etching of the $Ga_{1-x}Al_xAs$ layer, which can suppress the lateral etching.

ACKNOWLEDGEMENT

The authors wish to thank Dr. M. Takeshima for his encouragement throughout this work.

REFERENCES

[1] Y. Nakayama, K. Suyama, H. Shimizu, S. Yokogawa, and A. Shibatomi, "An LSI GaAs DCFL using self-aligned MESFET technology," in *Proc. 4th Ann. GaAs IC Symp.*, p. 6, 1982.
[2] W. V. Mclevige, C. T. M. Chang, and W. M. Duncan, "GaAs enhancement depletion MESFET memory technology," in *Proc. 4th Ann. GaAs IC Symp.*, p. 127, 1982.
[3] B. M. Welch and Y. Shen, "The manufacturability of GaAs integrated circuits," in *Proc. 4th Ann. GaAs IC Symp.*, p. 162, 1982.
[4] K. Asai, K. Kurumada, M. Hirayama, and M. Ohmori, "1 Kb static RAM using self-aligned FET technology," in *ISSCC Dig. Tech. Papers*, p. 46, Feb. 1983.
[5] N. Yokoyama, T. Ohnishi, H. Onodera, T. Shinoki, A. Shibatomi, and H. Ishikawa, "A GaAs 1 K static RAM using tungsten-silicide gate self-alignment technology," in *ISSCC Dig. Tech. Papers*, p. 44, Feb. 1983.

Low Field Mobility in GaAs Ion-Implanted FET's

KANG LEE, MICHAEL S. SHUR, KWYRO LEE, THO T. VU, P. C. T. ROBERTS, AND M. J. HELIX

Abstract—We describe a new technique which allows one to deduce the mobility profiles under the gate of an ion-implanted GaAs MESFET. The technique is based on the measurements of the transconductance and the series resistance at very low drain-to-source voltages. The experimental results show that the mobility drops to about 1000 $cm^2/V \cdot s$ at the channel interface from its maximum value of about 2500 $cm^2/V \cdot s$.

The parameters of GaAs MESFET's are strongly affected by low field mobility, especially in low pinchoff voltage devices [1].

In ion-implanted devices the low field mobility varies with the distance from the gate [2], [3]. *In situ* determination of the mobility profile is important for device modeling and improving MESFET fabrication procedures. Conventional methods [4]–[9] do not allow such in situ mobility profile measurements in 1-μm ion-implanted GaAs FET's.

The technique proposed in this brief is based on the measurements of the transconductance and the series resistance at very low drain-to-source voltages when the Shockley model is applicable. It is a direct method which allows one to determine the mobility profile *in situ* for short gate devices.

We consider a case when the drain-to-source voltage $V_{ds} << V_{Bi} - V_g$ where V_{Bi} is the built-in voltage and V_g is the voltage drop between the gate and the source side of the channel. Therefore the depletion region boundary is nearly parallel to the boundary between the active channel and the substrate. In effect, under such conditions a short-channel device behaves like a fat FET.

The equivalent circuit of the device between the source and drain may be then presented as a series connection of R_s, R_{ch}, and R_d. Here R_s, R_d are the source and drain series resistances, respectively. The reciprocal of the channel resistance R_{ch} for the channel with nonuniform mobility and doping profiles can

Manuscript received July 19, 1983; revised October 19, 1983. This work was supported in part by the Army Research Office and the Microelectronics and Informations Sciences Center at the University of Minnesota.

K. Lee, M. S. Shur, and K. Lee are with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455.
T. T. Vu and P.C.T. Roberts are with Honeywell Systems and Research Center, Minneapolis, MN 55413.
M. J. Helix is with Honeywell Corporate Technology Center, Bloomington, MN 55420.

be expressed as

$$R_{ch}^{-1} = \frac{qW}{L} \int_X^a \mu(X')N(X')\,dX' \tag{1}$$

where q is the electronic charge, a is the thickness of the channel, X is the depletion layer thickness, and L is the gate length. Again, (1) applies only at low V_{ds}.

For a given drain-to-source voltage $V_{ds} = I_d\,(R_s + R_{ch} + R_d)$ and the device transconductance g_m is given by

$$g_m = \frac{\partial I_d}{\partial V_g} = -\frac{V_{ds}}{R_T^2}\frac{\partial R_{ch}}{\partial V_g} \tag{2}$$

where

$$R_T = R_s + R_{ch} + R_d$$

and

$$\frac{\partial R_{ch}}{\partial V_g} = R_{ch}^2\left(\frac{qW\mu N}{L}\right)\frac{\partial X}{\partial V_g}. \tag{3}$$

Here we may also neglect by the voltage drop across R_s compared to V_g so that $V_g \simeq V_{gs}$ (the voltage drop $I_d R_s$ may, however, be comparable to V_{ds}).

The relationship between V_g and depletion layer thickness is given by

$$V_g = V_{Bi} - \frac{q}{\epsilon}\int_0^X X'N(X')dX' \tag{4}$$

where $V_{Bi} \simeq 0.75$ V for our devices. From (4) we find

$$\frac{\partial X}{\partial V_g} = 1\Big/\left(\frac{\partial V_g}{\partial X}\right) = 1\Big/\left(-\frac{q}{\epsilon}\cdot N\cdot X\right) = -\frac{\epsilon}{qNX}. \tag{5}$$

Substituting (5) into (3), we obtain

$$\frac{\partial R_{ch}}{\partial V_g} = -R_{ch}^2\cdot\frac{W\mu\epsilon}{LX}. \tag{6}$$

Combining (2) and (6), we get

$$g_m = \frac{\partial I_d}{\partial V_g} = \frac{\epsilon W V_{ds}}{L}\cdot\frac{\mu}{X}\cdot\left(\frac{R_{ch}}{R_T}\right)^2 = \alpha\cdot\frac{\mu}{X}\cdot\left(\frac{R_{ch}}{R_T}\right)^2 \tag{7}$$

where

$$\alpha = \frac{\epsilon\cdot W\cdot V_{ds}}{L}.$$

In the case when $R_s << R_{ch}$ and $R_d << R_{ch}$ (which is typically not the case for 1-μm GaAs MESFETs with nonself-aligned gates) (7) coincides with the equation for a fat FET derived by Pucel [8].

Our technique is based on the measurement of $g_m(V_g)$ and $R_T(V_g)$ ($R_T = R_s + R_d + R_{ch}$), on the determination of R_s and R_d using the Hower method [12] or [10] (which we modified for the nonuniform doping profile) and on solving (7) numerically together with (4) for the given doping profile.

We start the determination of the series resistance using the Hower method, i.e., we plot the channel resistance R_T versus $1/(1-\sqrt{\eta}\,)$ where $\eta = (V_{Bi} - V_g)/(V_{Bi} - V_T)$ and crudely determine the sum of the series resistances, from the intercept

$$R_T = R_s^{(0)} + R_d^{(0)} + \frac{1}{G_0(1-\sqrt{\eta}\,)}. \tag{8}$$

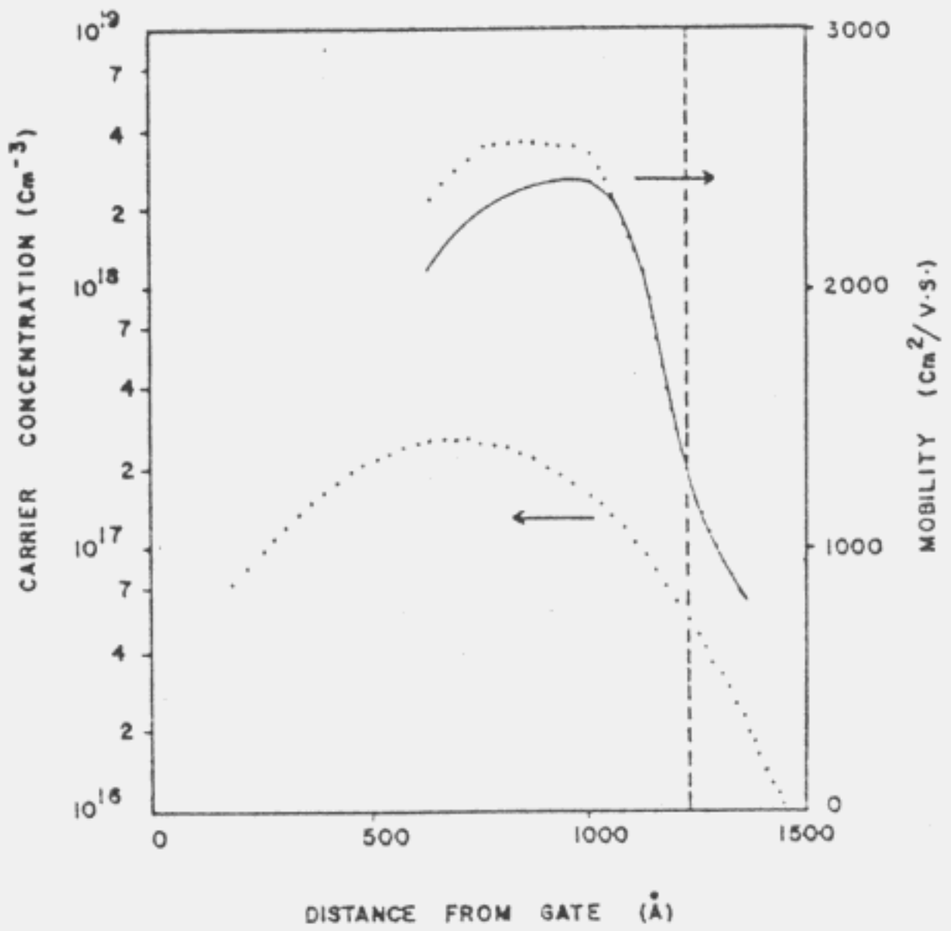

Fig. 1. Mobility and channel electron density versus distance from the gate for ion-implanted 1-μm gate length MESFET. The dotted line is the zero approximation mobility profile and the solid line is the final mobility profile. In the region to the right of the vertical dashed line our technique does not apply because the Debye length becomes comparable with the characteristic length of the carrier profile variation.

The threshold voltage V_T is adjusted slightly to yield a linear plot.

The next step involves the calculation of the approximate mobility profile as described above. After that, we plot the channel resistance versus $1/\sigma$ where, $\sigma = L/(WR_{ch})$. The intercept of this dependence yields $R_s + R_d$ and the slope L/W

$$R_T = R_s + R_d + \frac{L}{\sigma W}. \tag{9}$$

Finally, we solve (4) and (7) again to determine the mobility profile using the new value of $R_s + R_d$ and check for the convergence. Typically one iteration is all that is required for the accurate determination of the mobility profile.

GaAs MESFET's were fabricated using multiple selective ion implantation into undoped LEC semi-insulating GaAs. Selenium ions were implanted in the active channel and sulfur implantation was used for the n^+ regions under the ohmic contacts. Ohmic contacts were made using AuGe/Ni metals and the Schottky barrier/first level metal was TiW/Au patterned using a dielectric assisted liftoff technique. The interlevel dielectric was plasma enhanced CVD silicon oxy-nitride, and the second level metal was TiW/Au patterned using ion-beam milling. The threshold voltage was close to −1 V. Doping profiles of the ion-implanted semiconductor can be fairly well approximated by Gaussian distribution [11]. The gate voltage V_g versus X given by (4) calculated for the doping profile shown in Fig. 1 is depicted in Fig. 2. This curve has been tabulated and used for the numerical solution of (7). The measured transconductance g_m versus V_g for $V_{ds} = 20$ mV and $V_{ds} = 40$ mV is shown in Fig. 3(a). As can be shown from (7) the value of $(1/\mathrm{gm})\cdot(\partial\ \mathrm{gm}/\partial V_g)$ is independent for V_{ds} for low values of V_{ds}. Indeed, the difference in this product measured at 20 and 40 mV was less than 3 percent.

The channel current I_d measured at low V_{ds} is shown in Fig. 3(b) as a function of the gate bias. From this measurement the total resistance was obtained as $R_T = V_{ds}/I_d$. The source and drain resistance R_s and R_d are determined as suggested in [10] or [12]. Plotting R_T as a function of $(1-\sqrt{\eta}\,)^{-1}$ (see

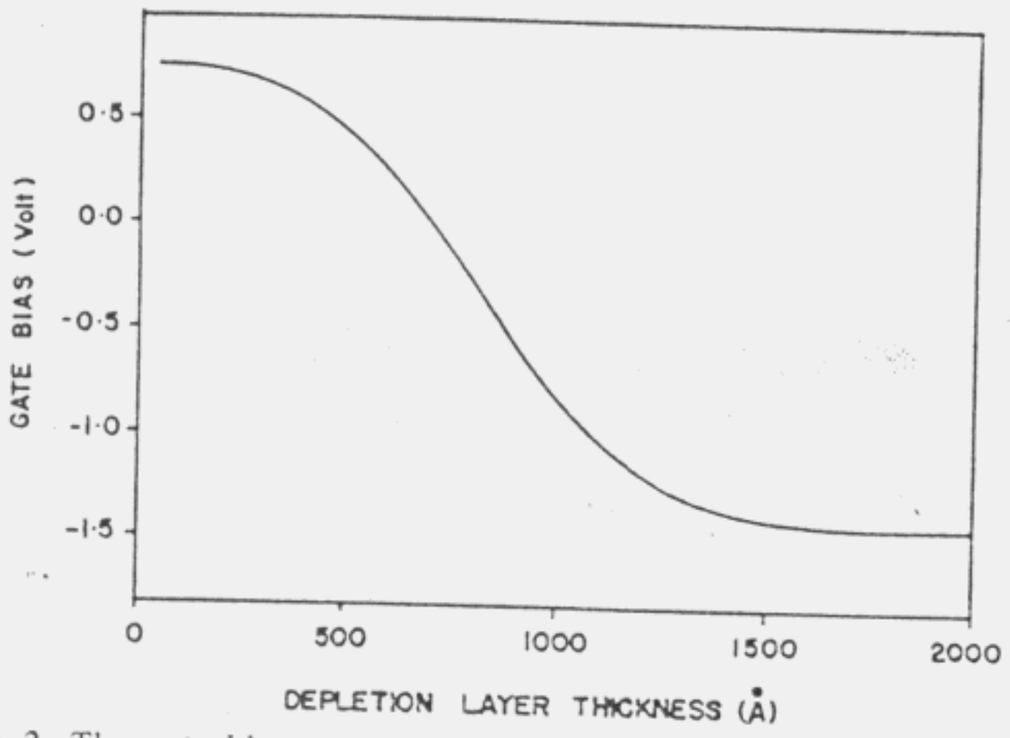

Fig. 2. The gate bias versus the depletion layer thickness (calculated from (4)).

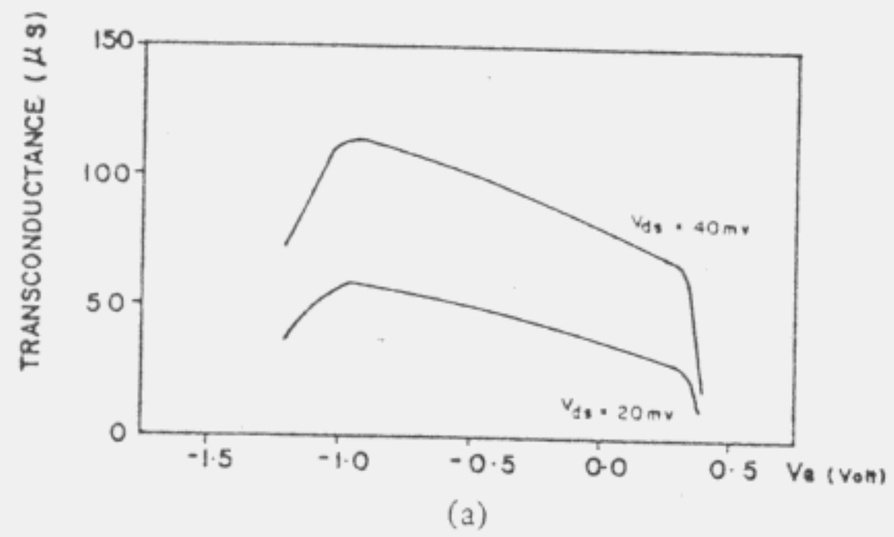

Fig. 3. The transconductance (a) and the channel current (b) as functions of gate bias for low V_{ds} for 20-μm wide devices.

(8)) and slightly adjusting V_T we obtain a linear plot for the data points. This yields both the value of $R_s + R_d$ as the intercept and a more accurate value for V_T than the value obtained from the measurements of the FET characteristics at large V_{ds} ($V_T = -0.995$ V).

Then we solve (7) together with (4). The resulting mobility profile is shown in Fig. 1 as a dotted line. Plotting R_T versus $1/\sigma$ (see (9)) yields a more accurate value of $R_s + R_d = 110\ \Omega$ (as compared with an approximate value of 120 Ω) (see Fig. 4) and the value of $L/W = 0.066$ (the slope) in good agreement with the directly measured value $L/W = 0.065$ (this value was determined optically).

Finally the mobility profile is recalculated again using the accurate value of $R_s + R_d$. The final profile is also shown in Fig. 1 as solid line. As can be seen from the figure the first iteration is not too far off from the zeroth approximation mobility curve. Our results indicate that the mobility may be quite low especially far from the gate. It is considerably

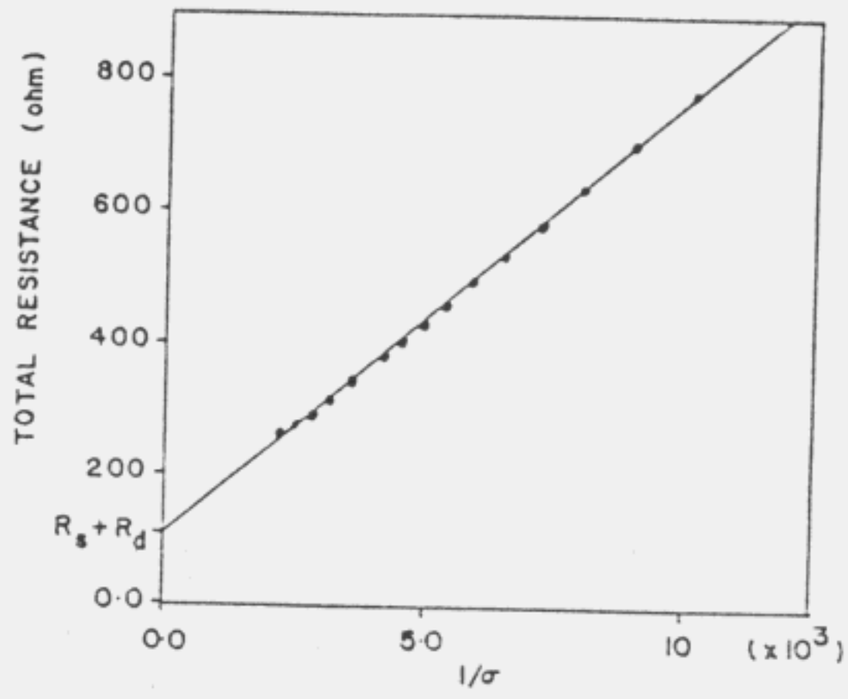

Fig. 4. Determination of R_s and R_d. The total resistance is plotted as a function of $1/\sigma$ where $\sigma = \int_x^\infty \mu(X')N(X')dX'$. This yields $R_s + R_d$ (110 Ω) as the intercept and L/W (0.066) as the slope.

smaller than the measured Hall mobility for the same wafers which is of the order of 3000–4000 $cm^2/V \cdot s$. A similar apparent decrease of the low field mobility in short devices has been noticed by Fukui [10]. The reasons for this decrease may be related to the device processing and are not clear at the present time. The nonuniform mobility profile has to be taken into account in modeling and characterization of ion-implanted GaAs devices, especially low pinchoff voltage devices where the low field mobility plays an important role in determining the device transconductance [1].

We should point out that the theory used in this brief may become inaccurate when the electron concentration drops below $5 \cdot 10^{16}\ cm^{-3}$ or so (i.e., at the distance farther from the gate than approximately 1200 Å) because in this region the Debye radius (190 Å at 300 K) becomes comparable with the characteristic length of the carrier profile variation. A more elaborate analysis should be used in this region, as suggested in [13].

Acknowledgment

The authors would like to thank R. Jiracek of SRC, Honeywell, for his help in the wafer testing.

References

[1] M. S. Shur, "Low-field mobility, effective saturation velocity, and performance of submicron GaAs MESFET's," *Electron. Lett.*, vol. 18, no. 21, pp. 909-910, Oct. 1982.
[2] J. S. Sites and H. H. Wieder, "Magnetoresistance mobility profiling of MESFET channels," *IEEE Trans. Electron Devices*, vol. ED-27, no. 12, pp. 2277-2281, Dec. 1980.
[3] A. A. Immorlica, Jr., D. R. Decker, and W. A. Hill, "A diagnostic pattern for GaAs FET material development and process monitoring," *IEEE Trans. Electron Devices*, vol. ED-27, no. 12, pp. 2285-2291, Dec. 1980.
[4] L. J. Van der Pauw, "A method of measuring specific resistivity and Hall effect of disc of arbitrary shape," *Philips Res. Rep.*, vol. 13, pp. 1-9, 1958.
[5] T. L. Tansley, "AC profiling by Schottky-gate cloverleaf," *J. Phys. E: Sci. Instr.*, vol. 8, pp. 52-54, Jan. 1975.
[6] L. J. Van der Pauw, "A method of measuring the resistivity and Hall coefficient on lamellae of arbitrary shape," *Phil. Tech. Rev.*, vol. 20, pp. 220-224, 1958/59.
[7] K. Lehovec, "Determination of impurity and mobility distribution in epitaxial semiconducting films on insulating substrate by C-V and Q-V analysis," *Appl. Phys. Lett.*, vol. 25, pp. 279-281, Sept. 1974.
[8] R. A. Pucel and C. F. Krumm, "Simple method of measuring drift mobility profiles in thin semiconductor films," *Electron. Lett.*, vol. 12, pp. 240-244, May 1976.

[9] J. D. Wiley and G. L. Miller, "Series resistance effects in semiconductor *C-V* profiling," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 265-273, May 1975.
[10] H. Fukui, "Determination of the basic device parameters of a GaAs MESFET," *Bell Syst. Tech. J.*, pp. 771-797, Mar. 1979.
[11] J. F. Gibbons, W. S. Johnson, and S. W. Myrlie, "Projected range statistics," in *Semiconductors and Related Material*, 2nd ed. Stroudsburg, PA: Dowen, Hutchinson, and Ross, 1975.
[12] P. L. Hower and N. G. Bechtel, "Current saturation and small-signal characteristics of GaAs FET's," *IEEE Trans. Electron Devices*, vol. ED-20, no. 3, Mar. 1973.
[13] H. Kroemer and W. Chien, "On the theory of Debye averaging in the C-V profiling of semiconductors," *Solid-State Electron.*, vol. 24, pp. 655-660, 1981.

Contributors

Dimitri A. Antoniadis (M'79) was born in Athens, Greece, in 1947. He received the B.S. degree in physics from the National University of Athens in 1970, and the Ph.D. degree in electrical engineering in 1976, from Stanford University, California.

From 1970 to 1971 he was a Fellow of the National Research Institute, Athens. From 1976 to 1978 he was a Research Associate and Instructor in the Department of Electrical Engineering at Stanford University. He joined the faculty at MIT in 1978 where he is currently an Associate Professor of Electrical Engineering. He is also Associate Director of the MIT Microsystems Program. From 1969 to 1976, he conducted research in the area of measurements, modeling, and numerical simulation of the earth's ionosphere and thermosphere. He has designed and developed various electronic instruments, currently used for the study of the ionosphere at several locations throughout the world. His present scientific activity lies in the area of silicon device and integrated circuit technology. He has directed the development of SUPREM (Stanford University Process Engineering Models), which has become a world-wide industry-standard engineering tool. His research is currently focused on three areas: Physics of point defects and associated substitutional atom diffusion and crystallographic defect kinetics in silicon; fabrication and modeling of very small geometry MOS devices; and silicon film recrystallization on amorphous substrates with ultimate goal three-dimensional integrated devices.

Dr. Antoniadis is a member of the Electrochemical Society and of the Materials Research Society.

*

Thierry Arnaud was born in Aix-les-Bains, France, on May 11, 1959. He received the diploma in electronical engineering in 1982 and the Diplôme d'Etudes approfondies in 1983 from the Ecole Nationale Supérieure d'Electronique et de Radioélectricité, Grenoble, France.

Since 1982, he has been with the Laboratoire d'Electromagnétisme de l'Institut National Polytechnique de Grenoble, where he has studied propagation in microstrip lines on semi-insulating substrate.

J. Mark Baird (M'69) was born in Murrary, UT on June 4, 1936. He received both the B.S. degree in 1964 and the Ph.D. in 1970 in electrical engineering from the University of Utah, Salt Lake City.

Since graduation, he has engaged in research and development of microwave and millimeter-wave tubes and components at Hughes Research Laboratories, Malibu, CA, and at B-K Dynamics, Inc., Rockville, MD as a Research Director. He is presently conducting research on high-power millimeter-wave gyrotron amplifiers and related devices. He is currently a Research Professor of the Electrical Engineering Department, University of Utah.

*

Henry P. Baltes (M'81) was born in Germany in 1941. He received the M.S. and Ph.D. degrees in physics from the Swiss Federal Institute of Technology (ETH) at Zürich in 1966 and 1971, respectively.

Subsequently he was on the faculty of Freie Universitaet Berlin, University of Duesseldorf, University of Waterloo/Ontario, and Ecole Polytechnique Fédérale (EPF) at Lausanne, Switzerland. He joined Landis and Gyr Zug Corporation, Switzerland, in 1974, where he was first involved in coherent optics, notably inverse scattering, and later became head of the company's solid state laboratory and was mainly involved in integrated sensor research as well as project management. From 1975 to 1982 he taught Optics and Laser Physics as well as Solid-State Physics and Transducers at EPF Lausanne. From 1978 to 1982 he was a member of the Board of Directors of the Swiss Physical Society and chairman of the Science Policy Committee. In 1983, he was appointed to the Henry Marshall Tory Chair at the University of Alberta, Edmonton, Canada, where he joined the Department of Electrical Engineering. He is also a member of the Board of Directors of the Alberta Microelectronic Centre. He is an author and co-author of 3 books and numerous publications on infrared physics, optics, microparticles, and solid-state devices.