CONTINUOUS HETEROSTRUCTURE FIELD EFFECT TRANSISTOR MODEL

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Abstract

We propose a new continuous model for Heterostructure Field Effect Transistors suitable for circuit simulation and device characterization. The model is based on the analytical solution of two-dimensional Poisson's equation in the saturation region. We experimentally determine the HFET saturation current and saturation voltage by differentiating the output characteristics in a unified and unambiguous way. We use these results for a systematic extraction of device and process parameters such as the threshold voltage, effective electron saturation velocity and mobility, drain and source series resistances, effective gate length and characteristic length for channel length modulation. The deduced values agree well with other independent measurements. We report the results of experimental studies of HFETs with nominal gate lengths of 1, 1.4, 2, and 5 micron. A large short-channel effect is observed for the 1 micron gate HFET. The gate length dependences of the device parameters uniquely determined by our method reveal that the effective gate length in our self-aligned structures is approximately 0.25 micron shorter than the nominal gate length. The same model should be also applicable to short channel silicon devices.

I. Introduction

The insight into device physics may be obtained from numerical simulations, such as self-consistent two-dimensional Monte-Carlo modeling [1][2]. However, such an approach is not suitable for applications in device design when the many dependences of device characteristics on design parameters have to be optimized, nor for device characterization when device and process parameters must be extracted from experimental data. Numerical simulation is not applicable to circuit design and simulation either when tens and hundreds of devices have to be simulated interacting with each other and other circuit elements. All these tasks require accurate analytical models. At the same time, these models must be based on physical device and material parameters in order to provide a needed feed-back between the fabrication process and device and circuit design.

An analytical description of Heterostructure Field Effect Transistors (HFETs) is usually based on a charge control model (see, for example, [3]). Such a model can be modified to account for important non-ideal effects, such as carrier injection into a substrate and gate dielectric layer, channel length modulation,etc. This model is based on the electron velocity saturation that happens at drain voltages higher than a certain critical drain voltage called saturation voltage. Even though the charge control model gives a fairly good fit to measured data with a judicial choice of device parameters (see, for example, [4]), parameter extraction for the charge control model remains an unresolved problem. Indeed, in its simplest formulation, this model leads to a discontinuity of drain conductance at drain saturation points and zero output conductance in the saturation region. This can be corrected by getting rid of the gradual channel approximation in the saturation regime. However, it is not a priori clear how to determine the saturation point from measured current-voltage characteristics. Even though several techniques to determine the saturation point have been proposed for silicon MOSFETs [5], these techniques are neither adequate for HFETs nor for submicron Si MOSFETs . In addition, some of the model parameters, such as mobility μ and series resistances R_S and R_d, have a somewhat similar effect on the calculated current-voltage characteristics, leading to non-uniqueness in fitted parameters. This problem becomes especially severe for computer-automated parameter acquisition systems.

In this paper, we describe an improved analytical model of HFETs that allows us not only to obtain excellent agreement with measured data but also to develop a clear and unambiguous procedure for determining the saturation current and saturation voltage. Based on pairs of the saturation current and saturation voltage values, we propose and implement a simple and clear–cut procedure to extract a complete set of device parameters from experimental data.

II. Modeling

Our analytical model is based on several assumptions. First, we neglect the gate current. Second, we assume the validity of the Gradual Channel Approximation (GCA) with constant gate to channel capacitance in the portion of channel where electron velocity is smaller than saturation the electron velocity, v_{sat} [3]. Third, we assume that once the velocity saturation occurs near drain edge of the channel, channel length modulation is responsible for further increase in the drain current. Fourth, we use the relation between the electric field and the electron velocity given by a following approximation [6]: $v = \mu F_x /[1+(F_x/2F_s)]$ for $F_x \le 2F_s$ and $v = v_{sat}$ for $F_x \ge 2F_s$ where v is the electron velocity, $F_s = v_{sat}/\mu$, $F_x = dV(x)/dx$, and V(x) is the channel potential.

Voltages with upper case subscripts (for example,V_{GS}, V_{DS}) denote intrinsic variables, while those with lower case subscripts (V_{gs},V_{ds}) denote extrinsic variables. Note, however, that the drain current (I_{DS})is the same for both cases.

From the conventional charge control model [7] ($qn_{ch}= C_i[V_{GT} - V(x)]$ where all the parameters have the same notation as in [5][6][8], we obtain the expression for the current-voltage characteristics of the HFET in a linear region :

$$I_{DSL} = \frac{1}{R_n}\frac{2V_{GT}V_{DS}-V_{DS}^2}{V_{DS}+2V_L} \qquad (1)$$

where $R_n = 1/WC_iv_{sat}$, $V_L=F_s L$, and L is the effective gate length.

At saturation ($V_{DS}=V_{DSAT}$), the electron drift velocity at the drain edge of the channel is saturated at v_{sat}. Then, the drain current is defined by $I_{DSAT} =q\, n_{ch}\, v_{sat}W = C_i\,(V_{GT} - V_{DSAT})v_{sat}W$. Also, eq. (1) holds at $V_{DS}=V_{DSAT}$. By equating these two equations, we obtain the following expressions for saturation voltage and current given by

$$I_{DSAT} = \frac{1}{R_n}\frac{V_{GT}^2}{V_{GT}+2V_L} \qquad (2a)$$

$$V_{DSAT} = \frac{2V_{GT}V_L}{V_{GT}+2V_L} \qquad (2b)$$

When V_{DS} becomes larger than V_{DSAT}, the point where $F=2F_s$ marked as $x=L-\Delta L$ in Fig. 1 moves closer to source. This effect is called "channel length modulation". In region I, the drain-to-source current in the saturation region, I_{DSS}, can be found from eq. (2a) by replacing V_L with $V_L - V_{\Delta L}= F_s(L-\Delta L)$:

$$I_{DSS} = \frac{1}{R_n}\frac{V_{GT}^2}{V_{GT}+2(V_L - V_{\Delta L})} \qquad (3a)$$

In good devices, suitable for circuit application, short channel effects must be relatively small so that $\Delta L \ll L$ and $V_{\Delta L} \ll V_{GT}/2 + V_L$. Hence, we can expand eq. (3a) to obtain

$$I_{DSS} \approx \frac{1}{R_n}\frac{V_{GT}^2}{V_{GT}+2V_L}\left[1+\frac{2V_{\Delta L}}{V_{GT}+2V_L}\right] \quad (3b)$$

Equation (3b) clearly show the increase of the drain current in the saturation region due to channel length modulation for an intrinsic HFET. To find ΔL, we solve 2-D Poisson's equation analytically in the region II [9]. The solution of the channel potential is expected to have the exponential dependence on distance toward drain [10]:

$$V_{DS} = V_{DSAT} + \alpha V_\lambda [\exp(\Delta L/\lambda) - 1] \quad (4)$$

where $\lambda=\sqrt{t(d+\Delta d)}$ and $V_\lambda=F_s\lambda$. The constant α can be found from the requirement of continuity of the drain conductance variation with the drain voltage at $V_{DS}=V_{DSAT}$: $\alpha=8(V_{GT}+V_L)V_L/(V_{GT}+2V_L)^2$. Equations (2a), (3a), and (4) give the following expression for the drain current in the saturation region:

$$I_{DSS} = I_{DSAT}\left[\left(1+\frac{2V_\lambda}{V_{GT}+2V_L}\right) \times \ln\left\{1+\frac{(V_{DS}-V_{DSAT})(V_{GT}+2V_L)^2}{8V_\lambda(V_{GT}+V_L)V_L}\right\}\right] \quad (5)$$

In short channel compound semiconductor devices with gate lengths of one micron or less, the extrinsic source and drain resistances are comparable to the channel resistance. Therefore, the voltage drop across these parasitic resistances can no longer be treated as a small perturbation to the external bias, (the assumption which has been used successfully for parameter extraction in silicon [11]). Moreover, for compound semiconductor devices, accurate determination of R_D and R_S using the gated transmission line method is usually not as successful as for Si MOSFETs due to the less uniform compound semiconductor device characteristics. At the same time, useful device modeling and parameter extraction method should be able to cover both the intrinsic characteristics and the extrinsic device characteristics. We can easily derive the extrinsic model by using the following relationship $V_{GS} = V_{gs} - I_{DS}R_S$ and $V_{DS} = V_{ds} - I_{DS}(R_S + R_D)$.

Substituting these equations into eq. (1), we obtain a quadratic equation in I_{DSL}. The solution of this equation is given by

$$I_{DSL}=(2V_{gt}V_{ds} - V_{ds}^2)/[A + \sqrt{A^2 - B}] \quad (6)$$

where $A= (R_n/2-R_D)V_{ds}+(R_S+R_D)V_{gt}+R_nV_L$ and $B= (R_S+R_D)(R_S - R_D+R_n)(2V_{gt}V_{ds}-V_{ds}^2)$.

Similarly, saturation current, I_{DSAT} can be found from the quadratic equation obtained such that

$$I_{DSAT} = V_{gt}^2/[DR_n+V_{gt}R_S+\sqrt{E}] \quad (7)$$

where $D=V_{gt}/2+V_L$ and $E=D^2R_n^2+2V_{gt}R_nR_SV_L$.

Once I_{DSAT} is found as a function of V_{gt}, we can calculate both the intrinsic gate voltage V_{GT} and the intrinsic saturation voltage V_{DSAT} easily. Then we find $V_{dsat}=V_{DSAT} + I_{DSAT}(R_S + R_D)$.

However, a reasonably well behaved HFET characteristics suitable for circuit application should be designed in such a way that λ is much smaller than L in order to reduce the short channel effects. If this is the case, we can assume that although V_{DS} increases above V_{DSAT}, V_{GT} remain nearly the same as that at the saturation point and $V_{ds} - V_{dsat} \approx V_{DS} - V_{DSAT}$.

$$I_{DSS}=I_{DSAT}\left\{1+\frac{2V_\lambda}{V_{gt}+2V_L-I_{DSAT}R_S}\ln[1+K]\right\} \quad (8)$$

where

$$K=\frac{(V_{ds}-V_{dsat})(V_{gt}+2V_L-I_{DSAT}R_S)^2}{8V_LV_\lambda(V_{gt}+V_L-I_{DSAT}R_S)}$$

In deep saturation, the second term in the logarithmic argument in eq. (8) is much larger than 1. Hence, the extrinsic drain resistance at the saturation region can be found as follows:

$$r_{dss} = 1/\left(\frac{\partial I_{DSS}}{\partial V_{ds}}\right) = \left(\frac{V_{gt}+2V_L}{I_{DSAT}} - R_S\right)\frac{V_{ds}-V_{dsat}}{2V_\lambda} \quad (9)$$

Eq. (9) is a very important result since it shows that we can determine V_{dsat} from the V_{ds}-intercept in r_{dss} versus V_{ds} plot as illustrated in Fig. 2. Moreover, we can find V_λ from the slope of this dependence once V_L and R_S are known. V_λ is an extremely important parameter which is a measure of the short channel effect and the channel length modulation.

III. Parameter Extraction and Discussion

In this section, we show how to extract device parameters suitable for circuit simulation from experimental data for conventional self-aligned AlGaAs/GaAs HFET devices with d= 400Å and W=10 μm. The nominal gate lengths are 1, 1.4, 2, and 5 μm. The extracted values of R_S, R_D, R_n, V_L, and V_λ are also listed in Table I.

Fig. 2 shows experimental determination of the saturation points for different external gate voltages. This determination is based on eq. (9). At $V_{ds} > V_{dsat}$, r_{dss} versus V_{ds} curves show well behaving linear characteristics, in agreement with eq. (9). At $V_{ds} >> V_{dsat}$, r_{dss} becomes small again because of other short channel effects, such as substrate conduction [12], and/or drain induced barrier lowering (DIBL) [13]. We can determine V_{dsat} from the V_{ds}-intercept in r_{dss} versus V_{ds} plot (In Fig. 2, a mark "S" is the saturation point for V_{gs}=0.4V.) Our determination of saturation point based on eq. (9) is much more accurate and straightforward than that reported previously for Si MOSFET which is based on the second derivative of the output characteristics [5]. Indeed, in the saturation region, the drain current is nearly constant. Hence, it is much easier to determine the saturation point using the method based on the first derivative and not on the second derivative which is very difficult to evaluate accurately.

Once the electron velocity reaches the saturation velocity v_{sat}, the drain current is described by $I_{DSAT} = (V_{GT} - V_{DSAT})/R_n$. If we account for the parasitic source and drain resistances, we obtain

$$I_{DSAT}(R_n-R_D)=V_{gs} - V_t - V_{dsat}. \quad (10)$$

According to eq. (10), the I_{DSAT} versus $(V_{gs}-V_{dsat})$ plot is a straight line. The reciprocal of the slope of this straight line corresponds to the $R_1 = R_n - R_D$ and the x-intercept yields the threshold voltage, V_t. Fig. 3 shows I_{DSAT} versus $(V_{gs}-V_{dsat})$ plot for three of our devices. The least square fit of our eq. (10) to the experimentally measured data yields the values of V_t and R_1.

The very definition of the threshold voltage in the short channel HFET is not unique. For example, the measurement of V_t from the V_{gs}-intercept in the $I_{ds}-V_{gs}$ curve at low drain bias is widely used in Si MOSFETs. However, this approach is not accurate enough for HFETs because of large series resistances R_S and R_D that are comparable to the channel resistance [14].

The difference $R_D - R_S$ can be determined either from the gate current measurement or from the measured values of the transconductances, interchanging the source and drain. We should notice that the exact determination of $R_D - R_S$ is not overly important because $R_D \approx R_S$ for a nearly symmetrical device. From the forward and reverse transconductance at saturation region, $R_0 = R_D - R_S = 1/g_{mr} - 1/g_{mf}$. We find $R_D - R_S = -20\ \Omega$ for all our devices. We obtain exactly the same values from the gate current measurements. We can rewrite eq. (2a) as follows

$$\frac{(V_{gt}-I_{DSAT}R_S)^2}{I_{DSAT}} = R_n(V_{gt}-I_{DSAT}R_S+2V_L) \quad (11)$$

Equation (11) implies that we can find R_n and $2V_L$ from the linear regression of $(V_{gt}-I_{DSAT}R_S)^2/I_{DSAT}$ versus $V_{gt}-I_{DSAT}R_S$ data. The values of V_λ extracted from the measured average slope of r_{dss} vs. $V_{ds}-V_{dsat}$ for different gate voltages (see eq. (9)).

The value of v_{sat} can be found from the extracted values of R_n using $R_n = 1/WC_iv_{sat}$. We obtained $v_{sat} = 1.28 \pm 0.05 \times 10^5$ m/sec (the average value for three different devices). This value agrees well with that of 1.1×10^5 m/sec estimated from f_T measurement [15]. This confirms that our device model and parameter extraction procedure are quite accurate. The low field mobility μ and electrical gate length can be found from

$$V_L = v_{sat} L/\mu = v_{sat} (L_M - \delta L)/\mu . \quad (12)$$

Here, L_M is the nominal gate length. If v_{sat} and μ are independent of gate length, we expect linear relationship between V_L and L_M (see Fig. 4). From the linear regression, we obtain $\delta L = 0.25$ μm and μ=10,000 cm²/V-sec. This value of μ is in good agreement with the Hall measurements [16]. The gate length offset, δL, can be introduced during many stages in the fabrication process. The main contribution for our devices comes from the implant straggle during the n^+ source and drain implantation. The obtained value of δL is in agreement with the value obtained from the output conductance measurements [17].

The threshold voltage, V_t is the one of the most important parameters both for the device characterization and circuit operation. However, the very definition of V_t is not unique. As can be seen from Table I, the threshold voltages (determined from eq. (10) and Fig. 3) are close for 1.4 and 2 μm devices. But, there is a considerable shift in V_t for 1 μm device due to the short channel effect. In Table II, we compare the values of V_t found using the following four methods:

Method 1: From the x-intercept in I_{DS} vs. V_{gs} plot at low V_{ds} (we use V_{ds}= 10 mV) as widely done for Si MOSFETs.

Method 2 : Same as Method 1 but for intrinsic device after correcting for the voltage drop across R_S and R_D.

Method 3 : As determined from eq. (10) and Fig. 3.

Method 4 : From the unified change control model reported in Ref. [8]: $I_{DS}(V_{GS}=V_t) = q\mu(\eta V_T + an_o/2)n_o W/L$ where $n_o = 5 \times 10^{10}/\text{cm}^2$.

The value of V_t obtained by Method 3 agrees well with that obtained using Method 4, which is based on material and process parameters. (For Method 4, we measure V_t at $V_{ds} = 0.1$V, which is large enough to satisfy the condition $V_{ds} >> \eta V_T$, but small enough not to cause the short channel effect.) Therefore, we recommend to use Method 4 for measurement of V_t, instead of Method 1 or 2. This method is much easier to use than Method 3.

The values of λ calculated from the values of V_λ in Table I are 1,650Å, 1,550Å and 2,650Å for devices with gate lengths L = 2.0, 1.4, and 1.0 μm, respectively. (The values of $v_{sat} = 1.28 \times 10^7$ cm/sec and μ = 10,000 cm²/V-sec were used in this calculation.) The values of λ for 1.4 μm and 2.0 μm gate devices agree well with each other, implying that the channel length modulation is responsible for the current increase in the saturation region for both devices. However,the value of λ for the 1.0 μm gate device is much larger. This indicates that other short channel effects are present, such as the substrate conduction [12] and/or drain induced barrier lowering [13]. All deduced values of λ are much larger than those estimated from eq. (9). This is the consequence of a relatively low substrate acceptor doping and deep source/drain junction depth [10].

The experimentally measured and calculated I_{DS}-V_{ds} characteristics for 1.4 μm is compared in Fig. 4. The calculation has been done using the extracted parameters given in Table I with no adjustable parameters. As can be seen from the figure, the agreement between the calculated and measured curves is excellent. From the subthreshold slope of S=70 mV/decade in our unintentionally doped substrate devices [8], we estimate the background acceptor concentration in the substrate to be on the order of 10^{16} cm^{-3}.

Table I
Device parameters extracted from I_{DS}-V_{ds} characteristics of HFETs having three different channel lengths.

W/L_M[μm]	10/2.0	10/1.4	10/1.2
V_t[V]	0.148	0.121	0.214
V_L[V]	0.204	0.155	0.086
R_S [Ω]	190	162	175
R_D [Ω]	170	142	155
V_λ[V]	0.021	0.020	0.034

IV. Conclusion

Our model allows us to describe the current-voltage characteristic in an analytical form for the entire range of drain and gate voltages in the strong inversion regime. Hence, our model is very well suited for manual and automated parameter extraction. Our parameter extraction technique is based on the experimental determination of the HFET saturation current and saturation voltage by differentiating the output characteristics. This technique allows us to obtain a systematic extraction of such device and process parameters as the threshold voltage, effective electron saturation velocity and mobility, drain and source series resistances, effective gate length, and characteristic length for channel length modulation in a unified and unambiguous way. The device parameters extracted using our technique from the experimental data agree well with the results of independent measurements. This proves the accuracy and versatility of our device model and parameter extraction procedure. This technique (in a slightly modified form) should be also applicable for deep submicron Si MOSFETs.

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Table II
Threshold voltages (V_t) found by four different methods.

W/L_M	10/1.0	10/1.4	10/2.0	10/5.0
Method 1	0.136	0.089	0.097	0.091
Method 2	0.210	0.195	0.202	0.124
Method 3	0.214	0.121	0.148	-
Method 4	0.206	0.129	0.153	0.123

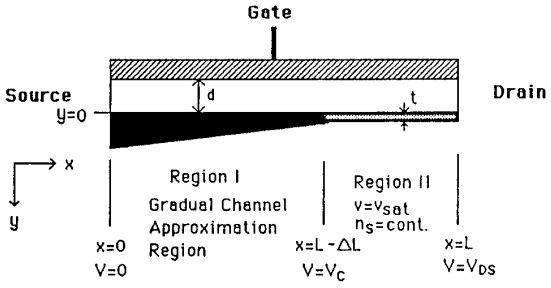

Fig. 1. Schematic representation of conducting channel

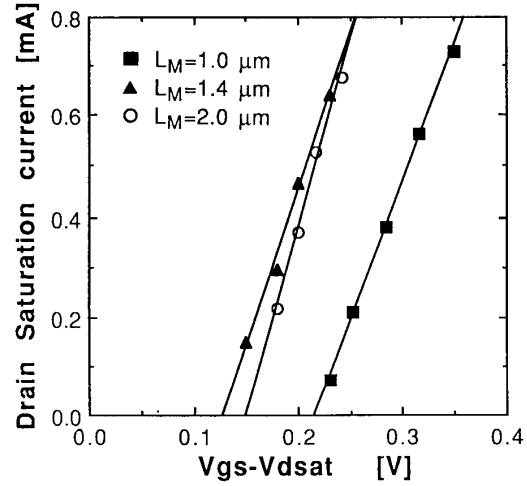

Fig. 3. Extraction of $R_n - R_D$ using eq. (10).

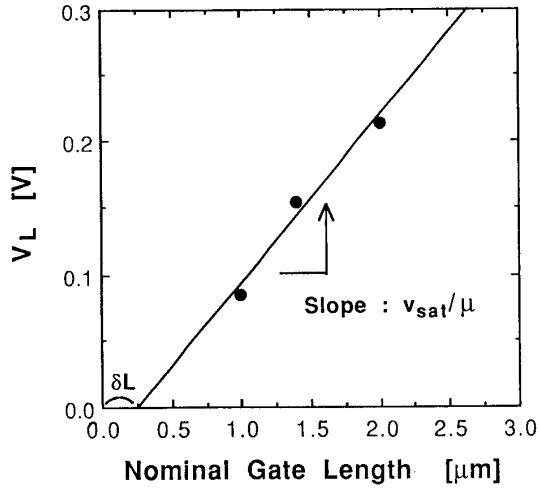

Fig. 4. Determination of mobility and δL according to eq. (12).

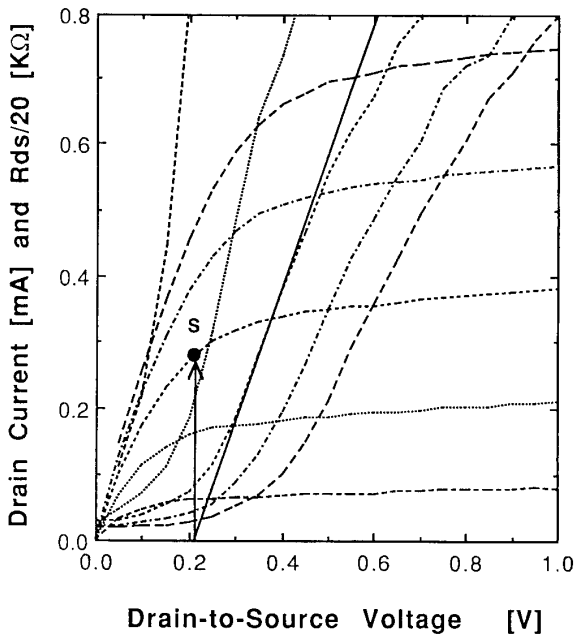

Fig. 2 Experimental determination of saturation voltage and saturation current for 1.4 μm gate device. For the top curve, V_{gs} = 0.6 V: step = –0.1 V. The point marked "S" is the saturation point for V_{gs} = 0.4 V.

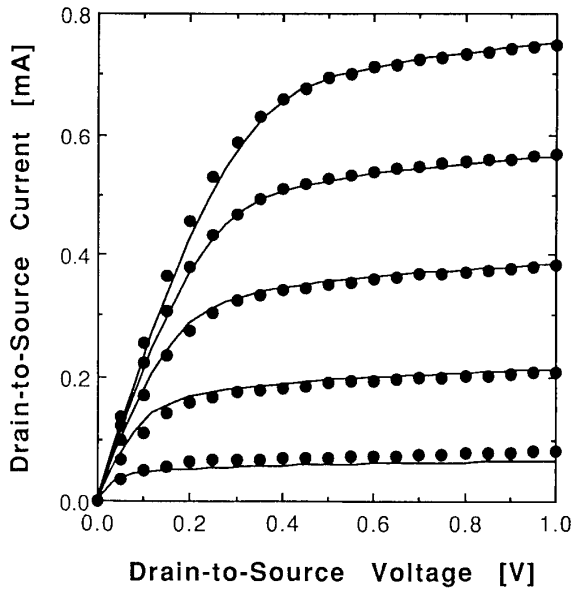

Fig. 5. Measured (solid dots) and calculated (solid lines) current-voltage characteristics of HFETs with gate lengths of 1.4 μm. The top curve in each figure corresponds to V_{gs}=0.6 V and step = – 0.1 V. The parameters used in the calculations are all extracted (see Table I).