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Self-Aligned Shallow Junction p^+-gate GaAs JFET for Higher Turn-on and Breakdown Voltages

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Abstract

New self-aligned GaAs Junction Field Effect Transistor (JFET) fabrication technology using elemental shallow Zn diffusion from patterned Au/Zn gate metal is reported in this paper. Compared to the conventional Al-gate MESFET, our nonoptimized long channel device shows about 0.3V higher gate turn-on voltage in the forward bias and much larger reverse breakdown voltage (-20V vs. -8V) with comparable transconductance. This device can have potential applications in DCFL logic circuit and microwave power applications.

I. Introduction

It is well known that conventional MESFET technology suffers from gate leakage problems due to the low turn-on voltage of the Schottky barrier (typically 0.7V) to be useful for low power and high speed DCFL (Direct Coupled FET Logic) circuit application. Therefore, there have been many attempts to increase the gate turn-on voltage using p^+ gate instead of Schottky barrier[1-4]. JFET has the merits of larger built-in voltage of p-n junction and gives larger noise margin and logic swing. However, compared to MESFET, either it has much lower performance due to the large parasitic capacitances or the fabrication technologies reported to date are too complex to be manufacturable at present time.

Zn diffusion in GaAs and other III-V semiconductors for p-type layer has long been very popularly used in open- or closed-type methods[5-7]. Sources of Zn have included the gallium-zinc alloys, combination of zinc-arsenic compounds, tungsten film embedding zinc and doped oxide source as solid type, and DEZ(Diethyl-Zinc) and TEAs(Triethyl-Arsine) as gas flow[8-10]. For the p^+-gate JFET, shallow Zn diffusion and small lateral diffusion are indispensable to obtain high performance[2]. But this requires critical alignment step of gate metal pattering over Zn diffused area to obtain short channel length and small parasitic capacitances.

In this paper, a new simple method to fabricate JFET using elemental shallow Zn diffusion from patterned Zn/Au gate metal is reported. Fig.1 shows the schematic cross section of the fabricated device. As can be seen in Fig.1, our process is the same as that of the conventional MESFET except shallow p^{++}-n junction formation under the Au gate. Because Zn is diffused from gate metal, p^{++}-n junction is self-aligned to the gate metal.

II. Device Fabrication

Si doped n-GaAs active layer and n^+-layer for ohmic contacts were grown by MOCVD. Thickness and doping concentration are 0.2μm and $3\times10^{17}cm^{-3}$ for n-layer and 0.1 μm and higher than 1×10^{18} cm^{-3} for n^+ layer, respectively. Ohmic contacts were formed with Au/Ni/AuGe for the source and drain by lift-off process . After gate pattern was defined by photolithography, channel region is recessed using $NH_4OH:H_2O_2:H_2O$ etchant (1:1:200) with an etch rate of 0.1μm/min. Gate

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metal composed of 0.1μm/0.2μm thick Au/Zn was evaporated. Si_3N_4 of 0.3μm thickness, is then sputtered. Si_3N_4 dielectric film not only passivates the surface as well as protects against Zn out-diffusion to the ambient and against lateral Zn diffusion along GaAs surface. Rapid thermal diffusion was carried out for a few seconds in an open-tube system with nitrogen ambient at 400°C. In addition to the recess etching, diffusion time was controlled to adjust the threshold voltage while temperature was kept constant at 400°C. Si_3N_4 was patterned by photolithography and etched in BOE(buffered oxide etchant) . Au in the gate metal not only reduces the gate resistance but also protects Zn from BOE attack.

The junction depth, which is estimated very crudely by comparing average I_{dss} values of fabricated devices, is shown in Fig.2 as a function of the square root of the diffusion time at 400°C. The electrical characteristics of our fabricated GaAs JFET with a junction depth of less than 50 nm are reported here.

III. Device Characteristics

The fabricated JFET and MESFET have 4 μm gate length and 220 μm width. Both conventional Schottky gate MESFET and proposed JFET are fabricated using a same process sequence except gate metal formation. Figure 3 compares forward gate current vs. voltage characteristics between conventional Al Schottky barrier (left curve) and p^{++} junction gate (right curve). We can see from this figure that the proposed device has about 0.3V higher forward turn-on voltage. Moreover, Fig.4 shows that reverse breakdown voltage of our proposed JFET is about -20V which is much larger than that of conventional Schottky gate (about -8V). From this figure, we can see that lateral diffusion of Zn along GaAs surface is very small. If there were appreciable lateral diffusion, p^{++}-n^+ junction would be formed between gate metal and n+ source and drain region(see Fig.1). If this is the case, reverse breakdown voltage would be very low. Ideality factor of our JFET is around 1.75. The drain I-V curves are shown in Fig.5. The transconductance, G_m, was measured to be about 90 mS/mm at V_{ds}= 4V and V_{gs} = -0.1V, which is quite high for the long gate length, while conventional MESFET has typical transconductance of around 70 mS/mm. This implies that Zn diffusion does not degraded device performance at least for the long channel device.

Although in this paper we report only the result for the relatively long channel JFET due to the lithography limit of our facility, similar improvement for the short channel JFET is expected. This is because from the measured data, we can estimate that the Zn diffusion has very shallow junction depth as well as very small lateral diffusion, both of which are very crucial for high performance short channel FETs.

IV. Conclusion

New self-aligned GaAs Junction Field Effect Transistor (JFET) fabrication technology using elemental shallow Zn diffusion from patterned Au/Zn gate metal is reported in this paper. Compared to the conventional Al-gate MESFET, our nonoptimized long channel device shows about 0.3V higher gate turn-on voltage in the forward bias and much larger reverse breakdown voltage (-20V vs. -8V) with comparable transconductance. Due to the very shallow junction depth and small lateral diffusion, we expect similar improvement can be obtained for the submicron FETs.

Acknowledgement

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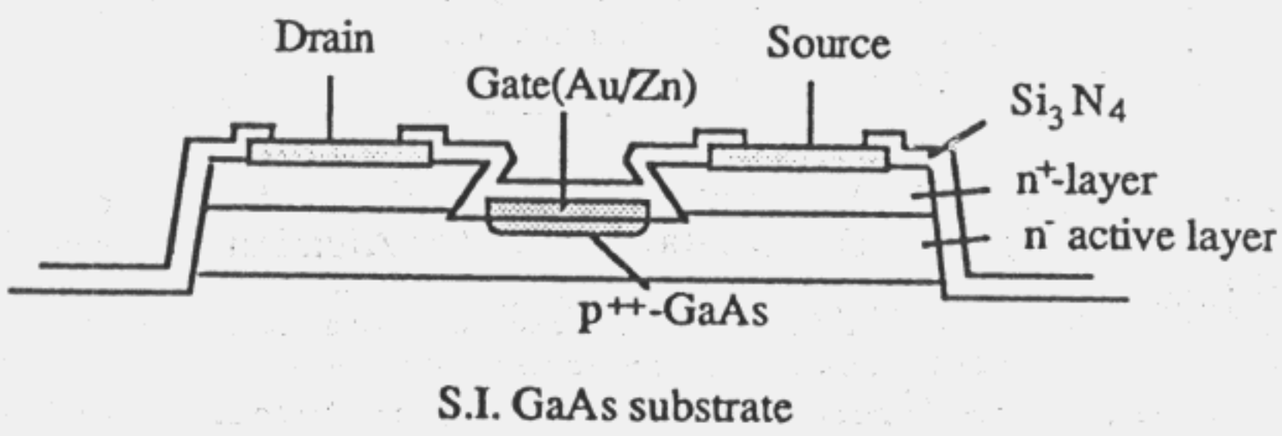

Figure 1. Schematic cross diagram of fabricated JFET

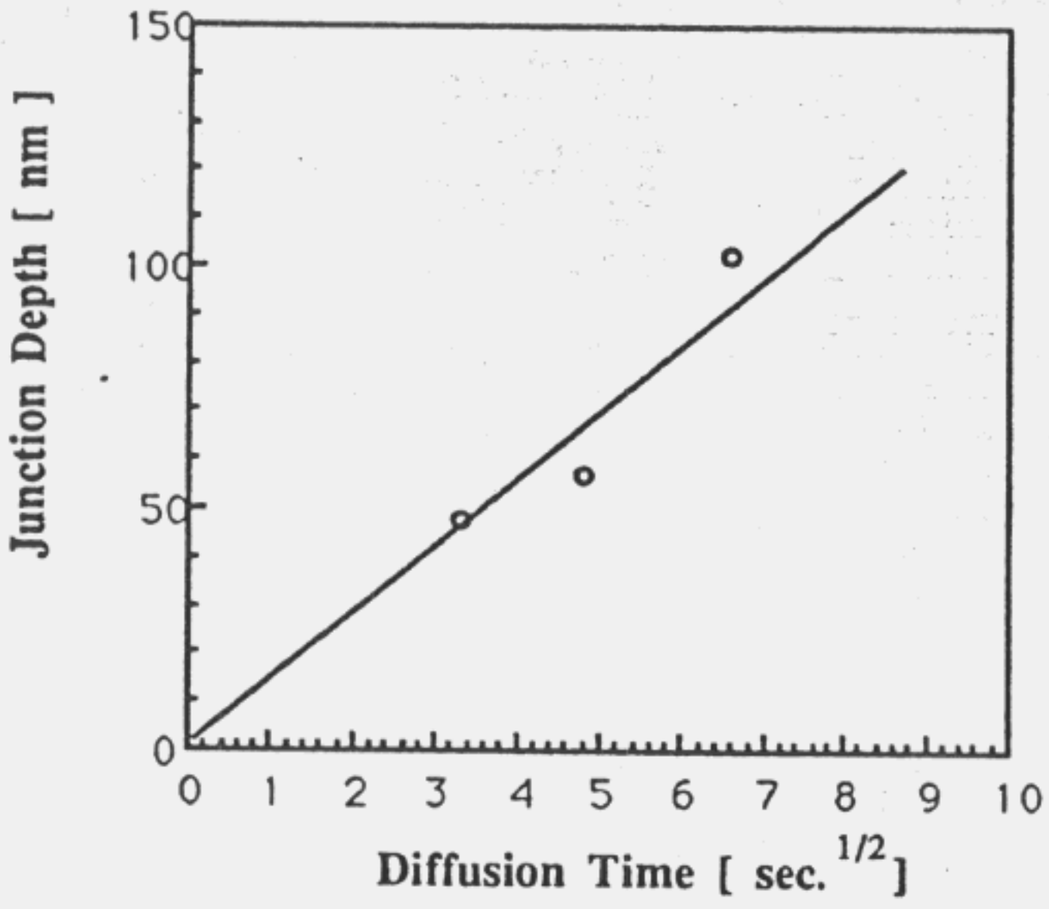

Figure 2. Junction depth as a function of the square root of the diffusion time.

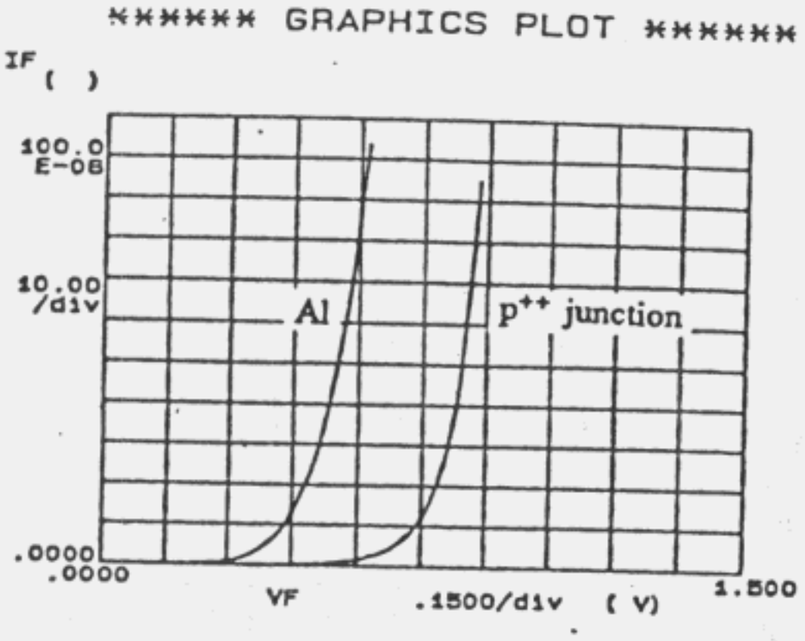

Figure 3. Comparison of forward I - V characteristics for Aluminum gate (left curve) and p^{++} junction gate (right curve).

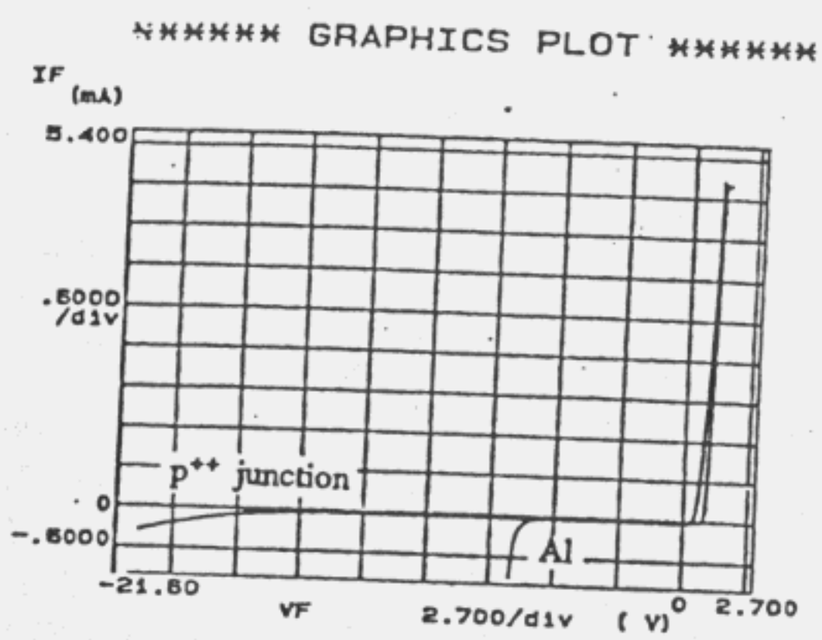

Figure 4. Comparison of reverse I-V characteristics for Aluminum gate and p^{++} junction gate.

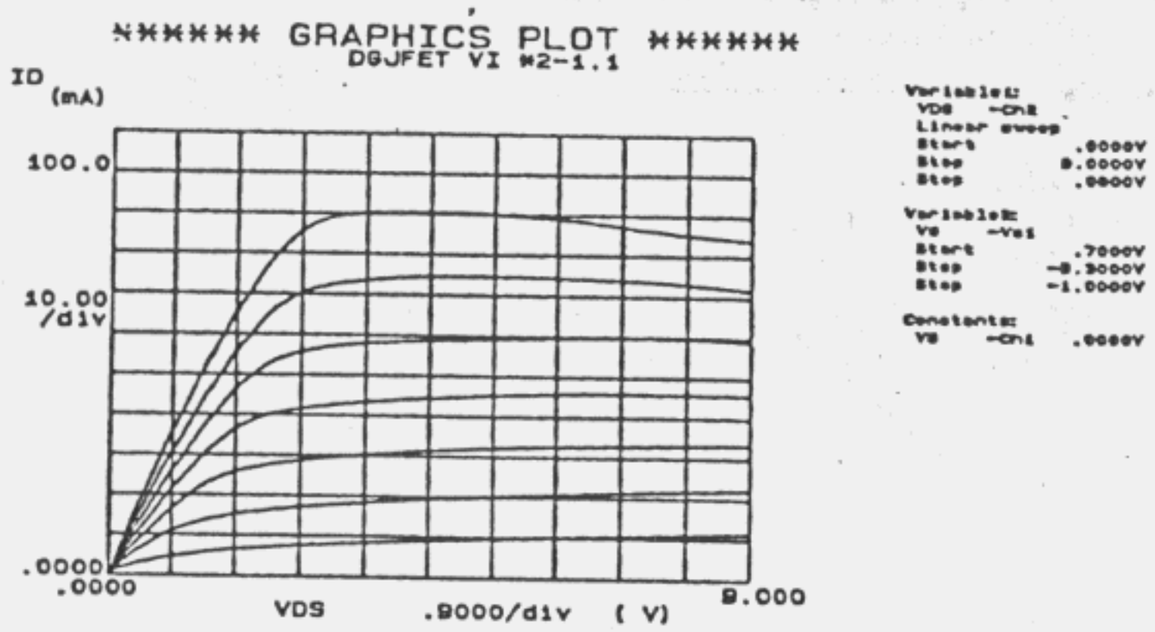

Figure 5. I_{ds}-V_{ds} characteristics of self-aligned JFET. Top curve for V_{gs}=+0.7V, bottom curve for V_{gs}=-5.3V, step =-1V