High Speed and Low Swing Interface Circuits Using Dynamic Over-Driving and Adaptive Sensing Scheme

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Abstract

In this paper, we propose novel interface circuits using Dynamic Over-Driving (*DOD*) and Adaptive Sensing (*AS*) scheme for high speed and energy-efficient interface on a chip. Our *AS*-receiver makes it possible to use very low swing because of its good noise immunity against the threshold voltage variations, and our *DOD*-driver reduces data transmission time even through heavy load capacitances. The simulation results show that the reduction of approximately 20% speed and 40% energy consumption is achieved for the proposed circuits, as compared with the conventional full CMOS inverters at low supply voltage (=1.5V).

1. Introduction

The conventional drive for a continuous scaling of integrated circuits had been the shrink of the systems and the increased speed. However, scaling not only influences the system sizes and performance positively, it also has major negative effects on the reliability and signal integrity of deep-submicron ICs [1]. For example, the RC delay of on-chip global wires increases substantially due to the increase of die size and the difficulty of metal-line scaling [2]. Moreover, the power consumption of wires and clock signals can be up to 40% and 50% of the total on-chip power consumption respectively [3].

Therefore, novel techniques for high speed and energy-efficient interface on a chip are very desirable. Most of the work attempting to optimize the bus energy -delay product can be divided into three categories;

1) design of bus drivers/receivers to decrease the bus swing [4];

2) bus structure redesign to take advantage of local communications [5];
3) encoding techniques to reduce the bus-switching activity [6].

In this paper, we will present a new on-chip interface circuits with novel features such as *DOD*- and *AS*-scheme for high speed and energy-efficient ULSI systems.

2. Test Architecture and Proposed Circuits

Fig. 1(a) illustrates the test architecture for comparing the performance of various interface circuits. The interconnect line is a metal-3 layer wire with a length of 6 mm, modeled by a $\pi 3$ distributed RC model with an extra capacitive load C_L distributed along the wire (for fanout), as shown in Fig. 1(b)[4]. All circuit simulations are based on 0.25μm ANAM CMOS process parameters and HSPICE models.

Fig. 2 presents the modified *SSD-LC* (Symmetric Source-follower Driver with Level Converter) [4] with our novel *DOD*-driver and *AS*-receiver, which are filled with gray. The *SSD-LC* is as simple as the full CMOS inverters, for it needs neither special low-Vt devices nor extra supplies. In addition, the energy-saving ratio of the interconnect with respect to the full CMOS inverters, predicted by (Vdd-Vtn-|Vtp|)/Vdd, is relatively large. This is because the swing of interconnect line is limited between |Vtp| and (Vdd-Vtn).

For the modification of the *SSD-LC*, we have adopted our *AS*-receiver to obtain further energy-savings by reducing the bus swing. Simultaneously, we have also appended our novel *DOD*-driver for improving the speed at low supply voltage. Detailed explanations of our schemes are described as follows.
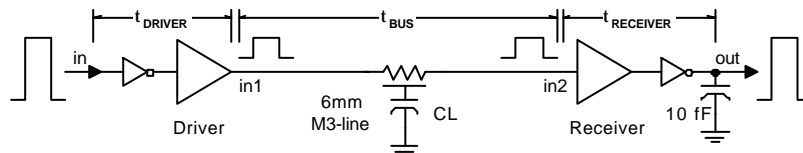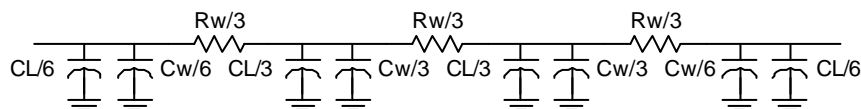

Fig. 1(a) Test architecture

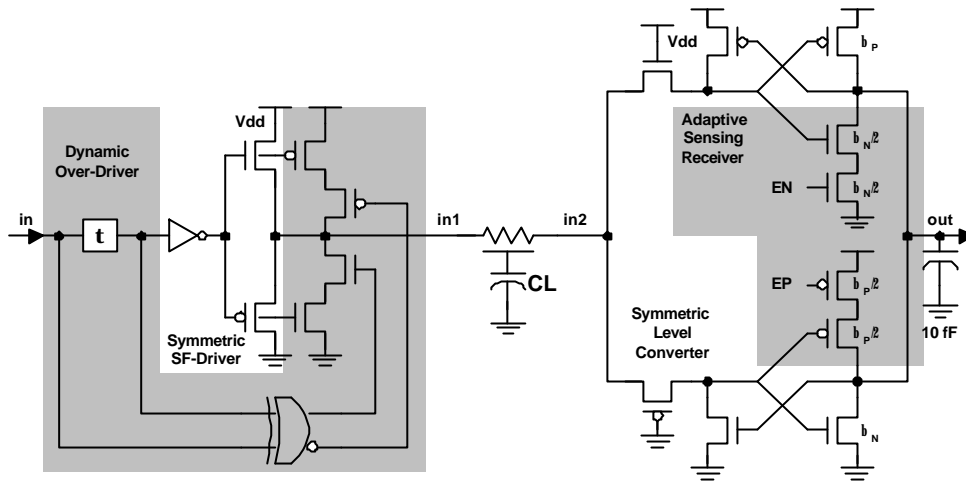**Fig. 1(b)** $\pi 3$ interconnect model with CL (CL=2pF, Rw=650Ω, Cw=0.6pF)

Fig. 2 The modified *SSD-LC* with our proposed *DOD*-driver and *AS*-receiver

3. Adaptive Sensing Scheme

Although the *SSD-LC* is relatively robust with respect to the supply noise and device variations, there is the minimum bus-swing not to be further reduced for reliable operation. The minimum bus swing is bounded by total system noise [7], which is composed of supply-independent noise and supply-dependent noise. However, the threshold voltage offset between driver and receiver, which is the major factor of supply-independent noise, can be reduced by our *AS*-scheme.

In Fig. 3, the simulated output voltage of the *LC* with/ without our *AS*-receiver is plotted against the input voltage (in2). Solid line is the voltage transfer curve of the *LC* without our *AS*-receiver at $\delta Vt=0V$. At the worst case, the Vt's for both n- and p-channel MOSFET's are shifted in the same direction. Moreover, the bus-signal swing limited by the driver is shifted toward the ground, while the transfer curve of the *LC* without our *AS*-receiver is shifted toward the supply. Hence, to balance the gross noise margin, the transfer curve with our *AS*-receiver must be shifted as shown in Fig. 3.

To adapt the sensing threshold voltage to the digitally-trimmed level, δVt or the logic threshold shift must be preliminarily known by the automatic detection procedure from test devices or the given interface circuits. Then, we can trim our receiver by adjusting the (W/L) ratio.

Fig. 4 shows the simulated critical input voltages of the modified receiver as a function of the threshold voltage variations of MOSFET's. The critical input voltage is defined as the input voltage which gives v(out)=Vdd/2. The worst variation of the critical input voltage of the *LC* ranges from 1.12 to 1.28V within δVt of ±100mV. Notice that the curve of the critical input voltages can be shifted to compensate the unbalanced noise margin, when EN or EP is adjusted. Hence, by using our *AS*-scheme, we can reduce the main static noise down to ±25mV within δVt of ±75mV.
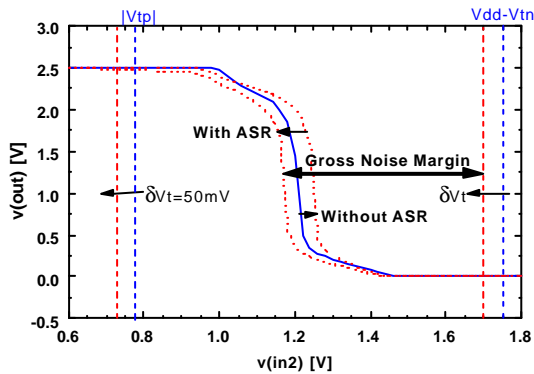

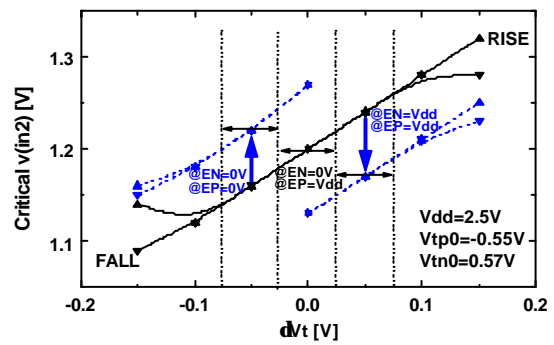**Fig. 3** Voltage transfer curve of the receivers

Fig. 4 Simulated critical input voltage vs. δVt

4. Dynamic Over-Driving Scheme

Rabaey [2] has originally suggested the basic idea of *DOD*-scheme to reduce the on-chip bus delay, but we have designed our *DOD*-driver for increasing the operation range of the *SSD* as well as for reducing the bus delay. This is because serious speed degradation of the *SSD* is observed when the supply voltage is below 2.5V. Therefore, for improving the driving capability of the *SSD*, our *DOD*-driver is dynamically enabled to drive a full-swing signal into the bus during *DOD*-time, whenever data transition between zero and one occurs.

Fig. 5 shows the simulated waveforms of the *SSD-LC* without/with our *DOD*-driver. Notice that the bus delay with the *DOD*-driver is reduced to half that of the *SSD-LC* due to our improved driving capability.

In Fig. 6, we noticed that total delay is reduced abruptly at some *DOD*-time while energy consumption is increased gradually, as the *DOD*-time is increased. Therefore, we have selected the optimal *DOD*-time (= τ_{opt}) by minimizing the energy-delay product.
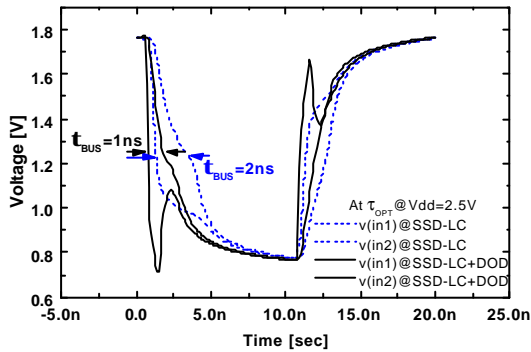

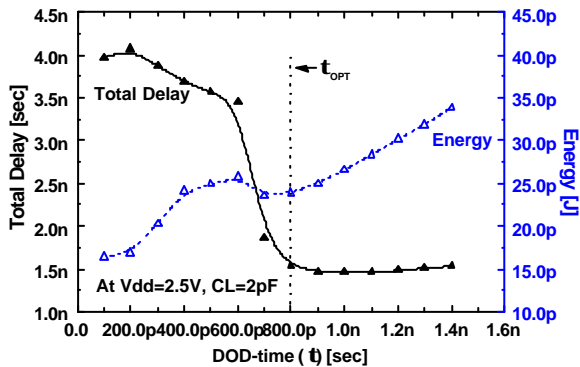**Fig. 5** Simulated waveform with/without *DOD*-scheme

Fig. 6 Delay, Energy vs. *DOD*-time

5. Simulation Results

The effect of the load capacitance on total delay is simulated as shown in Fig. 7(a). Notice that total delay of the proposed driver is still smaller than that of the full CMOS inverters even through heavy load capacitances. The another advantage of our *DOD*-driver is that it is very easy to adapt itself to various loads by simply changing the optimal *DOD*-time.

In Fig. 7(b), the delay times of our interface circuits, described in Fig. 1(a), are compared with those of the conventional inverters. Notice that $\tau_{RECEIVER}$ of our receiver is quite larger due to the reduced output drive currents with the reduced effective gate-voltages, but it is compensated for by the reduction of τ_{DRIVER} and τ_{BUS}.
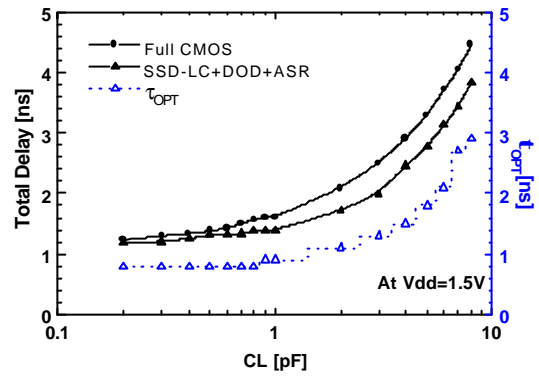

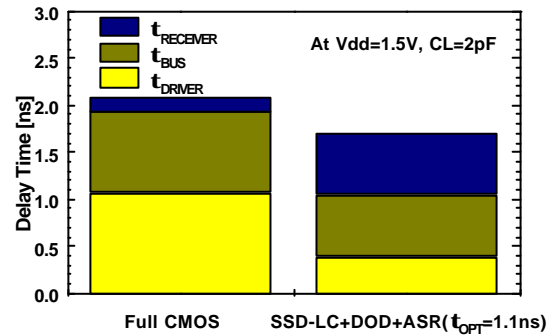**Fig. 7(a)** Delay vs. Capacitive load (CL)

Fig. 7(b) Comparison of delay-time

Fig. 8 shows the simulation results of total delay and energy for various interface circuits. Notice that the *SSD-LC* only works for the supply voltage higher than 2.25V, because of the degraded current-driving capability due to the body effects at the *SSD*. However, our proposed interface circuits work well at Vdd=1.5V with better performances than those of the other circuits.
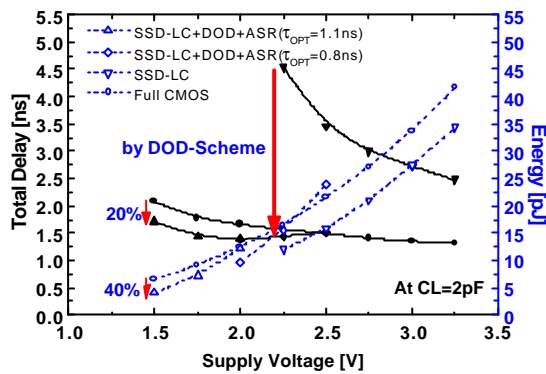
Fig. 8 Delay, Energy vs. Supply voltage

6. Conclusion

High speed and low-swing interface circuits with novel features such as *DOD*- and *AS*-scheme have been proposed. The reduction of 20% speed and 40% energy has been achieved with our *DOD*- and *AS*-scheme, as compared with the conventional CMOS inverters at low supply voltage (=1.5V).

These proposed schemes are still useful for the differential-mode interface circuits, and would give more gains for high speed and energy-efficient interface on a chip.

Acknowledgements

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