SA 18.3: Charge Recycling Differential Logic for Low-Power Application

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Energy efficiency has become one of the most important concerns in VLSI design. Conventional dynamic circuit techniques, which are preferred for high-speed operation, are inefficient as far as power consumption is concerned. Charge-recycling differential logic (CRDL) improves power efficiency by using some of already-used charge for precharge. It has the benefit of improved noise margin due to inherently static operation.

The generic CRDL gate shown in Figure 1 consists of two parts, a complementary output pass-transistor logic network with precharge circuitry, and an acceleration buffer. The pass-transistor logic network is used for logic evaluation. The precharge circuitry consists of a cross-coupled pair of the pMOS transistors, MP1 and MP2, and the nMOS transistor MN1 that connects both the output nodes. The threshold voltages of the pMOS transistors in the cross-coupled pair are relatively higher than other devices. The acceleration buffer, shown inside the dashed line in Figure 1, enhances speed by accelerating pull-down. Transistors MN2, MN3, and MN4 form a sense amplifier, while transistors MP3, MP4, and MN5 generate the output signal Eo. The buffer is enabled through the input Ei, and the output Eo is used as the Ei at the next stage.

As with other precharged dynamic circuits, the CRDL has two phases of operation, namely, the precharge phase and the evaluation phase. In the precharge phase, the clock signal CK goes high, connecting two output nodes to each other through the nMOS transistor MN1. Then, the charge on a pull-up node is shared with the complementary pull-down node setting the voltage level between the extremes. As the threshold voltages of the pMOS transistors in the cross-coupled pair are higher, the precharged value is about half the supply voltage. In the evaluation phase, the clock signal CK goes low, separating the precharged nodes. As the voltage level of one of the precharged nodes goes down by the pass-transistor network for logic evaluation, the other node is pulled high by the cross-coupled pMOS pair recovering a full-supply voltage. Then, the enable input signal Ei turns on the transistor MN4 to activate the sense amplifier, accelerating pull-down. Meanwhile, one of the transistors, MP3 and MP4, in the acceleration buffer, turns on to enable the output Eo which is to be used for activating the sense amplifier at the following stage.

The CRDL has several important advantages over the conventional dynamic logic circuits. First, it uses a precharge scheme in which the charge used for logic evaluation in a cycle is recycled to establish a precharge value in the next cycle. Thus, the CRDL consumes less power than conventional full-swing precharge circuits. In ideal situation assuming that precise half-supply precharge level is achieved, the amount of power consumed is exactly 50% that with a full-swing technique. The charge recycling operation reduces di/dt noise on the supply lines, sometimes a critical problem in conventional circuits. CRDL uses internally stored charge to precharge its output nodes during the precharge phase, resulting in a reduction in the amount of the current from the supply, and thus, the slope of the current variation causing this type of noise. Noise during evaluation also decreases due to reduced voltage swing, resulting in smaller current to and from the supply lines. Another advantage of this logic comes from the fact that there are no noise-sensitive dynamic nodes in the gates implemented with this logic technique. Although the operation of the CRDL is based on precharge and evaluation actions using a clock signal much like the conventional precharge logic circuits, all of the evaluated nodes are connected to either supply or ground rails leading to a static operation. Therefore, it eliminates problems related to dynamic nodes, such as degraded noise margin.

To verify performance, the CRDL current drawn from the supply rail, is compared with those of the conventional logic types such as the differential cascode voltage switch logic (DCVS) [1], and the latched CMOS differential logic (LCDL) [2]. Figures 2 and 3 plot simulation results for the current consumed in each logic circuit with varying the fan-in, and changing load capacitance, respectively. The current drawn by the CRDL is the smallest among all the logic styles compared, indicating that this logic circuit consumes the lowest power.

CRDL and DCVS 8b Manchester carry chains and full adders are benchmark circuits. CRDL implementations of these circuits are shown in Figures 4 and 5, respectively. The 8b carry chain is formed by cascading the carry chain cells in series. The first version is shown in Figure 6a in which the output signal Eo is used at the next stage as the buffer enable signal Ei. Figure 6b shows an improved version where the interconnection of Eo is modified. Eo of each stage is connected to the next 4th stage to reduce the propagation delay by optimizing sense activation timing. With this connection, the speed is improved approximately by 40% over the first version without additional power.

The experimental chip for the first version of the Manchester carry chain uses a 0.8μm 5V CMOS process. Because the threshold voltage adjustment is not feasible in this process, those of the cross-coupled pMOS transistors for the CRDL were changed by applying back-bias voltage so the precharged value is about 3.5V. Figure 7 shows the test circuit chip micrograph and Figure 8, the measured waveform. Table 1 lists the number of transistors, the average currents, delays, and the calculated power-delay products of the 8b carry chains implemented with each of the logic circuits. It shows that the CRDL gives 27% improvement over the DCVS in power-delay product. Simulated performance of the improved carry chain and the full adder shown in Table 2, indicate that the circuits improve power-delay product 54% and 20% over the conventional circuit, respectively.

Acknowledgments:

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References:

[1] Heller, L. G., et al., "Cascode Voltage Switch Logic: A Differential CMOS Logic Family," ISSCC Digest of Technical Papers, pp. 16-17, Feb., 1984.

[2] Wu, C. Y., et al., "Latched CMOS differential logic (LCDL) for complex high-speed VLSI," IEEE Journal of Solid-State Circuit, pp. 1324-1328, Sept., 1991.

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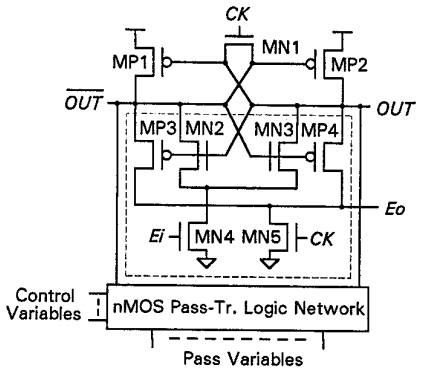

Figure 1: Schematic diagram of charge recycling differential logic.

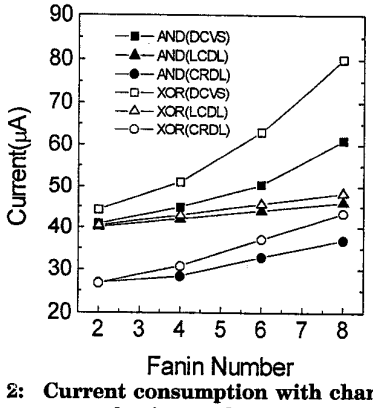

Figure 2: Current consumption with changing fan-in number.

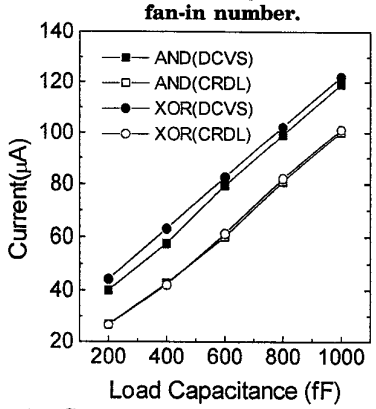

Figure 3: Current consumption with changing load capacitance.

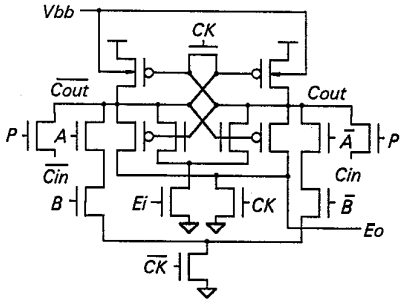

Figure 4: CRDL implementation of the carry chain cell.

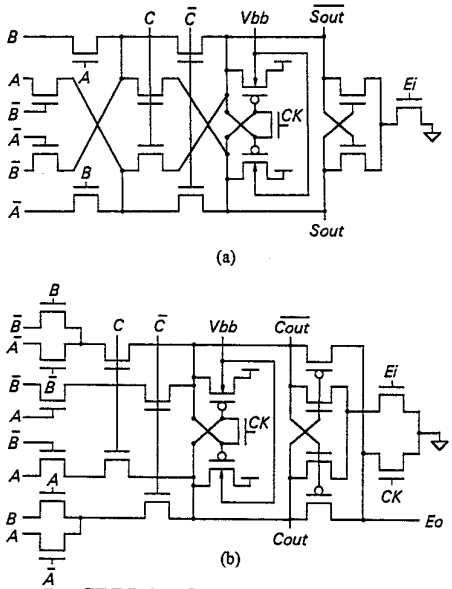

Figure 5: CRDL implementation of the full adder. (a) Sum circuit. (b) Carry circuit.

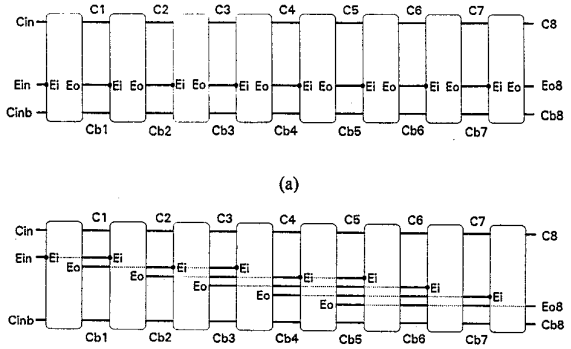

Figure 6: CRDL implementations of the 8b carry chain. (a) First version. (b) Improved version.

Figure 7, Tables 1 and 2: See page 462.

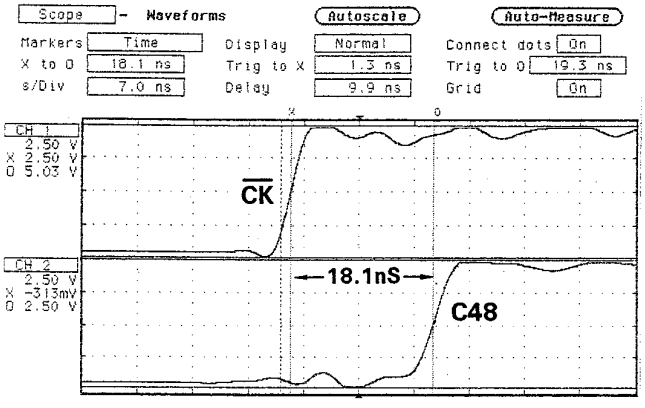

Figure 8: Measured waveform of the CRDL Manchester carry chain (6 stages).

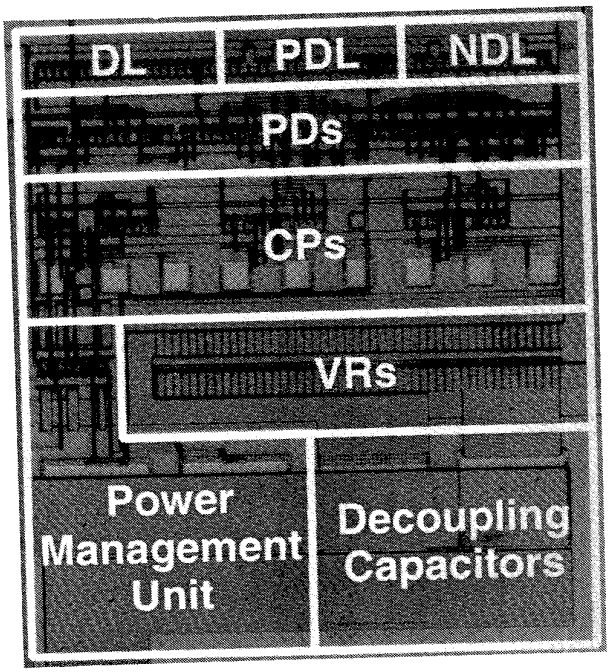

Figure 7: Chip micrograph.

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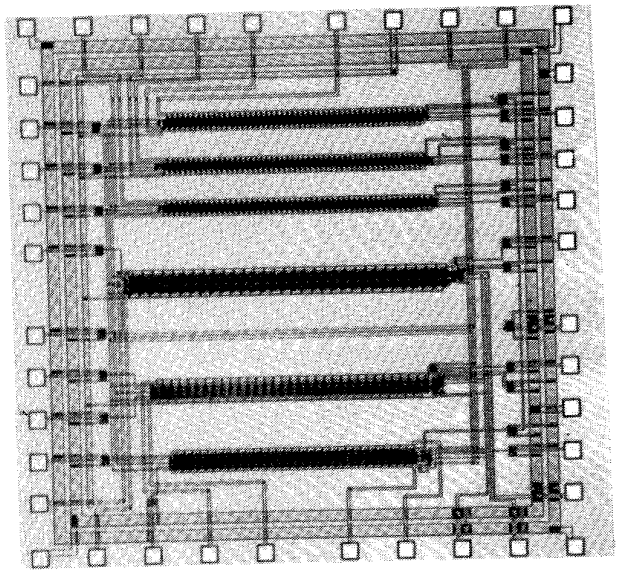

Figure 7: Micrograph of the test circuit.

Number of Transistors	Current (μA)	Delay (ns)	Power-Delay (pJ)
DCVS 106x6	620	17.8	55.18
CRDL 84.6	440	18.1	39.82

Table 1: Measurement result fot the Manchester carry chain.

		Transistor Count	Current (μ)A	Delay (ns)	Power-Delay (pJ)
Carry Chain	DCVS	106	155.3	3.50	2.718
	CRDL	84	114.5	2.17	1.242
Full Adder	DCVS	36	39.4	1.02	0.201
	CRDL	33	26.9	1.19	0.160

Table 2: Simulation result for the carry chain and the full adder.