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THE EFFECTS OF X-RAY IRRADIATION-INDUCED DAMAGE ON RELIABILITY IN MOS STRUCTURES

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Abstract—The effects of X-ray irradiation induced damage on long-term reliability of MOS structures have been investigated. The gate leakage currents at low electric field during a measurement of Fowler-Nordheim tunneling were increased after X-ray exposure, it was explained by the interface trap-assisted tunneling mechanism. This leakage component was completely eliminated by forming gas annealing at 450°C. The long-term reliability of MOS gate oxide is significantly affected by the residual damages in the oxide even after forming gas annealing. In X-ray damaged MOS structures, the average values of cumulative charge-to-breakdown (Q_{bd}) were reduced about 15% as compared with the unexposed devices. The major mechanism responsible for reduction of Q_{bd} in irradiated device is enhanced electron trapping into the neutral traps.

1. INTRODUCTION

X-ray lithography technique is considered to be one of the promising technology in ULSIs generation because of high resolution and overlay capability. However, this process causes radiation damages to devices and circuits, in particular, significant damage is incurred in the gate oxide of MOS structures. The understanding and control of X-ray induced damage in silicon devices are critical to the development of X-ray lithography technology. A lot of studies have been done to characterize the electrical properties and process dependence of this damage[1–5]. There is also much work dealing with annealability of coulombic and neutral traps and their charge centroids[6–8]. All reports show that the X-ray radiation induced damage in MOS structures consists of interface state traps, fixed positive charge (FPC) and neutral electron traps (NET) in the oxide. The FPC and interface states can be eliminated by a low temperature (≤ 500°C) annealing process such as post metalization annealing (PMA) at hydrogen ambient. The NETs are just as readily annealed at low temperature as FPC, but since there are more NETs to start with at rad (SiO_2) levels (< 1 Mrad), and since annealing is a kinetic process, it could be the case that, depending on rad (SiO_2) level the NET type of damage might not be annealed[6–8]. The NETs generated in the back end of lithographic step in MOSFET fabrication is a great concern, because high temperature annealing processing is impossible after metalization. The damage in gate oxide and interface causes changes in I–V characteristics. The degradation by exposure and the recovery by annealing of I–V characteristics have been fully understood[9,10]. Moreover, as a result of the existence of oxide charges and interface states, the MOSFETs have changes in GIDL (Gate Induced Drain Leakage), and in low field gate leakage current. A previous study dealt with the effects of irradiation on the GIDL[11], but the increment of gate leakage current, which is important in thin oxide MOSFETs, has not been addressed. In this paper, the effect of X-ray irradiation on gate leakage current is characterized in Section 3. The effects of remaining NETs after PMA annealing on hot-carrier effects have been studied by many contributors[12–14]. However, until now, the issue of X-ray radiation induced damage on cumulative charge-to-breakdown (Q_{bd}) characteristics has not been fully investigated yet. In Section 4 the effects of X-ray irradiation and forming gas annealing on Q_{bd} characteristics in MOS structures are studied.

2. EXPERIMENTAL PROCEDURE

The samples used in this study were phosphorus doped polysilicon gate nMOSFETs fabricated by the optical lithography technique, like those described in earlier radiation damage studies[2,4–8]. In order to form a P-WELL, a dose of $1.0 \times 10^{13}/cm^2$ borons were implanted into n-type (100) substrate having resistivity of 8–10 Ω-cm. The subsequent drive-in diffusion at 1150°C in dry O_2 ambient for 300 min built the P-WELL with about 3.0 μm junction depth.

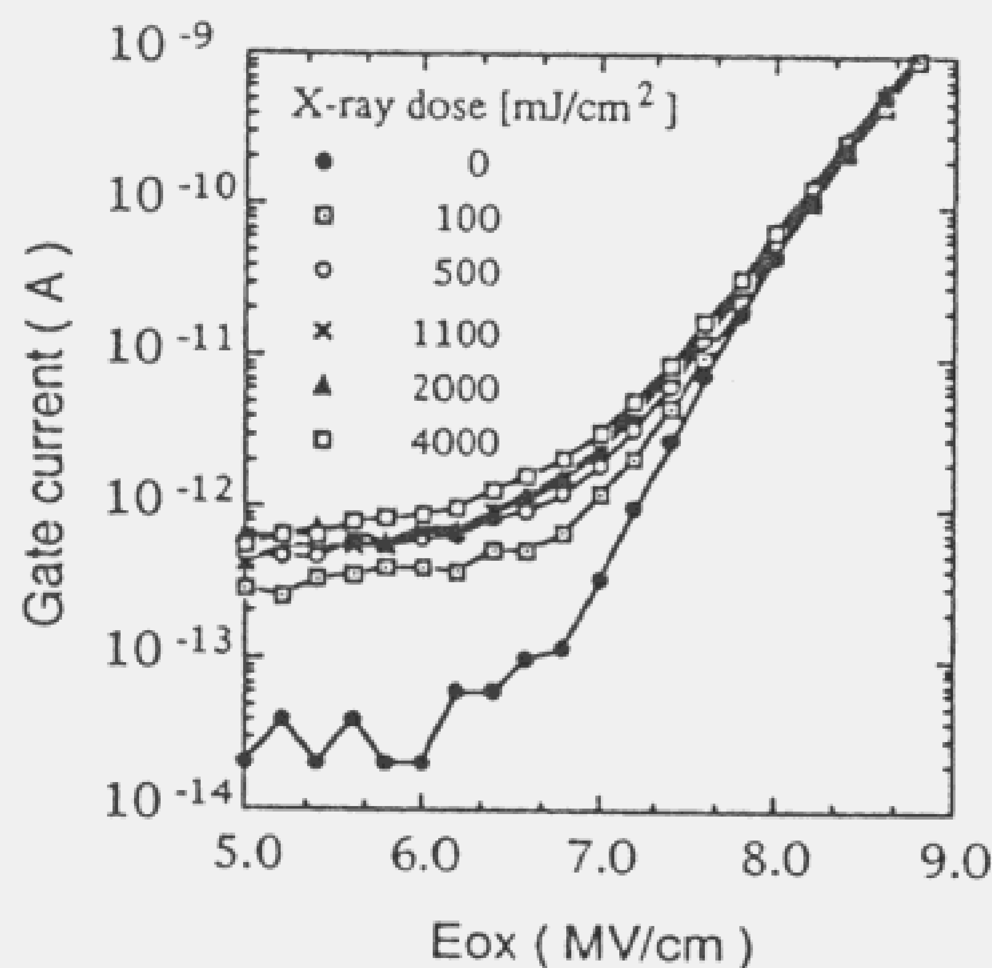

Fig. 1. F–N tunneling characteristics of X-ray exposed *n*MOSFETs before annealing with a gate area of 10^{-4} cm^2. During the measurement, pulsed positive biases were applied to the gate electrode, while the source, drain and substrate electrodes were grounded.

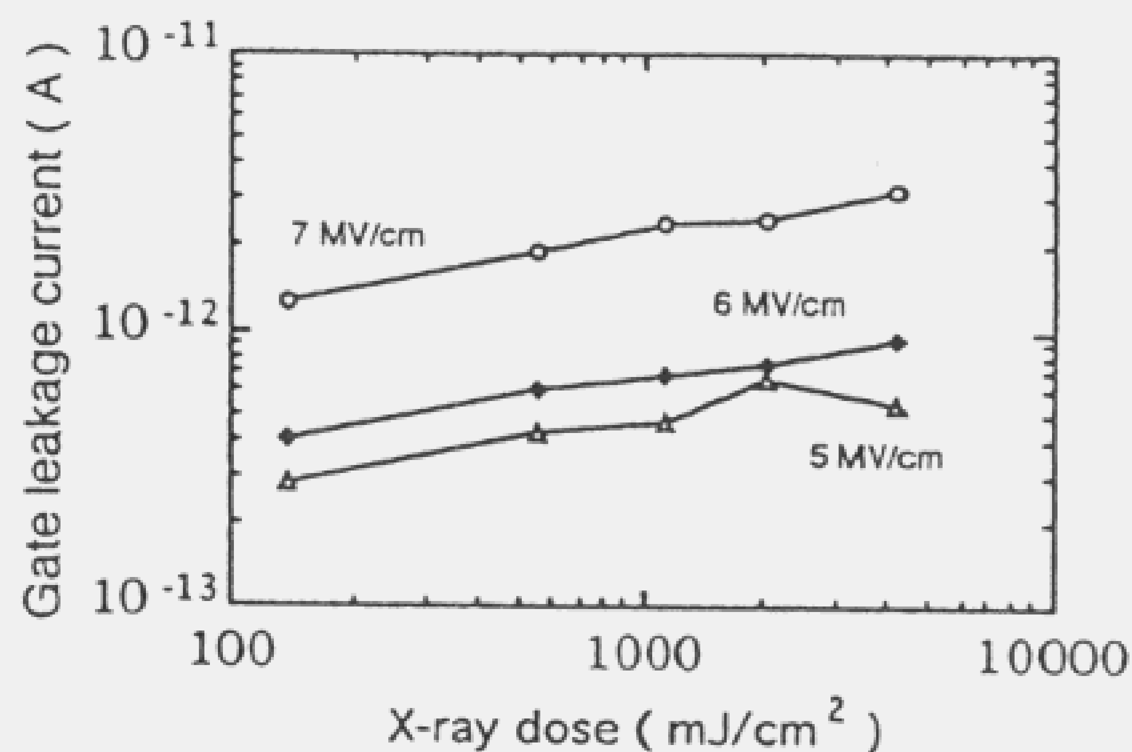

Fig. 3. The magnitude of gate leakage current vs X-ray dosage.

The 100 Å thick gate oxide was grown by dry oxidation with 3% HCl at 900°C, and it was annealed in dry N_2 for 10 min at the oxidation temperature. The threshold voltage is adjusted to 0.5 V by BF_2 implantation (4.5×10^{12}/cm^2). After the entire device fabrication steps, irradiation was done, without external bias, by synchrotron X-ray stepper which has 1.0–2.0 keV radiation energy. The incident X-ray doses were ranged from 100 to 4000 mJ/cm^2, and the corresponding absorbed doses in the gate oxide are from 9.3 to 370 Mrad (SiO_2), respectively. Some of the exposed samples were annealed at 450°C for 30 min in forming gas (10% H_2, 90% N_2). The I–V characteristics and charge pumping currents[15] of devices, before and after annealing and unexposed, were compared to investigate radiation damage and the effects of annealing. The *n*MOSFETs with a gate area of 10^{-4} cm^2 (length of 100 μm and width of 100 μm) were used in the measurement of gate leakage current and charge-to-breakdown characteristics. And charge pumping measurement has been performed using the *n*MOSFETs having length of 0.5 μm and width of 50 μm. The low temperature annealing in forming ambient has completely eliminated the interface states and positive charges.

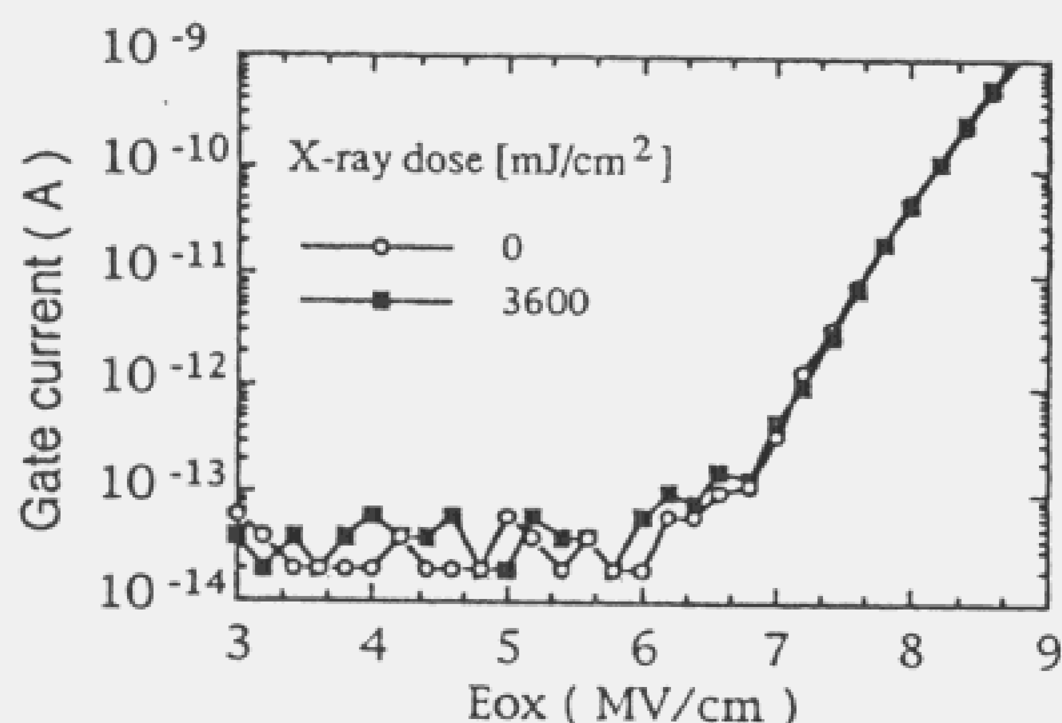

Fig. 2. The F–N tunneling characteristics of X-ray exposed and fresh *n*MOSFETs after forming gas annealing at 450°C for 30 min. The leakage component of current, shown in Fig. 1, is completely eliminated and the tunneling characteristics of the irradiated *n*MOSFET are recovered to those of fresh device.

3. RADIATION INDUCED GATE LEAKAGE CURRENT

Figure 1 shows the Fowler–Nordheim tunneling current vs oxide electric field under positive gate polarity for a fresh and X-ray irradiated *n*MOSFET before annealing. The currents were measured using the HP4142B Modular d.c. Source/Monitor, its minimum detectable current range is 20 fA. As a result of X-ray irradiation at the 100 Å gate oxide, there are distinct changes in leakage current of Fowler–Nordheim tunneling characteristics. At not only low electric field region ($\leqslant$6 MV/cm) but near the onset of tunneling (about 7 MV/cm), the X-ray damage induced leakage current is detectable. The leakage current is reduced rapidly in annealed device and the tunneling characteristics of the *n*MOSFET (X-ray irradiated and annealed) are recovered to those of fresh device, as shown in Fig. 2. The gate leakage current increases with the amount of irradiation dosage. Figures 3 and 4 show the amount of tunneling current at low electric field, and the

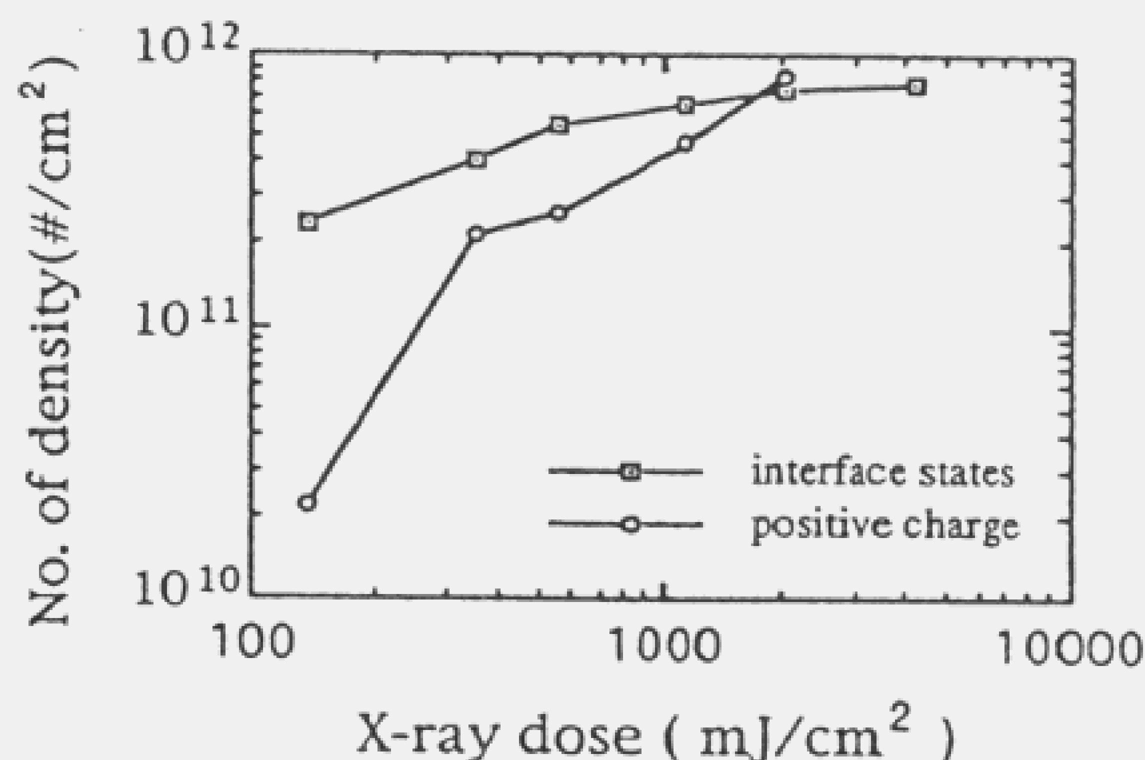

Fig. 4. The magnitude of generated interface state density and positive charge density as a function of irradiated dosage.

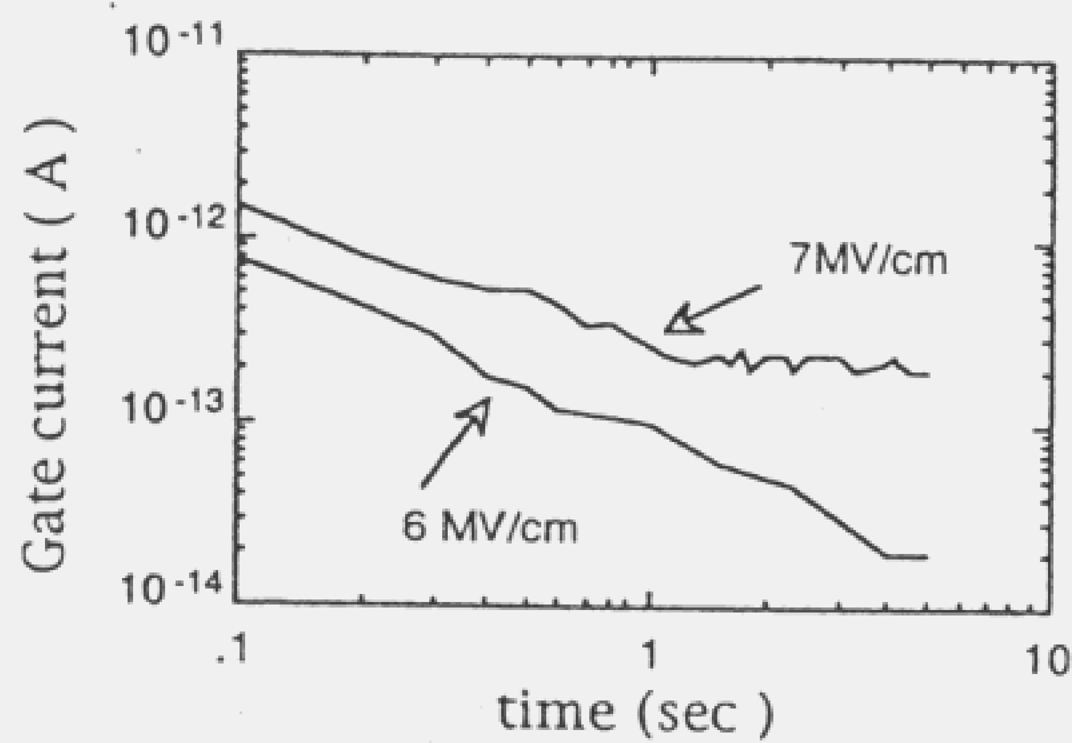

Fig. 5. Transients of gate leakage current of exposed nMOSFET (2000 mJ/cm^2) at different bias conditions.

interface state density and the positive charge density for X-ray irradiated nMOSFETs, respectively, as a function of irradiation dosage. This leakage current is not a steady-state current, rather it shows a $1/t$ dependence on time as shown in Fig. 5. The mechanism of leakage current should be closely correlated with X-ray induced damage in MOS structure mentioned in Refs [1–8]. The positive oxide charge density is increased with X-ray dosage in our measurement. Both the magnitude of leakage current and positive oxide charge density are correlated with the amount of X-ray dosage. This correlation can be used to suggest that the origin of these currents would be positive charge-assisted tunneling mechanism. This charge-assisted model relies on local barrier lowering for tunneling electrons caused by positive charge near the cathode (SiO_2/substrate interface in this study)[16]. The recent studies based on charge centroid measurements indicates that the FPC resides very close to the substrate[6–8]. The leakage is expected to be a steady state tunneling current, because positive charge near the cathode lower the electron barrier. Therefore, this model fails to explain the time dependence of non-steady state transient currents at the 100 Å gate oxide. On the other hand, the correlation of the excess current with the interface state density, shown in Figs 3 and 4, also supports the model that the leakage current in 100 Å oxide is originated from the trap-assisted tunneling mechanism. The results from Figs 1, 3 and 4 show the current is more likely dependent on the interface state density than oxide charge. The interface state induced current was also reported in Fowler–Nordheim stressed thin oxides[17,18]. The interface trap-assisted leakage current at Fowler–Nordheim stressed 100 Å oxide decays gradually, until the trap filling process is completed. The stress induced current transient as well as the X-ray induced leakage current follow the $1/t$ dependence predicted by the trap-assisted tunneling model[17,18]. The time dependent portion of X-ray induced leakage currents, shown in Fig. 5, is more closely fit to trap filling current when bias is applied, rather than those associated with either charge-assisted tunneling conduction or Fowler–Nordheim tunneling. The low temperature annealing process at forming ambient can completely eliminate the interface traps, and X-ray induced gate leakage current returns back to the unexposed value.

4. CHARGE-TO-BREAKDOWN CHARACTERISTICS

Cumulative charge-to-breakdown (Q_{bd}), has been regarded as one of the most important parameters in evaluating the reliability of MOS integrated circuits. In order to measure the value of Q_{bd}, the gate oxide of nMOSFETs was biased with a constant current. A current density of 50 mA/cm^2 was used for positive gate stress (substrate electron injection), and -30 mA/cm^2 was used for negative gate stress (gate electron injection). Figure 6 shows Q_{bd} values for the devices before annealing exposed by different X-ray dosage. In irradiated devices, both negative and positive biased Q_{bd} values are reduced. However, these values are not dependent significantly on the irradiated dosage. Note that the minimum absorbed doses in gate oxide is 9.3 Mrad (SiO_2) in this study. The each columns of Table 1 shows the Q_{bd} values for fresh, X-ray exposed, and annealed after exposed devices, respectively. The breakdown characteristics of the gate oxide of X-ray irradiated nMOSFETs were not improved by low temperature forming gas annealing. We found about 15% reduction of Q_{bd} values in exposed devices, regardless of forming gas annealing. This means that interface states traps and positive oxide charges generated by X-ray exposure do not affect the breakdown mechanism of irradiated thin gate oxide. And this result supports the role of

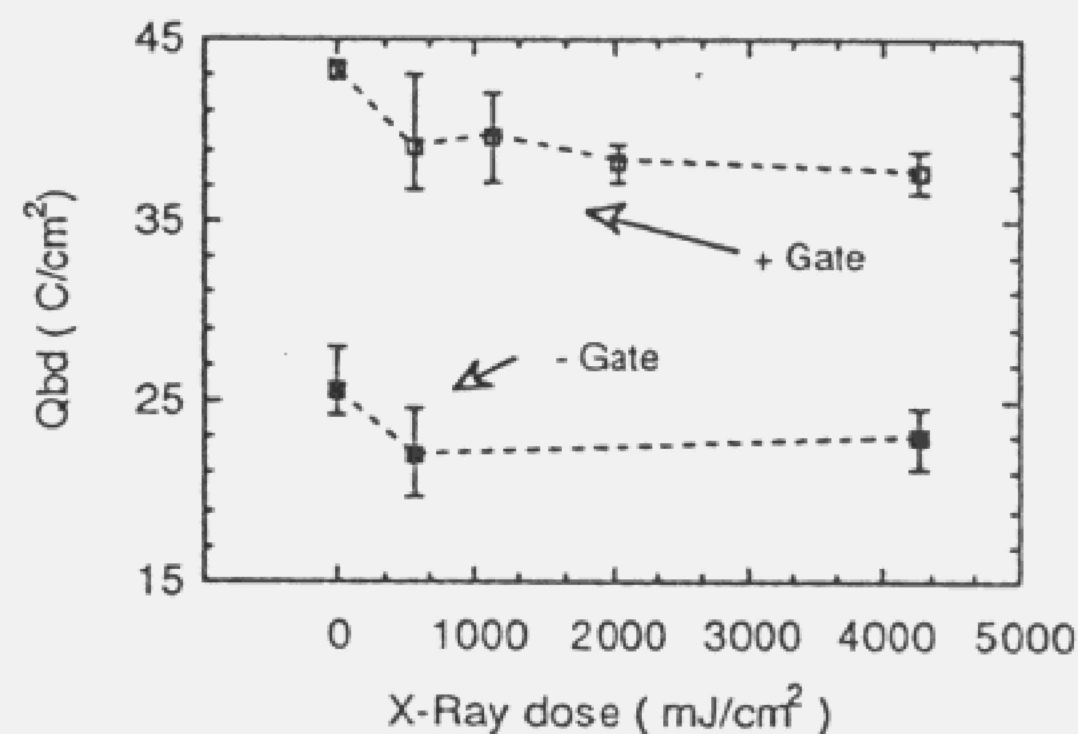

Fig. 6. The values of cumulative charge-to-breakdown as a function of the X-ray dosage. Where " − " sign refers to electron injection from the gate (with -30 mA/cm^2), and " + " sign refers to electron injection from the substrate (with 50 mA/cm^2).

Table 1. Average cumulative charge-to-breakdown values in C/cm^2 for fresh, X-ray exposed, and annealed after exposure devices, respectively

Fresh		X-ray exposed		X-ray exposed and annealed	
+Gate	−Gate	+Gate	−Gate	+Gate	−Gate
43.25	25.60	38.31	22.54	38.67	21.45

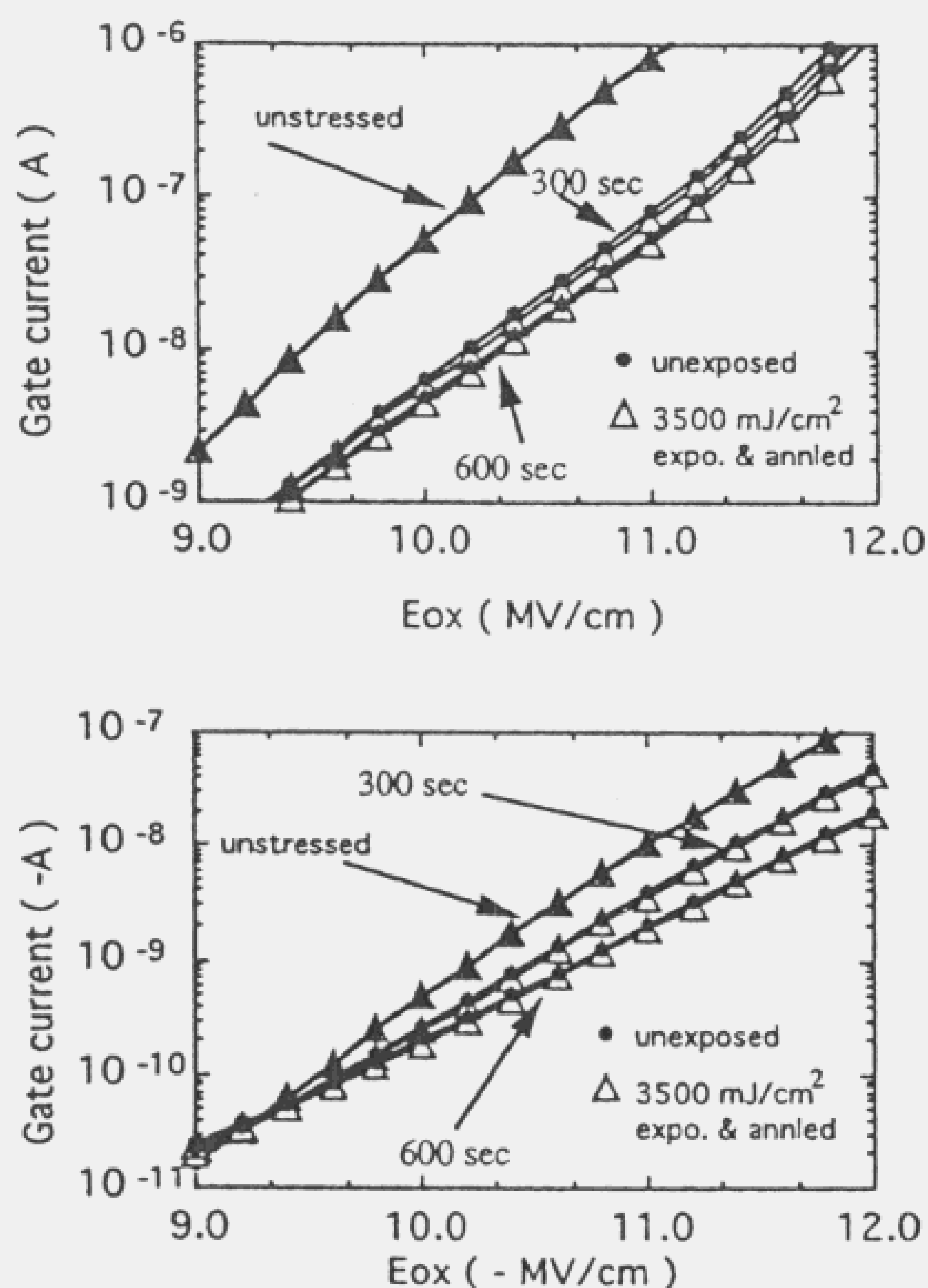

Fig. 7. F–N tunneling characteristics of *n*MOSFETs before and after constant current stress with a current density, $-30\ mA/cm^2$. The stressing time is shown in the figure. Both the unexposed samples and annealed devices have the same tunneling characteristics before the F–N stressing. (a) Substrate electron injection characteristics (positive gate bias). (b) Gate electron injection characteristics (negative gate bias).

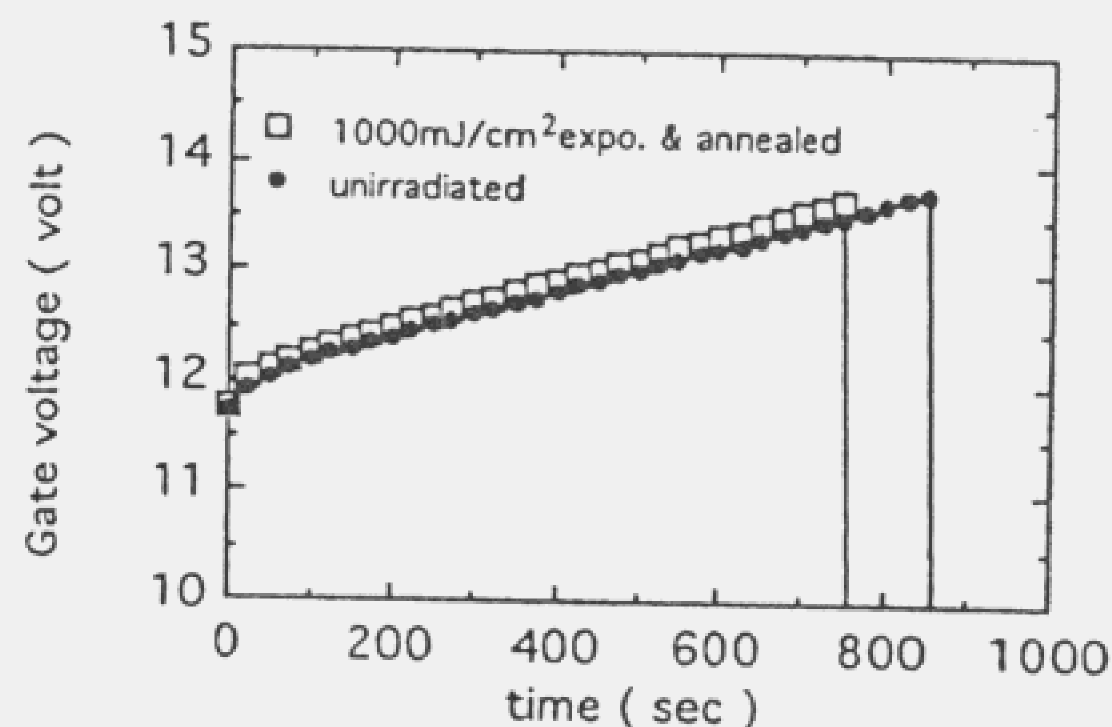

Fig. 8. Gate voltage increment during a constant current ($50\ mA/cm^2$) stressing.

NET in the reduction of Q_{bd}. Figure 7 shows the I_g–V_g curves for the *n*MOSFETs before and after being subjected to constant current stress with a density of $-30\ mA/cm^2$. For positive gate voltage measuring after stressing in Fig. 7(a), F–N tunneling curves are shifted to the right, which indicates that net trapped charge is negative in the oxide. We can observe that the X-ray irradiated device shows enhanced electron trapping rate compared with the unexpected device during stressing. The negative gate I_g–V_g characteristics after stressing, in Fig. 7(b), show reduction in slopes after stressing, but a difference in slopes is not observed between the irradiated and unexposed devices. Here, the reduction of slope indicates positive charge trapping at gate oxide near the cathode region, gate electrode in this case[19]. We cannot find enhancement of hole trapping rate in the annealed devices after X-ray irradiation.

Figure 8 shows a typical breakdown curve for a constant current stressing. The external gate bias voltage is raised as the density of trapped electron increases, because the constant current-bias maintains constant cathode field. Therefore, X-ray damaged devices have to undergo higher external bias than fresh device due to higher rate of electron trapping into NETs.

By these observations, we can conclude that the physical mechanism responsible for the reduction of Q_{bd} in X-ray irradiated gate oxides is enhanced electron trapping into the NETs.

5. SUMMARY AND CONCLUSIONS

The effects of X-ray irradiation damage on gate oxide reliability have been investigated. The excess gate leakage current at low electric field during F–N tunneling measurement was consistent with trap-assisted tunneling mechanism due to the interface traps created by X-ray irradiation. The excess leakage current can be eliminated by low temperature forming gas annealing step. The long-term reliability of MOS gate is significantly affected by the residual damage in the gate oxide even after forming gas annealing. The major mechanism responsible for the reduction of Q_{bd} in irradiated devices is enhanced electron trapping due to neutral electron traps. The degradation of reliability in irradiated MOS structures may become a limitation in the application of X-ray lithography technique to the integrated circuits which require low gate leakage current and high long-term stability such as EEPROM or Flash Memory. Moreover, avoiding the exposure of gate area during radiative process steps is very important in critical application.

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