A Low-Power 270MHz CMOS Direct-PLL FSK Modulator

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Abstract

A 270MHz direct-PLL FSK modulator for low-rate WPAN is implemented. It consumes only 4.9mW adopting current re-using technique and appropriate divider architecture. The 3rd order Delta-Sigma Modulator (DSM) and the high performance charge pump are designed for wide loop bandwidth, which enables to design a low power and low noise frequency synthesizer. The implemented prototype offers 500kHz loop-bandwidth and -104dBc/Hz in-band noise. It also plays a role of FSK modulator which shows only 1.1dB degradation at 10^{-3} BER compared with the ideal modulator.

1. Introduction

In mobile communication systems, especially for Low-Rate Wireless Personal Area Network (LR-WPAN) system, low power capability is the essential property because it brings the long battery life and good autonomy.

Fig. 1 shows the prototype block diagram of 4th order PLL direct modulator. While the conventional I/Q modulator requires two DACs, LPFs, an up-mixer, and a frequency synthesizer, this architecture needs only a frequency synthesizer. This simple architecture can lead to extremely low power consumption, and is suitable for the transmitter of LR-WPAN system.

In PLL direct modulator, wide loop bandwidth is highly desired because of two reasons. Firstly, high energy-efficiency is required for low power applications. Therefore, fast startup time of a frequency synthesizer is very important, which is dominated by loop bandwidth [1]. Second, the loop bandwidth limits the modulation data rate and as the higher data rate, the wider loop bandwidth is required.

Several papers have made an effort for the high data rate transmission with the narrow loop bandwidth such as pre-amplifying scheme [2] or two-port modulation [3]. But these schemes require the exact matching, which means hard trimming or additional power consumed calibration circuitry. Therefore, for increasing data rate, the bandwidth widening approach is more suitable for energy efficient LR-WPAN system.

2. Circuit Implementation

Low-noise 3rd order feedback type DSM with 1-bit quantized output is implemented externally for the flexible measurement for this prototype and 41MHz reference frequency was chosen for the sufficient suppression of the DSM quantization noise.

To ensure the excellent I/Q signal, VCO output frequency is set to 540MHz, twice of RF carrier frequency, and a fixed divide-by-2 circuit is used. Frequency divider is composed of the combination of Current Mode Logic (CML) and CMOS static logic. In high frequency band, such as fixed divide-by-2 and divide-by-2/3, CML scheme is adopted, while the other low frequency circuits are implemented using CMOS static logic, which shows good power efficiency. Further reduction of power consumption was obtained by current re-using and self-DC biasing techniques.

The designed charge pump is shown in Fig. 2. In order to use high reference frequency for wide loop bandwidth, charge pump should be carefully designed because the rising and falling time can be ignored no longer. Furthermore, mismatches affect in-band noise characteristic and reference spurious tone power. To prevent up/down DC current mismatch, replica and error feedback circuits are implemented. When the current is switched by the input, inserted unity gain OP-amp helps to minimize the non-ideal charge re-distribution effect.

3. Experimental Results

The 270MHz prototype modulator was fabricated using 0.18um CMOS with the consumption of 1135um × 726um die area.

Measured phase noise performance is as low as –104dBc/Hz at 10kHz offset and DSM quantization noise is –100dBc/Hz at 2MHz offset, with the power consumption of only 4.9mW. These results have enough margins to meet the requirements of LR-WPAN application.

The settling time is less than 7usec when output frequency moves from the lowest to the highest of the application frequency band. This fast turn-on time successfully leads to meet low power consumption of the entire system.

Fig. 3 shows the modulated output spectrum for the input chip sequence of '101010…', which is assumed as the worst case input, with the rate of 231kcps. Based on the measured output waveform, BER performance was estimated , as shown in Fig. 4 , under the assumption of direct conversion receiver and semi-coherent demodulator. The result shows only 1.1 dB degradation at 10^{-3} BER compared with the ideal FSK-modulator.

Comparison results of overall performance with other works are summarized in Table. 1, in which this work records the lowest ratio of f_{ref} / f_{BW} , where f_{ref} is reference frequency and f_{BW} is loop bandwidth. Although VCO frequency is considered, this work has excellent power and noise performance.

4. Conclusion

A 270MHz direct-PLL FSK modulator with 500kHz loop bandwidth is implemented. It consumes only 4.9mW adopting

current re-using technique, self-DC biasing scheme, and appropriate divider architecture. The 3rd–order feedback type DSM and the high performance charge pump help to achieve wide loop bandwidth, which enables to design a low power, low noise frequency synthesizer.

Acknowledgement

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References

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Ref	[4]	[5]	[6]	This Work
Tech	0.5um CMOS	0.35um CMOS	0.35um BiCMOS	0.18um CMOS
f_{VCO} [MHz]	900	900	2500	540
f_{ref} [MHz]	8	13	8	41
f_{BW} [kHz]	40	90	35	500
f_{ref} / f_{BW}	200	144	229	82
Phase Noise [dBc/Hz] @ 10kHz	-92	-80	-82	-104
Power [mW]	29	17.4	16	4.9
Etc	w/o VCO		w/o VCO	w/o DSM

Table. 1 Performance comparison with other works

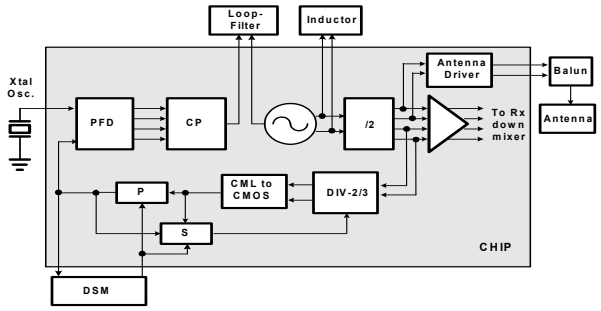

Fig. 1 Functional block diagram of prototype system

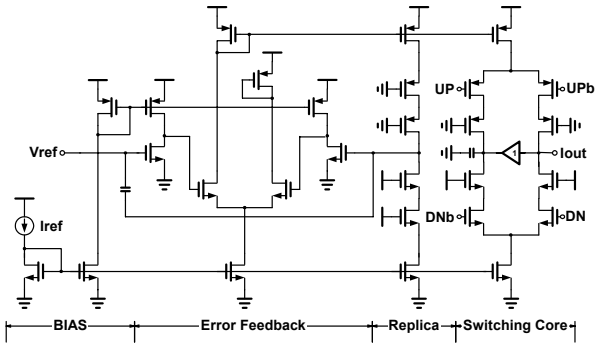

Fig. 2 Circuit diagram of charge-pump

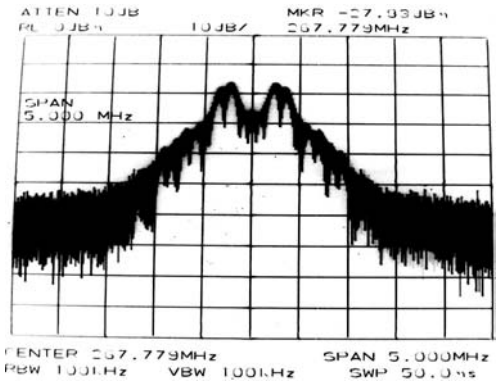

Fig. 3 Modulated output spectrum

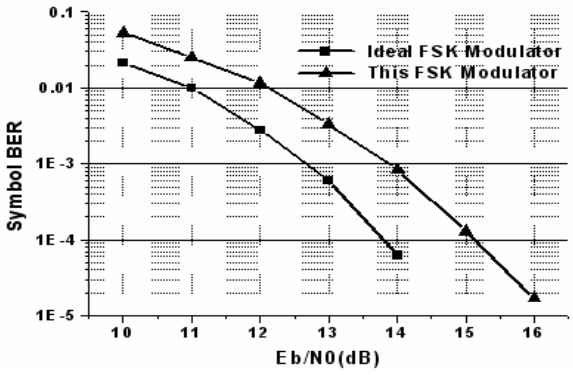

Fig. 4 Estimated BER performance comparison