Resistance Matrix in Crosstalk Modeling for Multiconductor Systems

Sunil Yu[1, 3], Dusan M. Petranovic[2], Shoba Krishnan[1], Kwyro Lee[3], and Cary Y. Yang[1]

[1] Nanoelectronics Laboratory, Santa Clara University, Santa Clara, CA,
[2] Mentor Graphics Corporation, [3] Dept. of EECS and MICROS Research Center, KAIST, Korea
E-mail : syu@scu.edu

Abstract

A complete modal analysis is introduced to derive the crosstalk voltage waveform in multiconductor coupled systems. In addition to the capacitance and inductance matrices, it also includes a resistance matrix. The off-diagonal terms of the resistance matrix are related to the return path, which is important for accurate noise modeling at high frequency. It is shown that the error in crosstalk peak noise can be as high as 30% if the return path resistance is ignored. This work completes a previous modal analysis of a multiconductor system and significantly improves accuracy of crosstalk noise estimation, which is becoming increasingly important in design of deep-submicron integrated circuits.

1. Introduction

With the advancement of process technologies into deep-submicron regimes, the aspect ratio of the interconnect lines is becoming larger. As a consequence, the crosstalk noise between signal lines becomes more severe through capacitive and inductive coupling. For successful design and verification it is important to come up with an accurate and efficient way to approximate crosstalk noise at various levels of design abstraction. Significant efforts have been made recently to develop a noise model that could be used in the early stage of chip design [1-5]. The previous models expressed the crosstalk noise using Heaviside's expansion [1], modified Bessel function [2], and TWA (Traveling-wave-based Wave Approximation) [3]. In all cases, a modal analysis technique to analyze crosstalk noise for two or more lines was used. Modal analysis is an eigenmode method for characterizing a given interconnect structure. For an N-conductor structure, coupled transmission line equations can be transformed to N single isolated equations through modal analysis. As a result, if we know the solution for a single line, it is easy to get the solution for the coupled multi-line structure by recombining modal results. To perform this analysis, the extracted transmission line parameter matrices for inductance, capacitance, and resistance must be transformed. However, previous works [1-4] considered only the diagonal terms of the resistance matrix and ignored the off-diagonal terms which are related to the return path resistance. They still yielded good results in the low-frequency regime due to large return area. However, at high frequencies, when the return path is confined around the signal line to reduce the impedance of the loop, the resistance becomes important and a significant error in noise estimation can occur. In this paper, we investigate the effects of the resistance matrix on the noise analysis and show how inclusion of the resistance of the return path can significantly improve the noise approximation results.

2. Modal Analysis for Crosstalk

To analyze crosstalk noise, we first consider a two-line structure as shown in Fig. 1. The buffers driving the interconnect lines are modeled as voltage sources with a source resistance and the receivers connected at the end of the lines are modeled as capacitors. After applying the Kirchhoff's voltage and current laws to this system (two identical lines), the transmission line equations are given

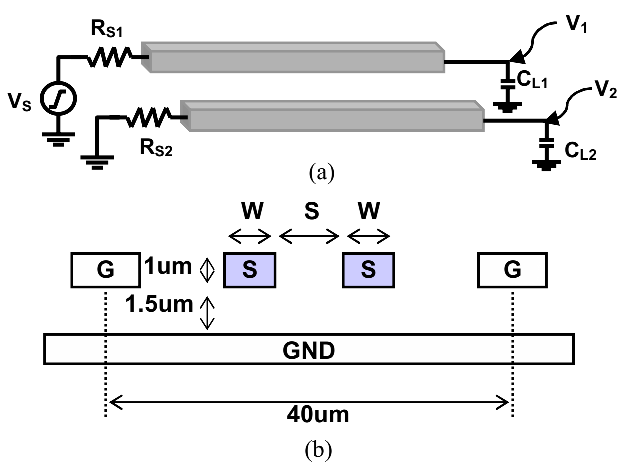


Fig. 1. Two-conductor system with a driver resistor and load capacitor. (a) circuit diagram (b) cross section.

0-7695-2093-6/04 $20.00 © 2004 IEEE

IEEE COMPUTER SOCIETY

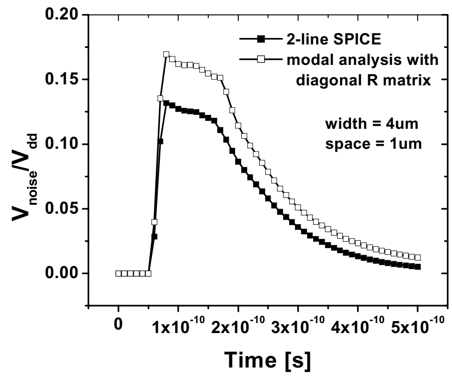


Fig. 2. Noise voltage induced on a victim line in Fig. 1 for two-line SPICE simulation and modal analysis with diagonal resistance matrix. Rise time is 10ps. Source resistance and load capacitance are 25ohm and 0.1pF, respectively.

by

$$\frac{\partial^2}{\partial z^2}\begin{bmatrix}V_1\\V_2\end{bmatrix}=\begin{bmatrix}R & 0\\0 & R\end{bmatrix}\begin{bmatrix}C_s+C_m & -C_m\\-C_m & C_s+C_m\end{bmatrix}\frac{\partial}{\partial t}\begin{bmatrix}V_1\\V_2\end{bmatrix} +\begin{bmatrix}L_s & L_m\\L_m & L_s\end{bmatrix}\begin{bmatrix}C_s+C_m & -C_m\\-C_m & C_s+C_m\end{bmatrix}\frac{\partial^2}{\partial t^2}\begin{bmatrix}V_1\\V_2\end{bmatrix}, \quad (1)$$

where R is the line resistance and C_s, C_m, L_s, and L_m are the line self capacitance, mutual capacitance, self inductance and mutual inductance, respectively [2, 3]. In this equation, the resistance matrix is assumed to be diagonal as in previous works [1-4]. Using modal voltages as $V_+=V_1+V_2$ for in-phase mode and $V_-=V_1-V_2$ for out-of-phase mode, we can transform the equations of the system to a diagonal form:

$$\frac{\partial^2}{\partial z^2}\begin{bmatrix}V_+\\V_-\end{bmatrix}=\begin{bmatrix}R & 0\\0 & R\end{bmatrix}\begin{bmatrix}C_s & 0\\0 & C_s+2C_m\end{bmatrix}\frac{\partial}{\partial t}\begin{bmatrix}V_+\\V_-\end{bmatrix} +\begin{bmatrix}L_s+L_m & 0\\0 & L_s-L_m\end{bmatrix}\begin{bmatrix}C_s & 0\\0 & C_s+2C_m\end{bmatrix}\frac{\partial^2}{\partial t^2}\begin{bmatrix}V_+\\V_-\end{bmatrix} \quad (2)$$

From equation (2), the modal inductance and capacitance matrices of the two-conductor transmission line system can be written as follows.

$$[L_{\mathrm{mod}}]=\begin{bmatrix}L_s+L_m & 0\\0 & L_s-L_m\end{bmatrix} \quad (3)$$

$$[C_{\mathrm{mod}}]=\begin{bmatrix}C_s & 0\\0 & C_s+2C_m\end{bmatrix} \quad (4)$$

From equations (3) and (4), we can use $L_+=L_s+L_m$ and $C_+=C_s$ to represent interconnect parameters for in-phase mode and $L_-=L_s-L_m$ and $C_-=C_s+2C_m$ for out-of-phase mode, respectively. After obtaining the modal solutions, V_+ and V_-, line voltages, V_1 and V_2, can be calculated with appropriate initial conditions.

This modal method with diagonal resistance matrix is compared with 2-line SPICE simulation for a switching condition when line 1 switches from logic 0 to 1 and line 2 remains at logic 0 (Fig. 2). A distributed model (W element) for transmission line is used in the SPICE simulation and a commercial field solver [6] is used to extract transmission line parameters. Although the shapes of the noise waveforms are quite similar to each other, the error of the peak noise shows over 30%. This error is a result of neglecting the non-zero off-diagonal terms in the resistance matrix, as will be explained in the next section. Overestimation of crosstalk noise may mislead the chip designers to space signals further apart or add additional shielding, resulting in larger chip area.

3. Properties of Resistance Matrix

In general, a resistance matrix can be expressed as

$$[R]=\begin{bmatrix}R_{11} & R_{12}\\R_{12} & R_{22}\end{bmatrix}, \quad (5)$$

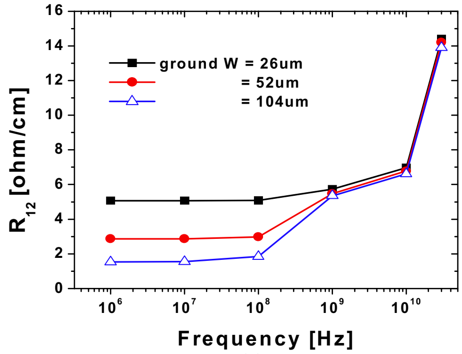
where R_{11} and R_{22} are the sums of the resistance of the corresponding signal line and the resistance of a return path for each line at low frequency. The real part of the mutual impedance, R_{12}, is related to the return path. If we consider an ideal return path (perfect conductor or very large return area), R_{12} will be close to zero and the resistance matrix will become diagonal at low frequency. However, in reality, the return path is not perfect ground and has some resistance. An ideal return path is a good assumption for low-frequency regime because the return current flow spreads throughout the entire return path or the ground plane to reduce the resistance. However, when the operating frequency increases, the return current will flow near the signal line to reduce the impedance of the loop [7, 8] and the off-diagonal terms of the resistance matrix will be non-zero. For example, a resistance matrix for two 1-cm long coupled interconnect lines with 4μm width and 1μm spacing at 10GHz is given by

$$[R_{two}]=\begin{bmatrix}67.5 & 6.9\\6.9 & 67.5\end{bmatrix}\quad[\Omega/cm]. \quad (6)$$

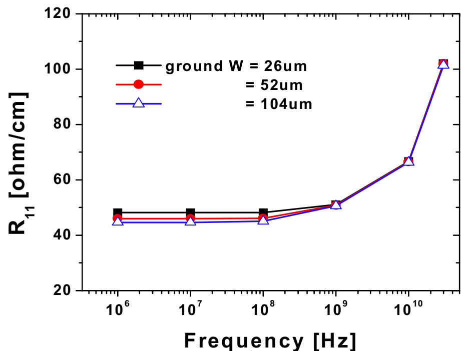
Fig. 3 shows how R_{11} and R_{12} change with frequency for various dimensions of the ground plane. Below 100MHz, because the return current flows through the entire ground plane, R_{12} depends on the ground plane dimension.

0-7695-2093-6/04 $20.00 © 2004 IEEE

IEEE COMPUTER SOCIETY



(a)



(b)

Fig. 3. Resistance versus frequency characteristics for various ground plane widths. (a) R_{12} characteristics (b) R_{11} characteristics. The widths and space of signal lines are 4μm and 1.5μm, respectively. R_{12}s are quite different for various ground plane sizes at low frequency regime.

However, the difference among the three dimensions diminishes when the operating frequency goes above 1GHz, since the current return path becomes narrower. Thus resistance for a multiconductor system should be treated in full matrix form and not just diagonal. The differences among self-resistances, R_{11}, are relatively small for various ground sizes, and a steep increase at very high frequencies is due to skin and proximity effects.

Substituting equation (5) into equation (1) and applying the in-phase and out-of-phase voltage transformations, the modal matrix of resistance can be obtained as

$$[R_{\text{mod}}]=\frac{1}{2}\begin{bmatrix} R_{11}+R_{22}+2R_{12} & R_{11}-R_{22} \\ R_{11}-R_{22} & R_{11}+R_{22}-2R_{12} \end{bmatrix}. \quad (7)$$

This matrix would be diagonal for two identical lines. Equations (3), (4). and (7) provide a complete set of modal matrices for transmission line parameters, from which the crosstalk noise voltage can be obtained by solving equation (2). Fig. 4 shows the simulated crosstalk noise voltage obtained with various methods. The result

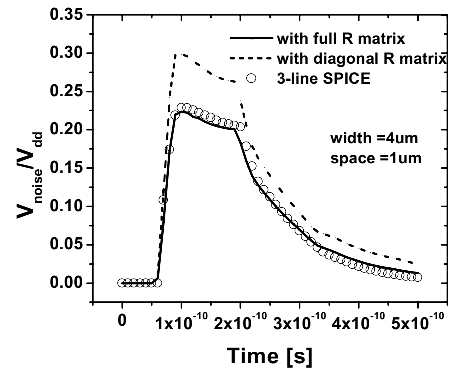


Fig. 4. Crosstalk noise voltage waveform induced on a victim line for modal analysis with a full resistance matrix, with diagonal resistance matrix and two-line SPICE simulation. Input rise time is 10ps.

(a)

(b)

Fig. 5. Current distribution in two-conductor transmission line system at 10GHz (a) in-phase mode (b) out-of-phase mode. The brighter color means higher current density.

obtained using a complete resistance matrix matches well with the result obtained from SPICE simulation.

Fig. 5 shows current distributions for the in-phase and out-of-phase conditions [6]. The widths of lines are 4μm and spacing is 1.5μm. The distance from a ground plane is 1.5μm and driving frequency is 10GHz. At this frequency, the return current in the ground plane is confined to the region directly underneath the signal lines, giving rise to higher resistance. This phenomenon results in increased impedance in the in-phase mode and decreased impedance in the out-of-phase mode. These two conditions of return current distribution are consistent with the modal parameters for resistance.

The methodology presented in this paper can be extended to a multiconductor transmission line system. Fig 6 shows a schematic of a three-conductor transmission line system. In this system, the worst crosstalk noise occurs in the center line when the two outer lines are switched simultaneously. The three methods, 1) SPICE simulation, the modal analysis with 2) full resistance

0-7695-2093-6/04 $20.00 © 2004 IEEE

IEEE COMPUTER SOCIETY

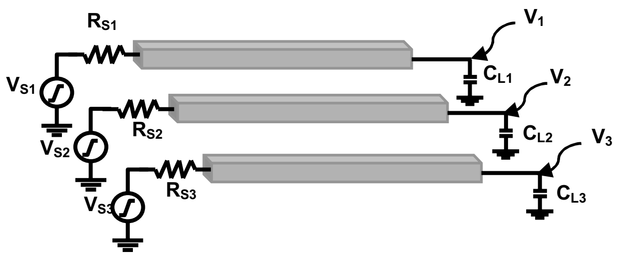


Fig. 6. Three-conductor transmission line system.

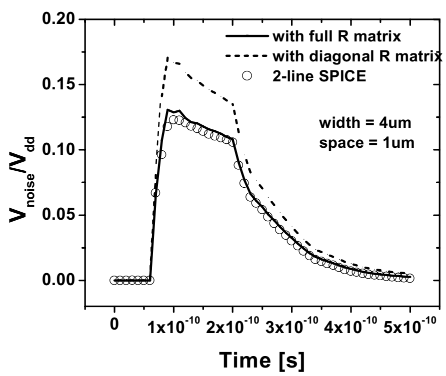
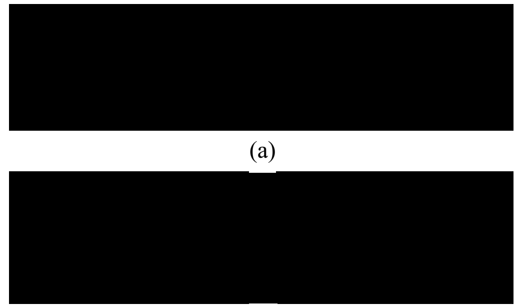


Fig. 7. Voltage waveforms induced on center line in three-conductor transmission line system when the two outer lines are simultaneously switched and the center line remains quiet. Input rise time is 10ps.

matrix ,and 3) diagonal resistance matrix are compared. The results shown in Fig. 7 again confirm that the full resistance matrix is necessary to obtain accurate crosstalk noise estimation. The return current distribution is related to the switching condition of each line. The distributions for the two basic conditions are shown in Fig. 8. The (↑↑↑) condition means that the three lines are switching in phase, which has the largest characteristic impedance. The (↓↑↓) condition produces the largest signal delay in the central signal line because the capacitance coupling between center and outer lines is maximized under this condition [9].

4. Conclusion

A complete modal analysis including full resistance matrix is presented to derive crosstalk waveform in multiconductor coupled systems. The error in crosstalk peak noise can be up to 30% in a two-conductor transmission line system if a single value of resistance is used instead of a full resistance matrix. We derived a modal resistance matrix from transmission line equations. The crosstalk waveform using full resistance matrix matches well with the result obtained from SPICE simulation. The relation between switching mode and current distribution is also investigated. Our work improves upon a previous modal analysis of a multiconductor system and produces accurate crosstalk estimation, which is essential for IC design and verification.



(a)

(b)

Fig. 8. Current distribution in three-conductor transmission line system at 10GHz (a) (↑↑↑) condition (b) (↓↑↓) condition.

5. References

[1] T. Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI's," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 118-124, Jan. 1993.

[2] J. A. Davis and J. D. Meindle, "Compact Distributed RLC interconnect Models-Part II; Coupled Line Transient Expression and Peak Crosstalk in Multilevel Network," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2078-2087, Nov. 2000.

[3] Y. Eo, S. Shin, W. R. Eisenstadt and J. Shim, "Generalized Traveling-Wave-Based Waveform Approximation Technique for the Efficient Signal Integrity Verification of Multicoupled Transmission Line System," *IEEE Trans. Computer-Aided Design*, vol. 21, no. 12, pp. 1489-1497, Dec. 2002.

[4] R. Venkatesan, J. A. Davis and J. D. Meindl, "Compact Distributed RLC Interconnect Models-Part IV; Unified Models for Time Delay, Crosstalk, and Repeater Insertion," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1094-1102, Apr. 2003.

[5] S-C. Wong, G-Y. Lee, and D-J. Ma, "Modeling of Interconnect Capacitance, Delay, and, Crosstalk in VLSI," *IEEE Trans. Semiconductor Manufacturing*, vol. 13, no. 1, pp. 108-111, Feb. 2000.

[6] *Maxwell Q2D/Q3D Parameter Extractor User's Guide*, Ansoft Corp., Pittsburgh, PA 2003

[7] S-P. Sim, S. Krishnan, D. M. Petranovic, N. D. Arora, K. Lee and C. Y. Yang, "A Unified RLC Model for High-Speed On-Chip Interconnects," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1501-1510, Jun. 2003.

[8] B. Krauter and S. Mehrotra, "Layout based frequency dependent inductance and resistance extraction for on-chip interconnect timing analysis," *Proc. DAC.*, 1998, pp. 303-308.

[9] S. H. Hall, G. W. Hall and J. A. McCall, *High-Speed Digital System Design*. Wiley-Interscience, 2000, chapter

0-7695-2093-6/04 $20.00 © 2004 IEEE

IEEE COMPUTER SOCIETY