CMOS RF Modeling and Parameter Extraction Approaches Taking Charge Conservation into Account

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Outline

- Introduction
- KAIST approach for RF CMOS modeling
- Small signal parameter extraction method
- Model verification
- Comparison with other models
- Large signal I-V and Q-V model construction
- Conclusions and future prospects

Introduction

- CMOS as RF technology
- Review of III-V MESFET/HFET works
- Root's proposal
- Required accuracy for RF transistor models

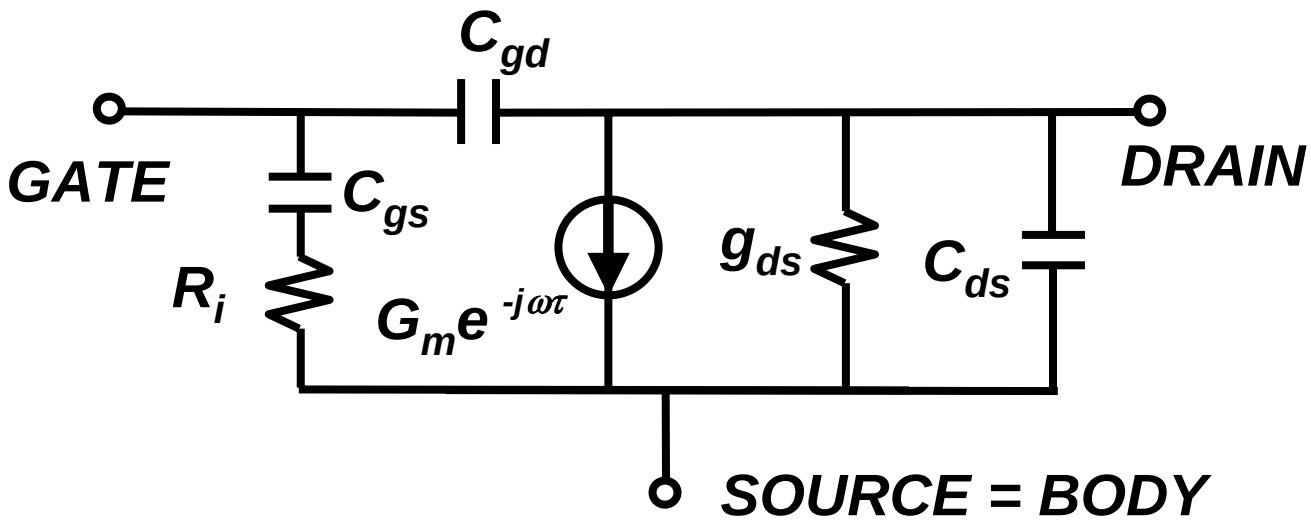
CMOS as RF technology

- Continuous down scaling of CMOS active devices
  - f_T and f_{max} above 20 GHz
  - *Excellent potential for 2 ~ 5 GHz wireless communication*
- Continuous up scaling of CMOS interconnection technology
  - *Few nH inductors with Q>10 and MIM capacitors with small parasitics*
- Possibility of integrating RF, analog, and digital circuits in a single chip : *Single chip radio.*

- But accurate and reliable CMOS RF modeling and characterization methods are not available yet, which has utmost importance to be competitive in RF chip design.

Review of III-V MESFET/HFET works - I

- Mostly based on Small Signal Models



- 7 parameters, leaving one degree of freedom for fitting frequency dependent 2-port s-parameter measured at particular bias point.
- Metal gate (No Rg!) on semi-insulating substrate (No loss in Cds!)
- Reciprocal Cgs and Cgd which are not correct for active devices!
- Ri is needed to consider input loss!

Review of III-V MESFET/HFET works - II

- Large signal models

- Analytical models: do not have enough accuracy mainly because of bad repeatability of III-V transistor characteristics.
- Table models constructed by numerical integration of small signal measured data: technology independent, but not physical, nor scalable.

Why large signal model?

- Large signal I(V) and Q(V) are still the best choice as the state variables describing multi-terminal MOSFET in quasi-static approximation for RF ECAD.

- Here I and Q are uniquely determined as functions of node voltages. Thus we do not have to worry about such problems as charge and current conservations.

Why small-signal equivalent circuit compatible with large signal model?

- ***Small signal s-parameter measurement*** is the only practical characterization method at high frequencies.
- Thus we should be able to construct small signal equivalent circuits compatible with their large signal model. This not only is mathematically and physically correct, but is very important for circuit simulation accuracy and speed.
- For example, Cgs/Cgd and Gm/Gds at each bias point cannot be chosen independently to conserve charge and current, respectively. Moreover, each capacitor is not bilateral, i.e., Cgd and Cdg are different.

Root's proposal for charge non-conservation problem

- Circuit simulation based on nonlinear large signal transient analysis (TA) does not agree with that on small signal linear AC model derived from it, because large and small signal models are inconsistent!

- One cannot construct large signal model from integrating (wrong) small signal model!

- Need to consider charge conservation independent of (Vgs, Vds) bias trajectory.

- Voltage controlled charge source (VCQS) should be used instead of capacitance to calculate displacement current!

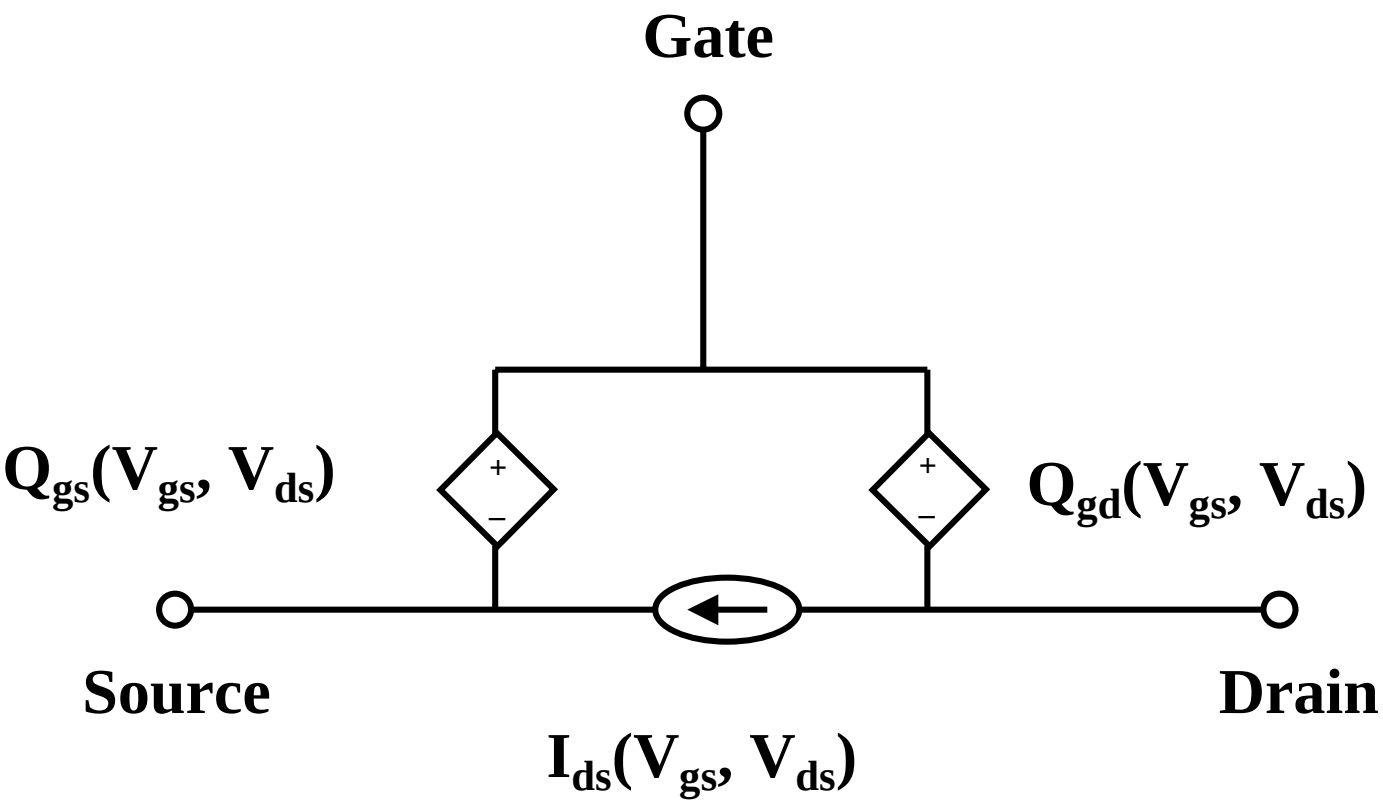
- D.E. Root, "Charge Based Partially Distributed MESFET Model for SPICE", (invited paper) Modeling High-Speed GaAs Devices and Nonlinear CAD Workshop, Palo Alto, CA, Feb. 1987.

- Note charge non-conserving problem was first addressed by Ward and Dutton in 1978 and then by Ping Yang et al. in 1983 for low frequency MOSFET circuits.

Root's proposal (continued)

- Same is true for drain current which should be voltage path independent !

Root's intrinsic large signal FET model



Root's approach to consider charge conservation

$$Q_{GD} = Q_{GD}(V_{GS}, V_{DS})$$

$$\frac{dQ_{GD}}{dt} = \frac{\partial Q_{GD}}{\partial V_{GS}} \cdot \frac{dV_{GS}}{dt} + \frac{\partial Q_{GD}}{\partial V_{DS}} \cdot \frac{dV_{DS}}{dt}$$

$$= C_{DG} \frac{dV_{GS}}{dt} - C_{GD} \frac{dV_{DS}}{dt}$$

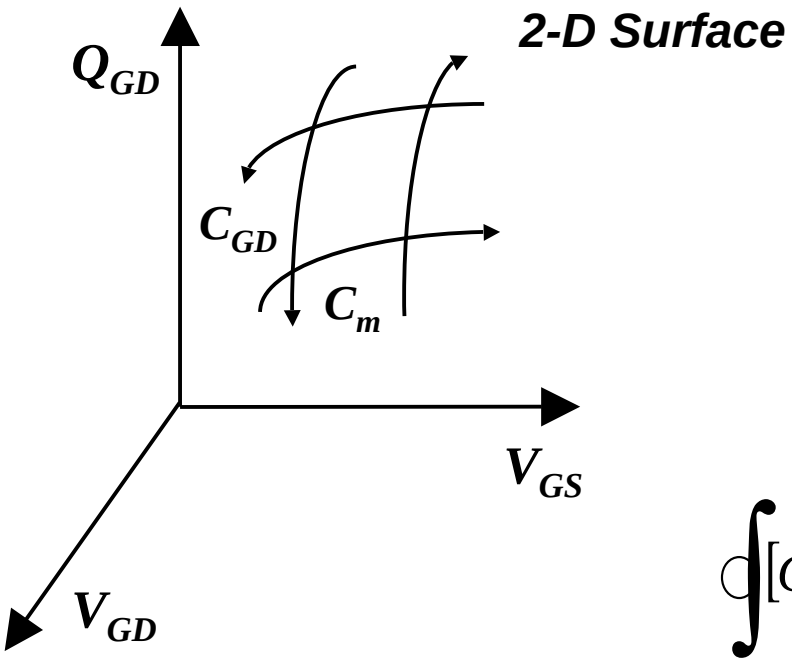
$$= (C_{DG} - C_{GD}) \frac{dV_{GS}}{dt} + C_{GD} \frac{dV_{GD}}{dt}$$

$$= C_m \frac{dV_{GS}}{dt} + C_{GD} \frac{dV_{GD}}{dt}$$

C_m : transcapacitance

- reactive analogue of the transconductance
- needed for charge conservation

Root's approach to consider charge conservation

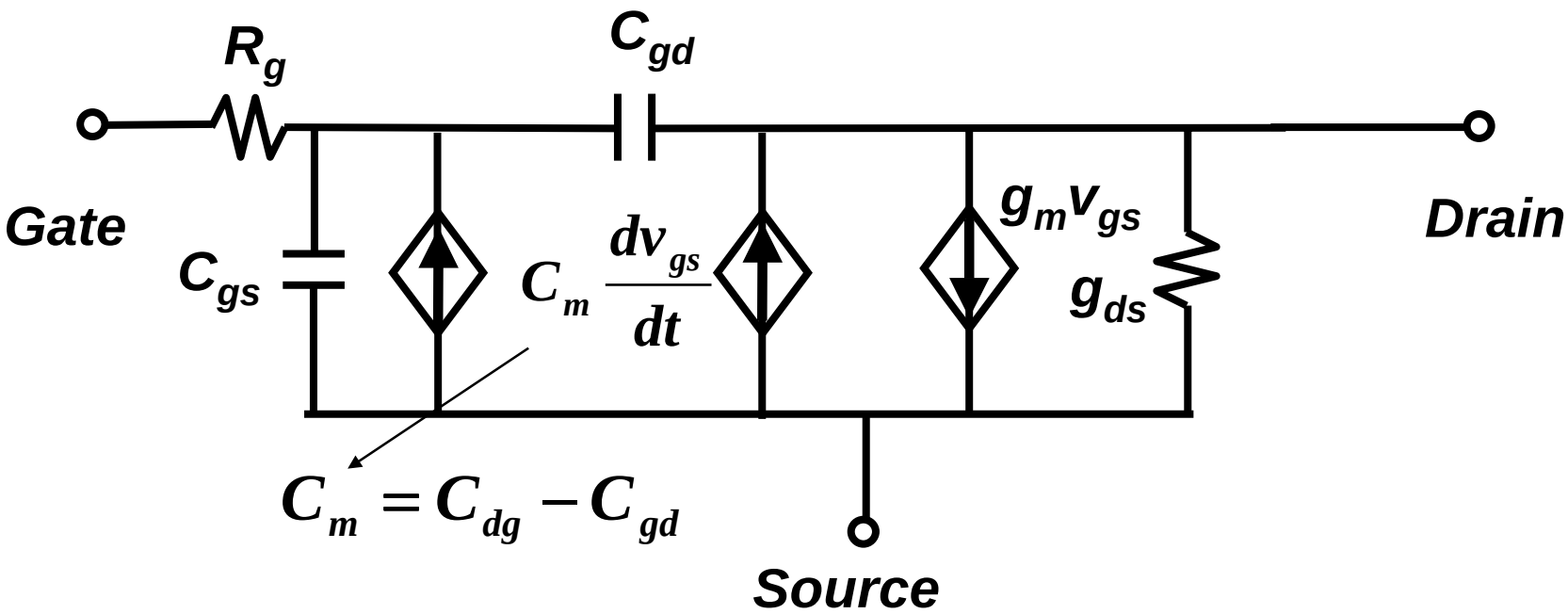


- Q_{GD}, C_m, C_{GD} depend only on the controlling voltages.
- C_m and C_{GD} are not independent functions to uniquely define Q_{GD}.
- Bias path independence

$$\oint [C_{GD}(V_{GD}, V_{GS})dV_{GD} + C_m(V_{GD}, V_{GS})dV_{GS}] = 0$$

$$\Rightarrow \frac{\partial C_{GD}}{\partial V_{GS}} = \frac{\partial C_m}{\partial V_{GD}}$$

Root's intrinsic small signal FET model



Required Accuracy for RF transistor models

- Required accuracy for RF circuit simulation

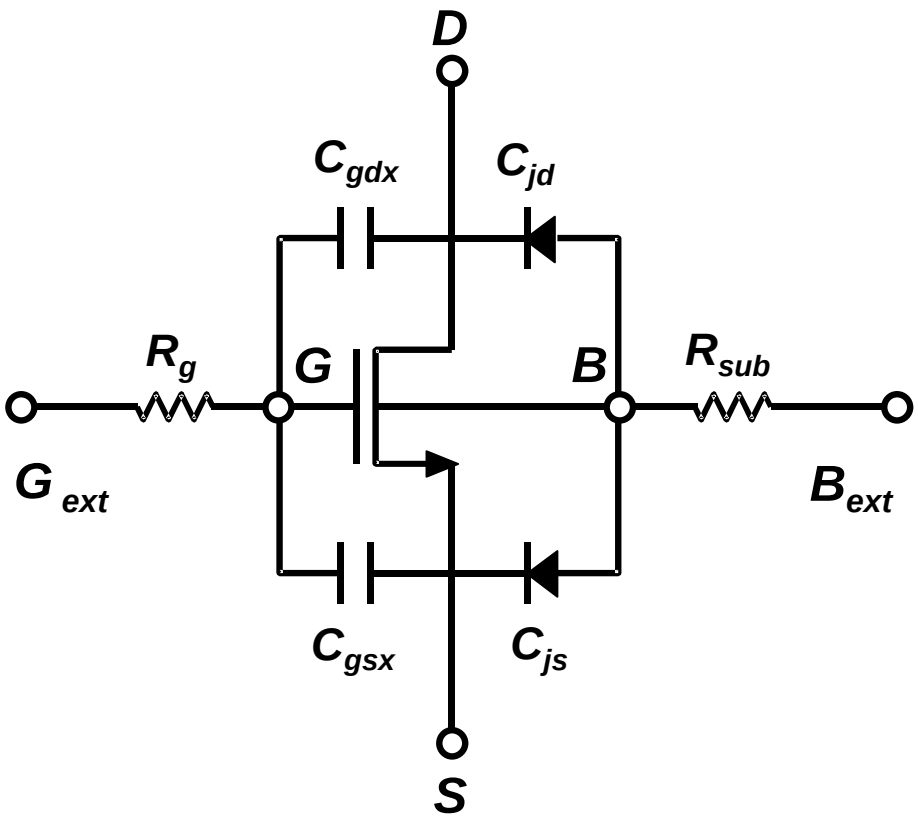
LNA	***Mixer***	***Oscillator***	***Power Amp.***
• Bias (*I*) • Gain (*I'*, *C*) • Linearity (*I''*, *I'''*, *C'*) • Thermal noise	• Bias (*I*) • Conversion gain (*I''*, *C*) • Linearity (*I''''*, *C'*)	• Bias (*I*) • Oscillation frequency (*I'*,*C*) • Oscillation amplitude (*I''*, *I'''*, *C'*) • Phase noise (*1/f* noise)	• Bias (*I*) • Gain (*I'*, *C*) • Linearity (*I''*, *I'''*, *C'*)

Much higher order continuity is desired for accuracy/computational efficiency for circuit simulation using Harmonic Balance Technique!

KAIST approach for RF CMOS modeling

- Based on existing popularly used large signal I-V and Q-V models, such as BSIM, to take care of conservation problem properly,
- Construct correct small signal equivalent circuit model consistent with large signal model as Root proposed,
- Extract parameters from s-parameter measurement at each bias point in an easy and straightforward way using no more than linear regression,
- Optimize large signal model parameters to fit for the entire bias points.

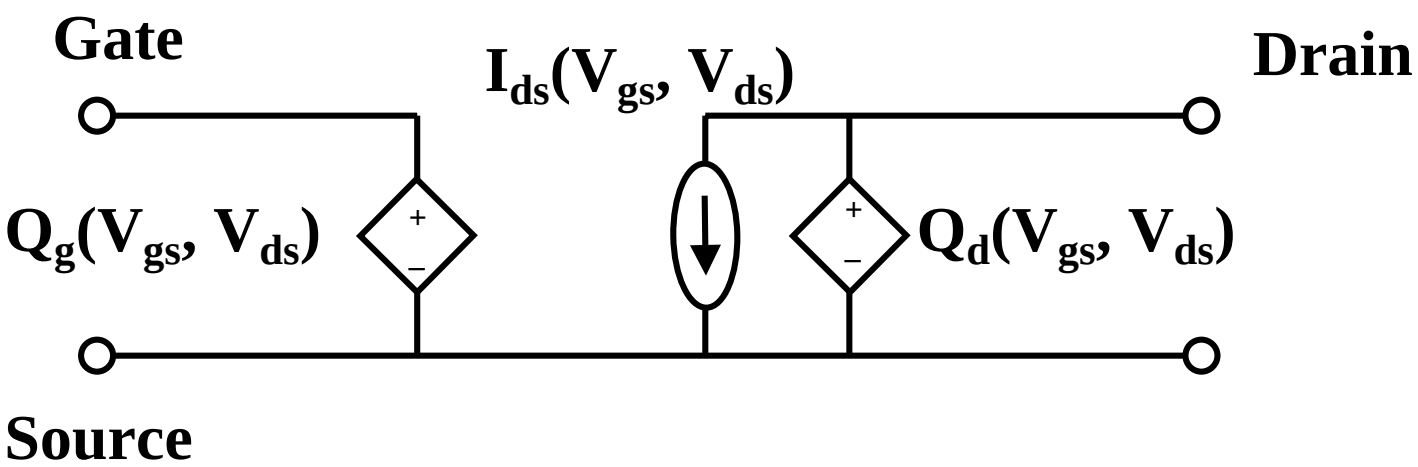
Large Signal RF CMOS Macro Model



- Gate resistance : R_g (gate electrode resistance + channel resistance, R_i)
- Substrate resistance : R_{sub}*
- Large signal I-V and Q-V models for intrinsic MOS
- Parasitic capacitances: C_{gsx} and C_{gdx}.

* W. Liu, R. Gharpurey, M. C. Chang, U.Erdogan, R. Aggarwal, and J. P. Mattia, "R.F. MOSFET modeling accounting for distributed substrate and channel resistances with emphasis on the BSIM3v3 SPICE model," *Int. Electron Devices Meeting*, pp. 309–312, 1997.

KAIST Large Signal intrinsic common source 3- terminal MOS RF model



Calculation of displacement current for intrinsic MOSFET

– Small signal charging currents

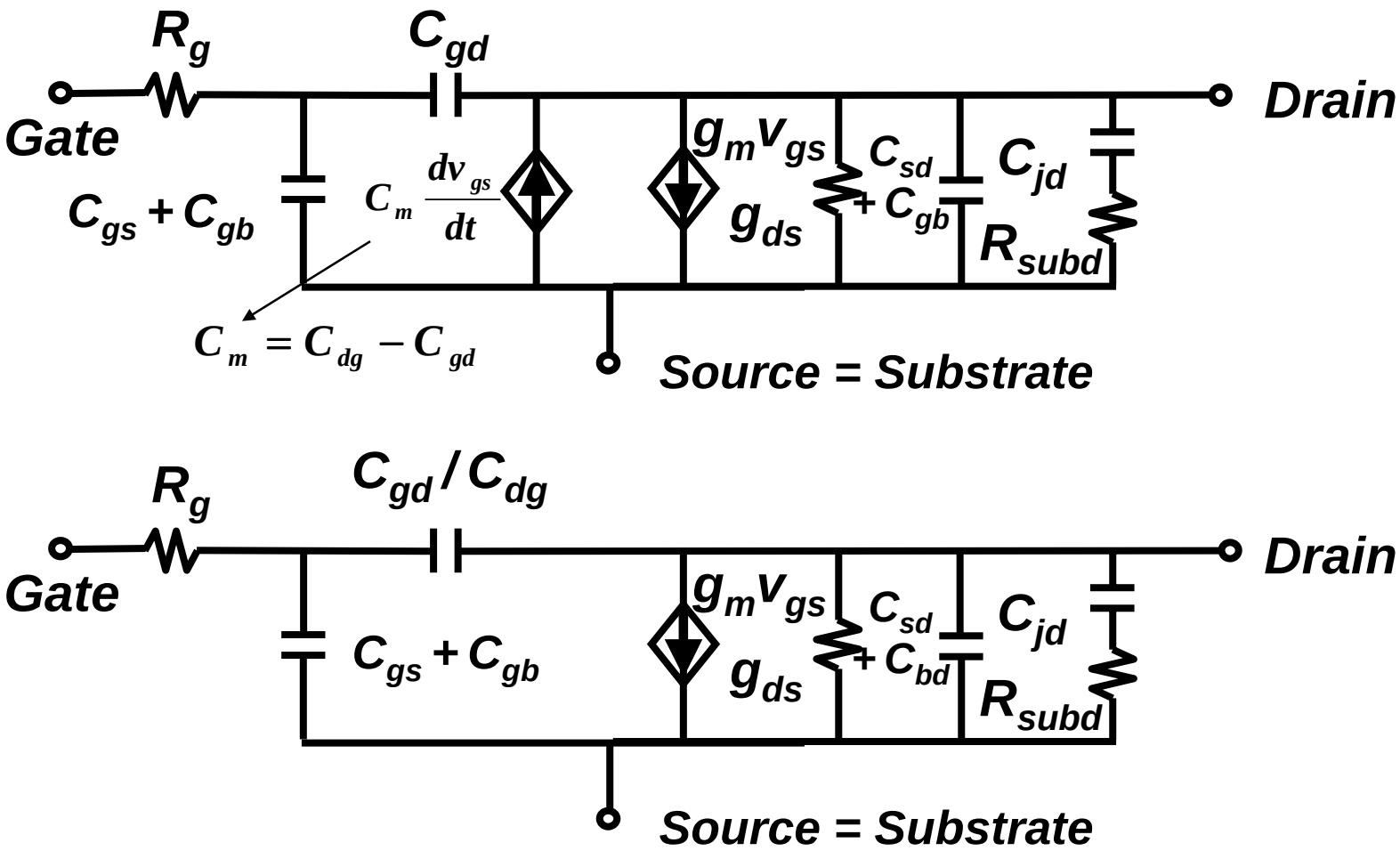
$$i_g(t) = C_{gg}\frac{dv_{gs}}{dt} - C_{gd}\frac{dv_{ds}}{dt} = (C_{gs} + C_{gb} + C_{gd})\frac{dv_{gs}}{dt} - C_{gd}\frac{dv_{ds}}{dt}$$

$$i_d(t) = -C_{dg}\frac{dv_{gs}}{dt} + C_{dd}\frac{dv_{ds}}{dt} = -C_{dg}\frac{dv_{gs}}{dt} + (C_{gd} + C_{sd} + C_{bd})\frac{dv_{ds}}{dt}$$

– Non-reciprocal capacitance
  - C_{gd} : effect of the drain voltage on the gate charge
  - C_{dg} : effect of the gate voltage on the drain charge

– In general, $\boldsymbol{C_{gd} \neq C_{dg}}$

KAIST small signal RF CMOS model



Parameter extraction method

- Construct small signal equivalent circuit model compatible with large signal one
- Convert measured s-parameters into y-parameters
- Extract small signal equivalent parameters from fitting measured and modeled y-parameters
- Avoid complex curve fitting or optimization
- Very simple and straightforward method such as either direct extraction or linear regression at most

Parameter Extraction Method

Assuming $\omega^2 C_{gg}{}^2 R_g{}^2 \ll 1$,

$$Y_{11} \approx \omega^2 C_{gg}{}^2 R_g + j\omega C_{gg}$$

$$Y_{21} \approx g_m - \omega^2 C_{dg} C_{gg} R_g - j\omega C_{dg} - j\omega g_m R_g C_{gg}$$

$$Y_{12} \approx -\omega^2 C_{gd} C_{gg} R_g - j\omega C_{gd}$$

$$Y_{22} \approx g_{ds} + \frac{\omega^2 C_{jd}{}^2 R_{subd}}{1+\omega^2 C_{jd}{}^2 R_{subd}{}^2} + \omega^2 C_{dg} C_{gd} R_g + \omega^2 g_m R_g^2 C_{gd} C_{gg}$$

$$+ j\frac{\omega C_{jd}}{1+\omega^2 C_{jd}{}^2 R_{subd}{}^2} + j\omega(C_{sd}+C_{bd}) + j\omega C_{gd} + j\omega g_m C_{gd} R_g - j\omega^3 C_{gd} C_{dg} C_{gg} R_g^2$$

Parameter extraction method (continued)

$$C_{gd} = -\frac{\mathrm{Im}[Y_{12}]}{\omega}$$

$$R_g = \frac{\mathrm{Re}[Y_{11}]}{(\mathrm{Im}[Y_{11}])^2}$$

$$g_m = \mathrm{Re}[Y_{21}]\Big|_{\omega^2=0}$$

$$C_{dg} = -\frac{\mathrm{Im}[Y_{21}]}{\omega} - g_m R_g C_{gg}$$

$$C_{gg} = \frac{\mathrm{Im}[Y_{11}]}{\omega}$$

$$g_{ds} = \mathrm{Re}[Y_{22}]\Big|_{\omega^2=0}$$

Parameter Extraction Method (continued)

$$Y_{sub} = Y_{22} - g_{ds} - \omega^2 C_{gd} C_{dg} R_g$$
$$- \omega^2 g_m R_g{}^2 C_{gd} C_{gg} - j\omega(C_{sd} + C_{bd}) - j\omega C_{gd}$$
$$- j\omega g_m R_g C_{gd}$$

$$= \frac{\omega^2 C_{jd}{}^2 R_{subd}}{1 + \omega^2 C_{jd}{}^2 R_{subd}{}^2} + \frac{j\omega C_{jd}}{1 + \omega^2 C_{jd}{}^2 R_{subd}{}^2}$$

Parameter extraction method (continued)

- R_{sub} is from slope from ω^2 / Re(Y_{sub}) vs. ω^2 plot

$$\frac{\omega^2}{\mathrm{Re}(Y_{sub})} = \omega^2 R_{sub} + \frac{1}{C_{jd}^2 R_{sub}}$$

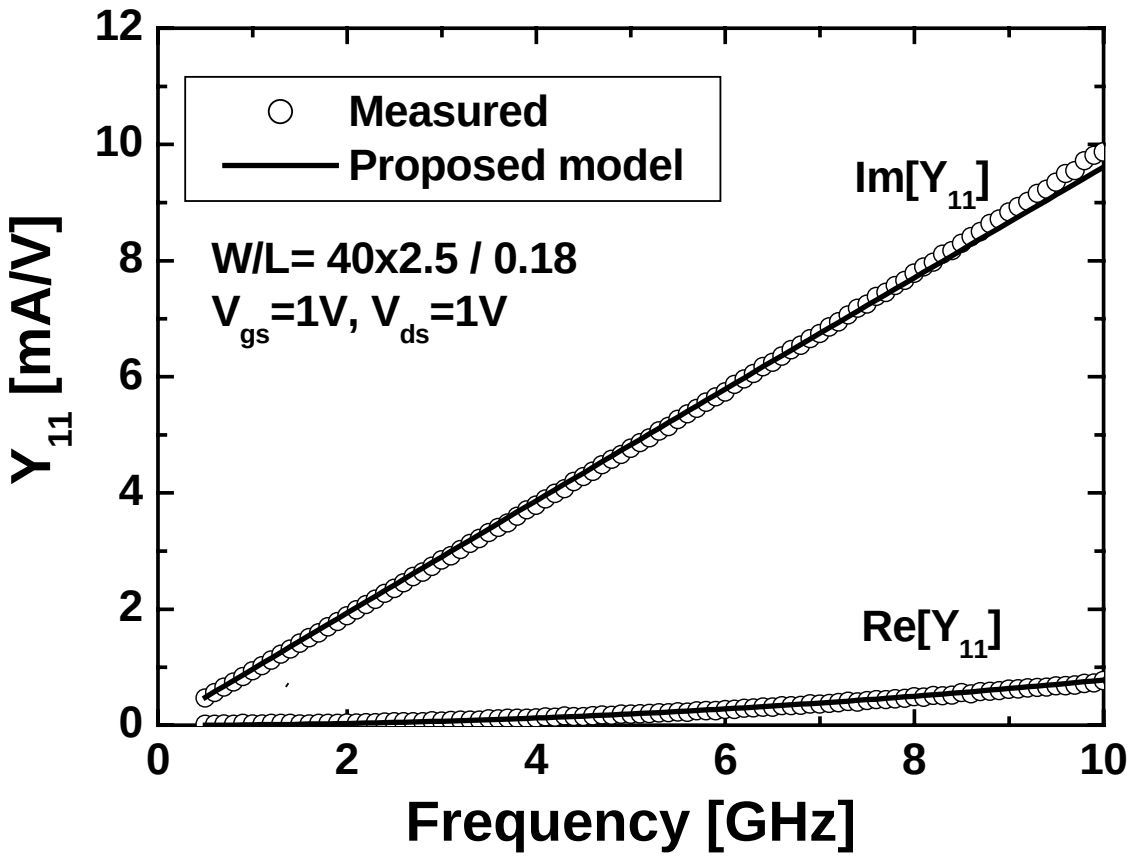
$$C_{jd} = \left(\frac{\omega^2 R_{sub}}{\mathrm{Re}(Y_{sub})} - \omega^2 R_{sub}^2 \right)$$

- C_{sd}: from Im(Y_{22}) after de-embedding others

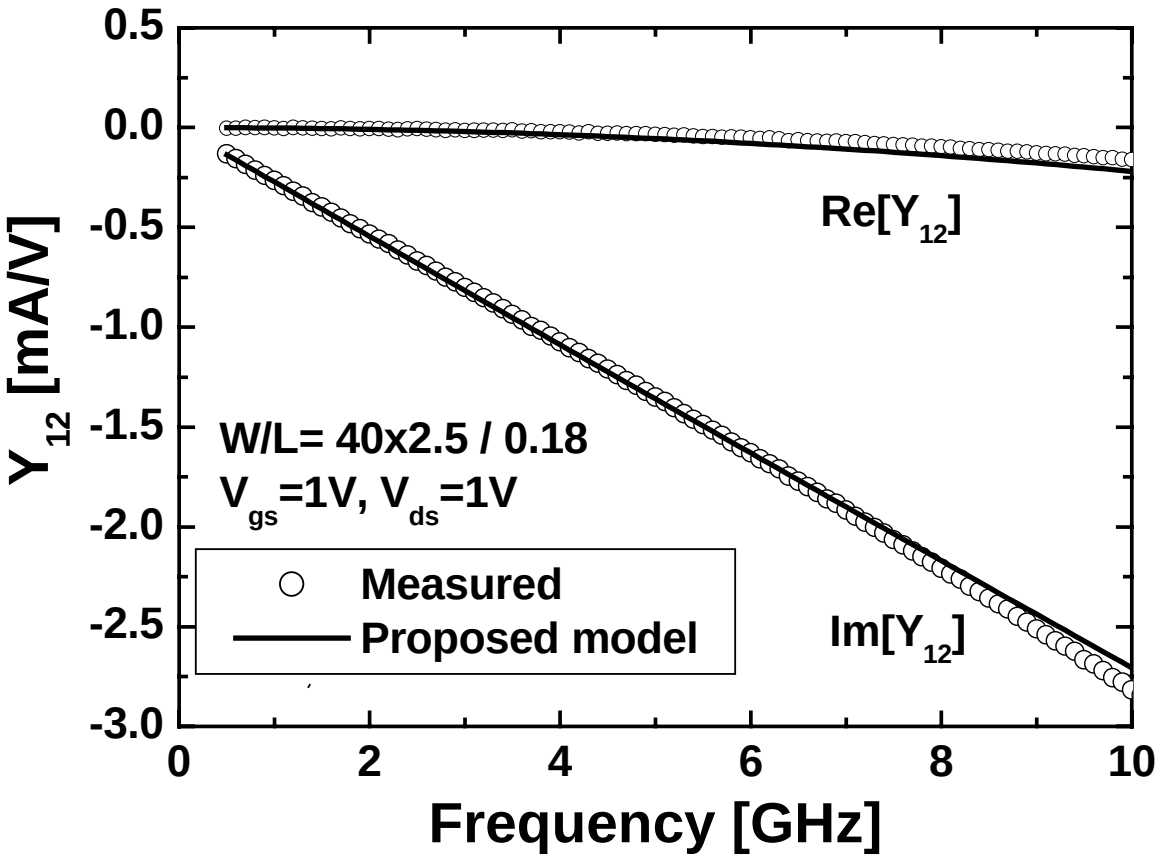
Extraction examples

- Multi-fingered 0.18-μm n-MOSFET
  - Total width = 100 μm and 25 μm
  - Number of fingers = 40 and 10
  - V_{th}= 0.45 V
- *S*-parameter measurement
  - Common source-substrate configuration
  - On-wafer RF probing and HP 8510C
- Two-step (open and short) de-embedding
- $\omega^2 C_{gg}{}^2 R_g{}^2 = 0.065 << 1$ @ 10 GHz

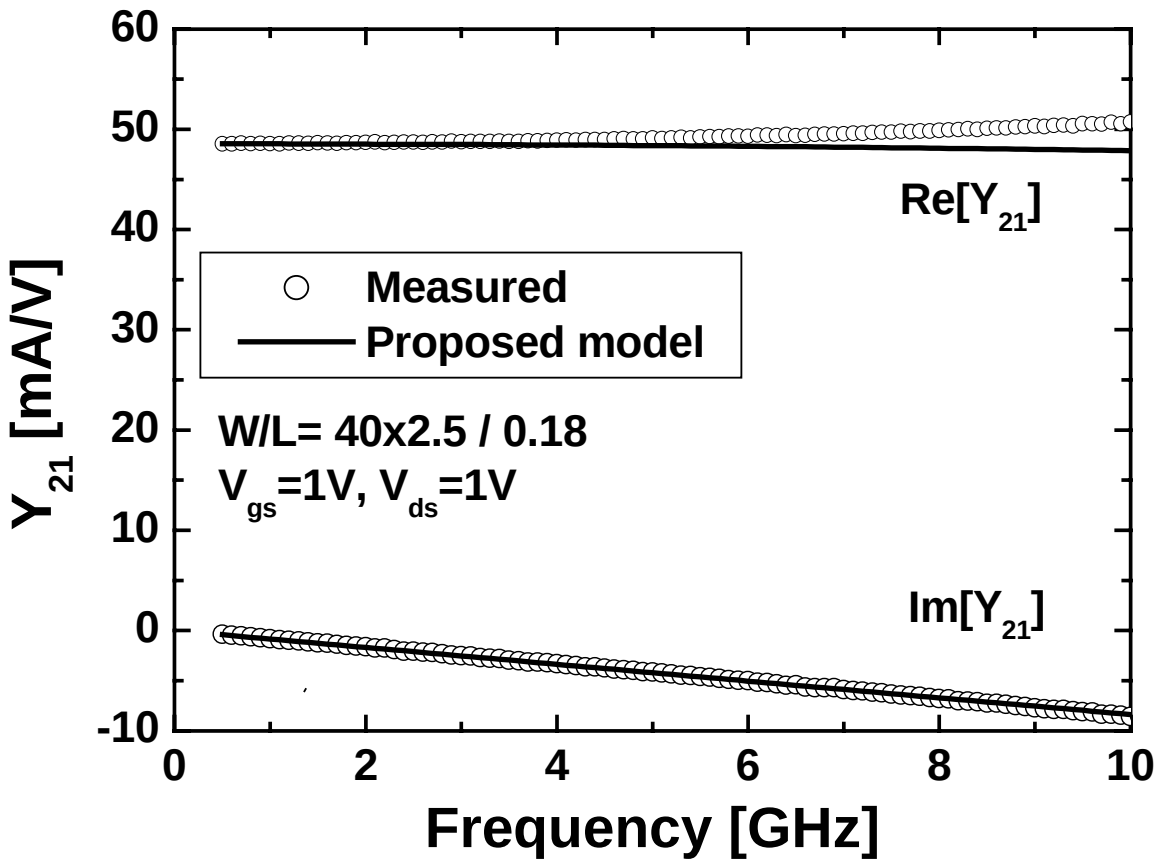
Model Verification, Y_{11}



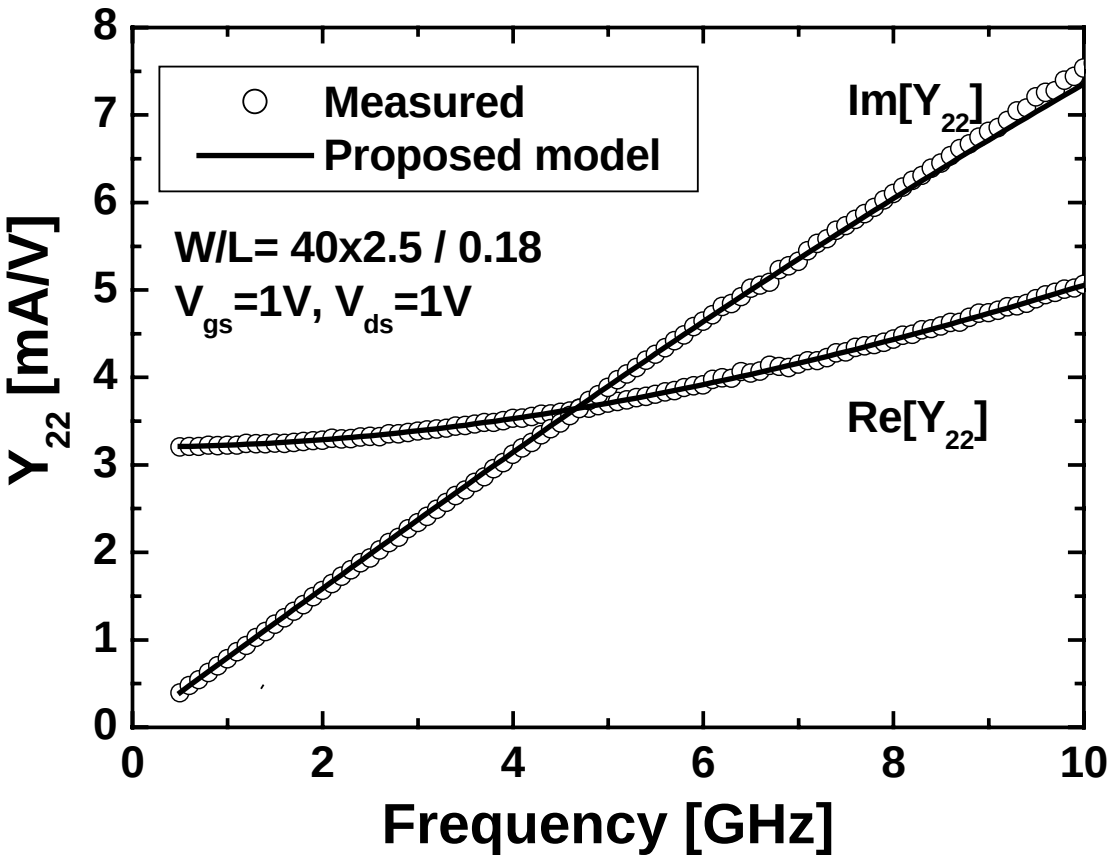
Model Verification, Y_{12}



Model Verification, Y_{21}



Model Verification, Y_{22}

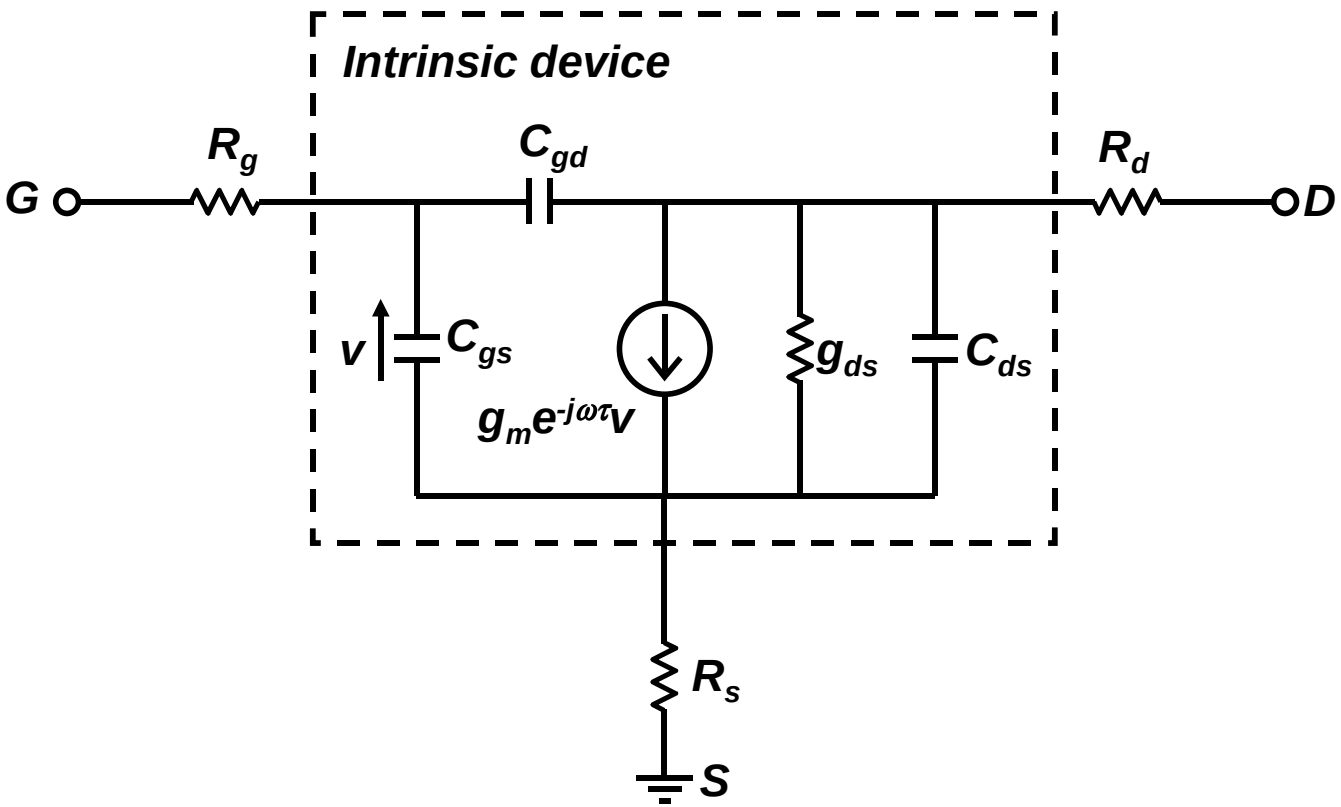


Model Verification

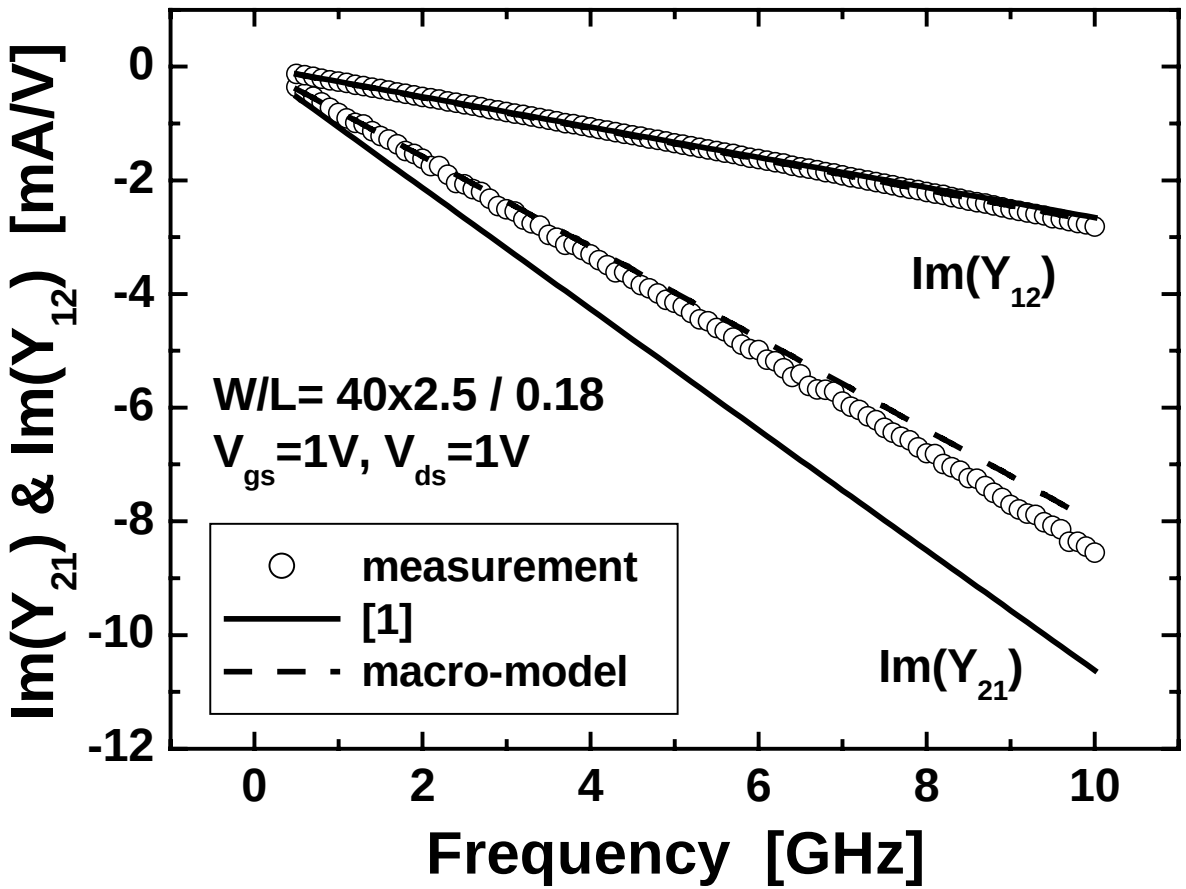
- Accurate without any further optimization after extraction.
- Total root-mean-square error = 1.8 %
- Easy checking of confidence level for extraction results
- Straightforward and fast enough for bias dependence measurement for large signal construction and for statistical yield analysis in manufacturing environment

Comparison with other model [1]

- Comparison with conventional small signal model



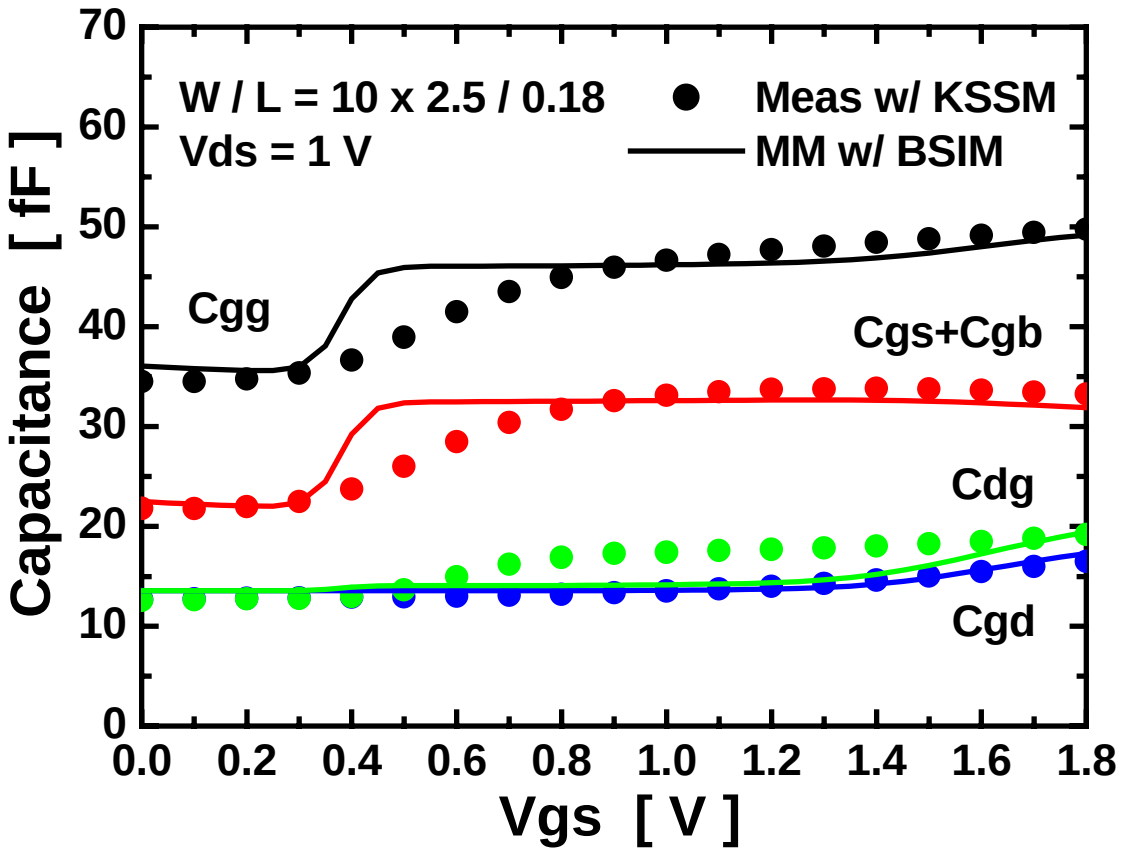
Comparison with conventional small signal model



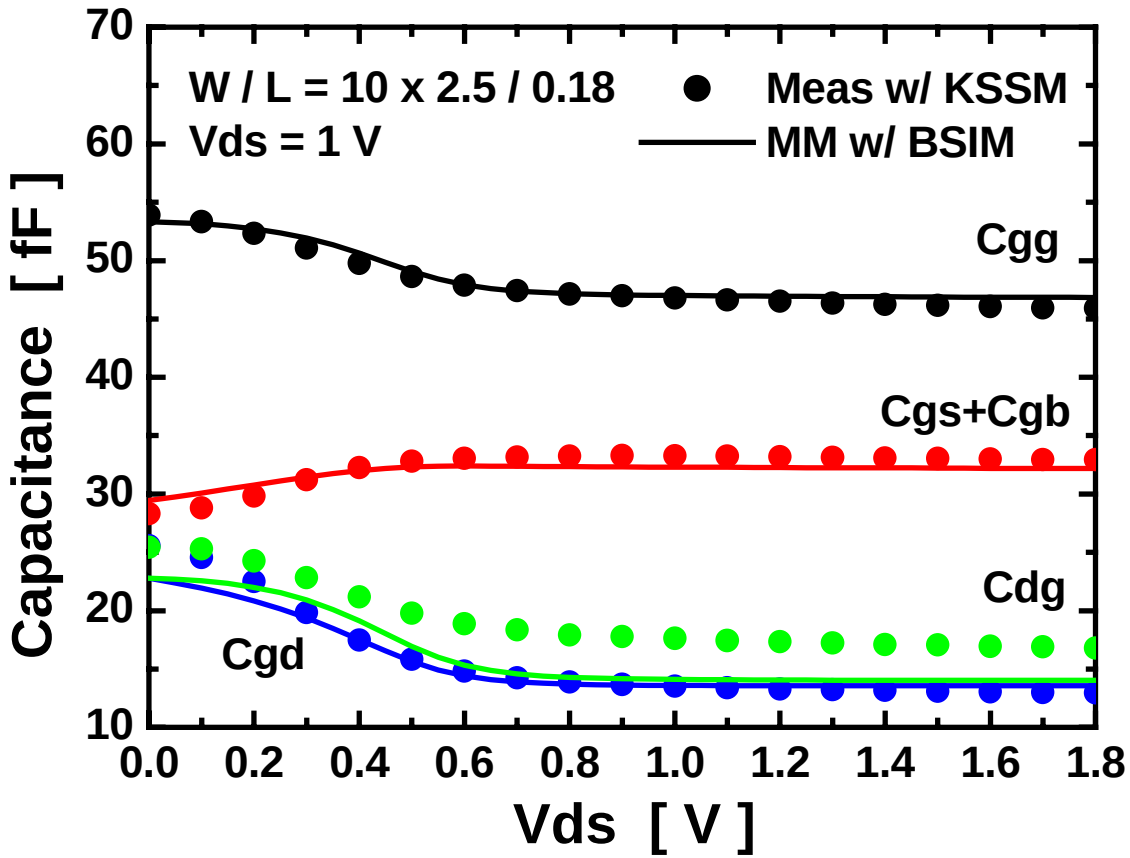
Comparison with conventional small signal model

- The conventional model is very simple but one cannot fit Y_{12} and Y_{21} simultaneously.
- Non-reciprocity in C_{gd} and C_{dg} are necessary to fit these simultaneously.
- For the macro-model, the reciprocal capacitance C_{gdx} cannot solve this non-reciprocity.

Bias Dependence of the Extracted C-V Parameters: V_{gs} dependence



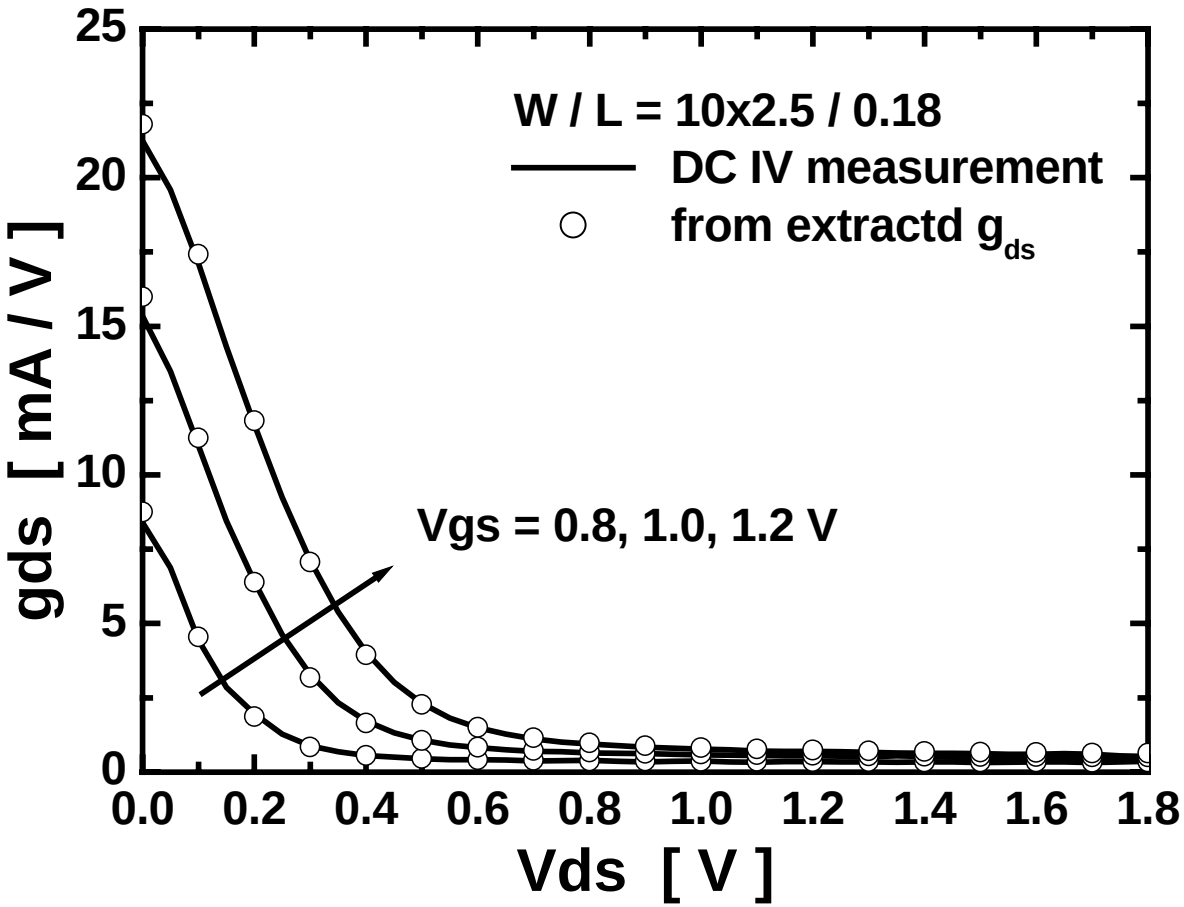
Bias dependence of the extracted C-V parameters: V_{ds} dependence



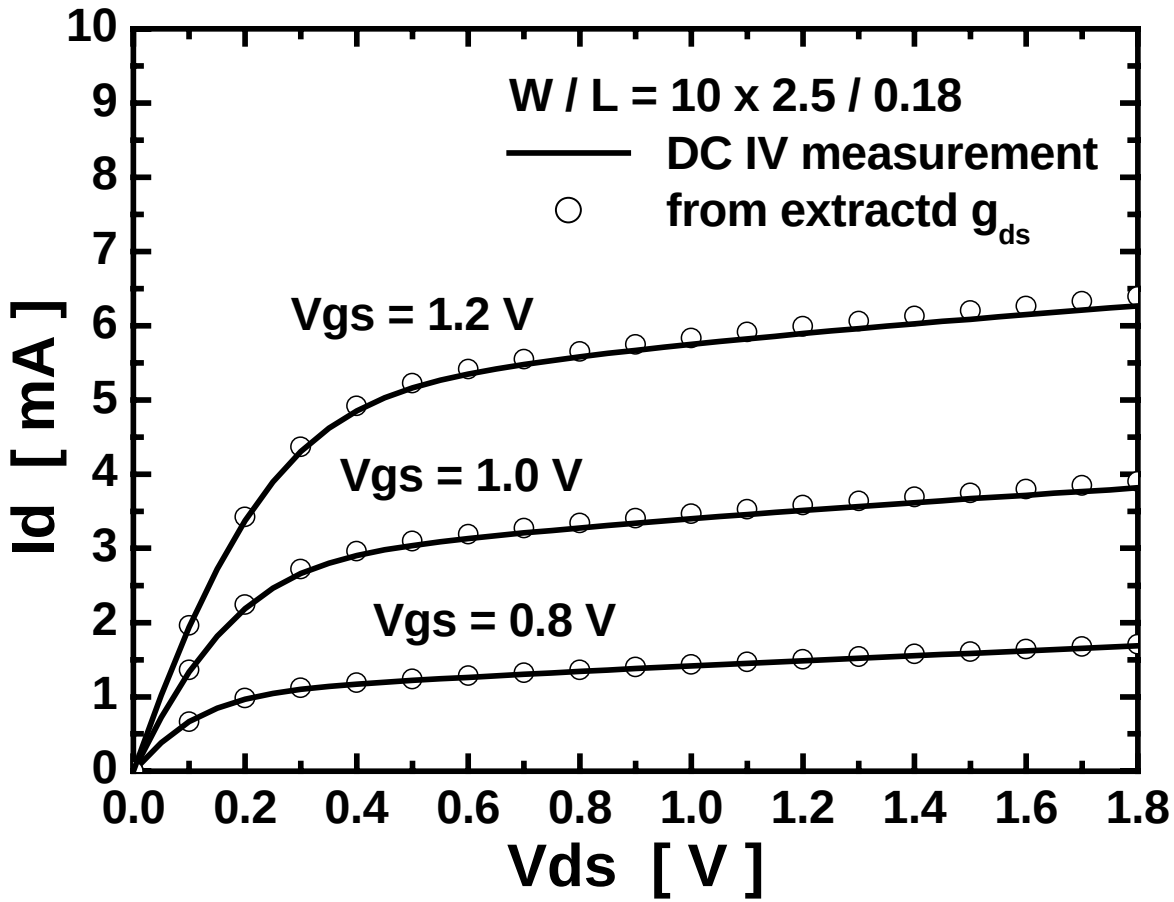
Bias Dependence of the Extracted Parameters

- *C-V* behavior is what we expect from MOSFET device physics.
- C_{dg} is larger than C_{gd}, demonstrating the necessity of non-reciprocity.
- Charge conservation is important not only for the simulation accuracy and efficiency but also for the compatibility with large-signal *Q-V* models.

G_{ds} between DC and RF measurement



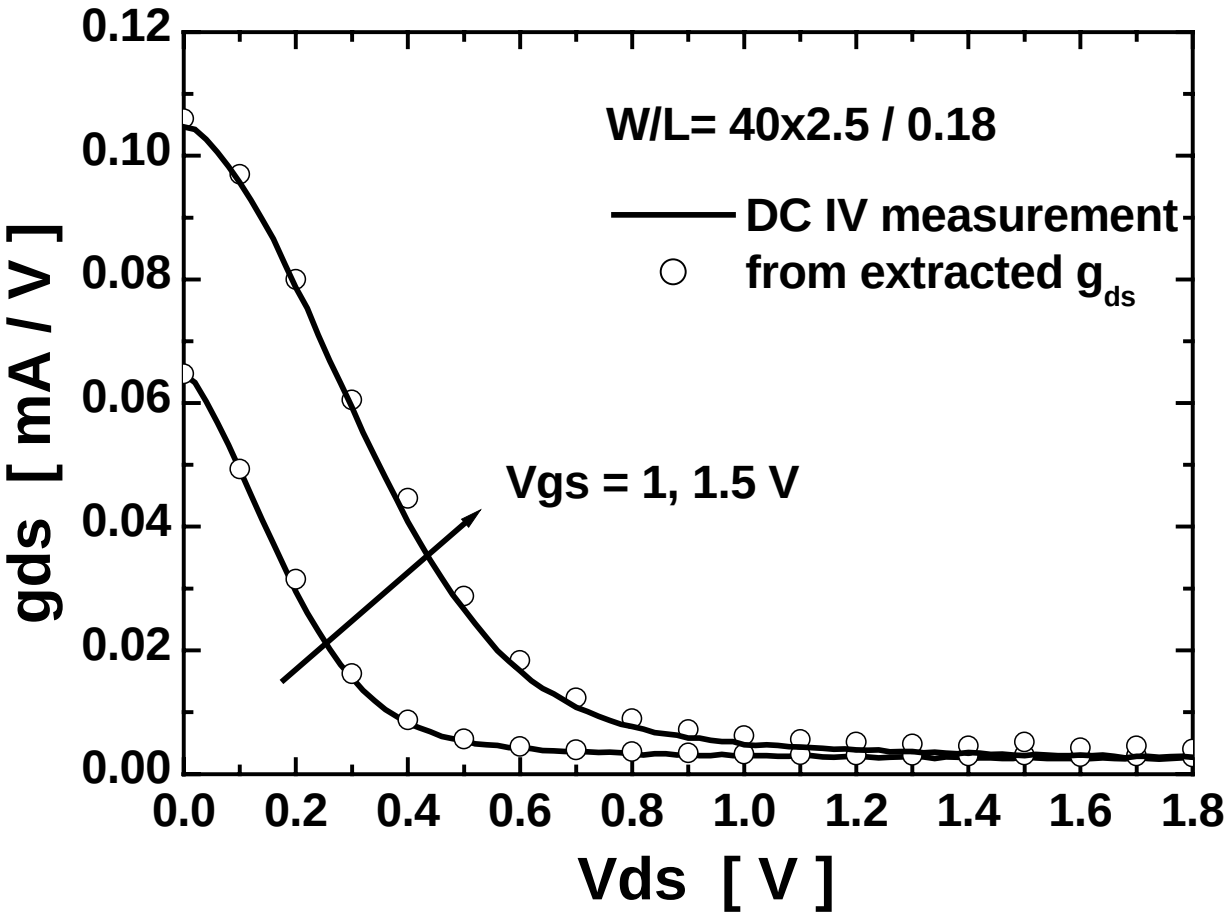
I_d-V_{ds} construction from G_{ds} integration



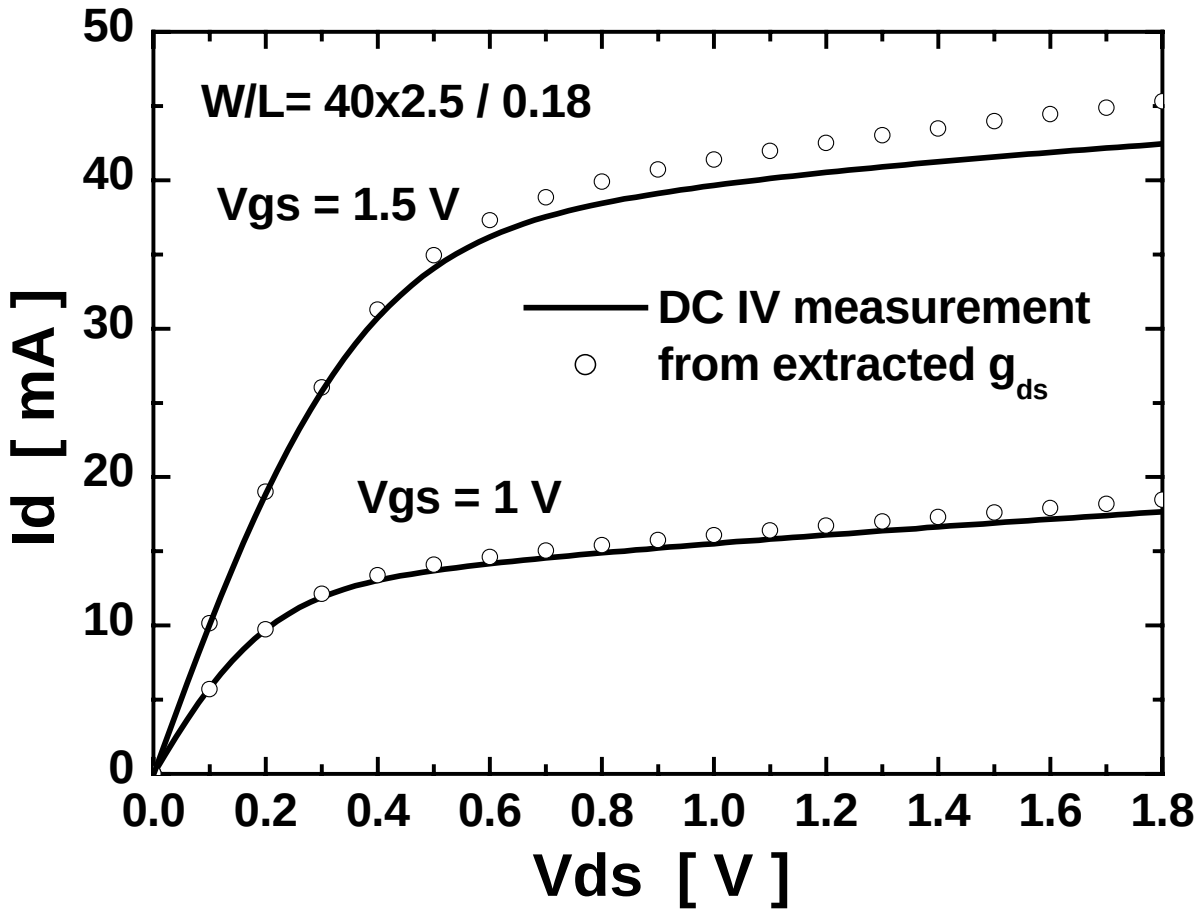
Conclusions

- Correct construction of small signal model compatible with large signal one is very important not only for the accuracy but for the efficiency of circuit simulation.
- Simple and straightforward parameter extraction method using no more than linear regression, which is important for computerized data acquisition, has been demonstrated.
- Construction methods of large signal I-V and Q-V models from small ones have been demonstrated.
- One large-signal I-V model is found to be enough for DC, low-frequency analog, as well as RF circuit simulation.
- Needs more elaborate short channel Q-V model.

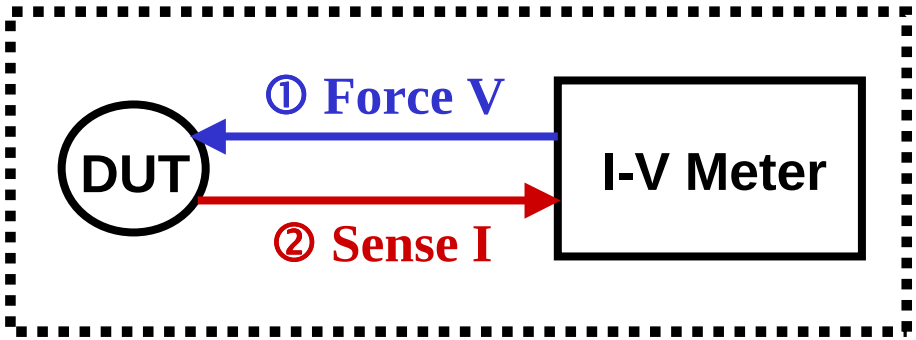
G_{ds} inconsistency problem for large FET

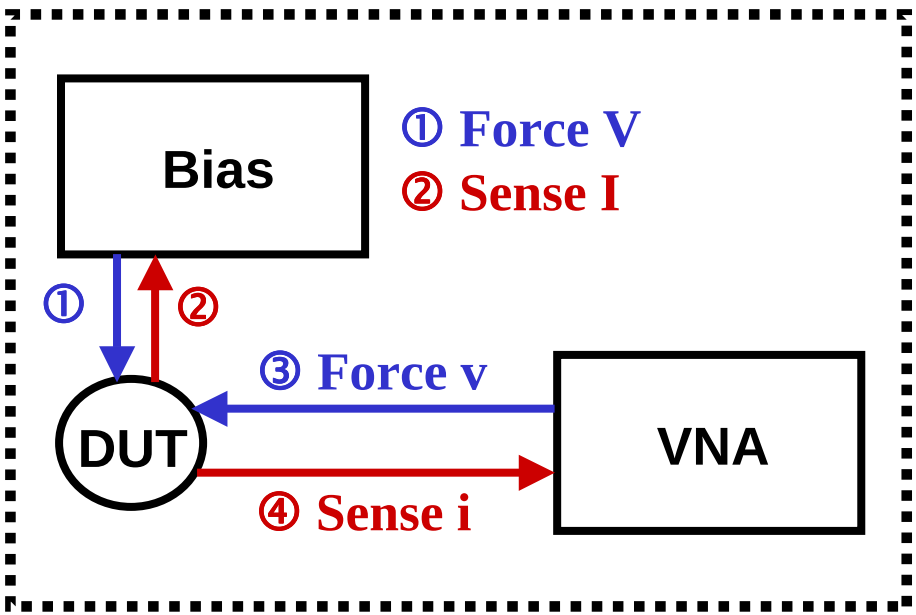


I_d-V_{ds} inconsistency for large FET



Reason of Discrepancy





DC I-V Measurement:

① Voltage drop due to series R's

② g_{ds} (I_{ds}) degradation

$$\frac{1}{g_{ds,meas}} = \frac{1}{g_{ds}(V_{gs}', V_{ds}')} + R_d + R_s + \frac{g_m(V_{gs}', V_{ds}')}{g_{ds}(V_{gs}', V_{ds}')} R_s$$

S-Parameter Measurement:

①② I,V degradation due to Series R's

③④ Deembedded (parasitic-free) path

$$\frac{1}{g_{ds,meas}} = \frac{1}{g_{ds}(V_{gs}', V_{ds}')}$$

Reason for inconsistency-simulation