A Highly Linear Wideband CMOS Low-Noise Amplifier Based on Current Amplification for Digital TV Tuner Applications

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***Abstract*—A differential wideband low-noise amplifier (LNA) based on the current amplification scheme is presented for digital TV tuners. In order to highly improve the linearity and exploit the noise cancellation, a common-gate stage with positive current feedback is integrated in parallel with a common-source stage using the current mirror amplifier. The proposed 0.18-μm CMOS LNA exhibits a power gain of 20.5 dB, an IIP3 of 2.7 dBm, an IIP2 of 43 dBm, and an average noise figure of 3.3 dB with 32.4 mW power consumption at a 1.8-V power supply and 0.12 mm^2 area.**

***Index Terms*—Common-gate (CG) amplifier, current amplification, digital television (TV), low-noise amplifier (LNA), noise-canceling, positive current feedback, wideband.**

I. Introduction

THE terrestrial digital television (TV) systems such as advanced television systems committee-terrestrial (ATSC-T) used in North America and digital video broadcasting- terrestrial (DVB-T) used in Europe have many channels covering from 48 to 860 MHz [1]. A wideband low-noise amplifier (LNA) for the TV tuner to receive these TV signals has many challenging issues: broadband impedance matching, low noise figure (NF), high linearity, and wideband gain flatness. A common-gate (CG) LNA has been widely used for broadband input matching, but it faces a severe trade-off between NF and input impedance matching. It is difficult for the CG LNA to achieve NF lower than 4 dB with good input impedance matching. Recently, the feed-forward noise-canceling technique has been reported to separate noise and impedance matching process in the CG LNA [2], [3]. However, these LNAs do not have differential topology and thus suffer from a poor second-order input-referred intercept point (IIP2). Since many channel signals received into a wideband TV tuner can produce a large number of second-order and third-order in-band distortion products, a fully differential LNA with high linearity is preferable.

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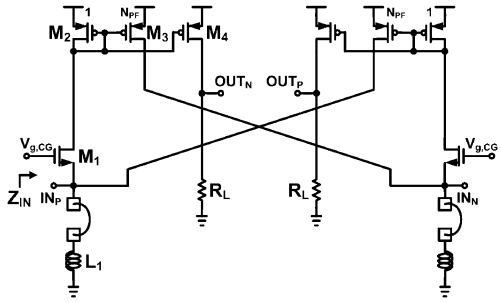

Fig. 1. Differential common-gate LNA with the positive current feedback based on the current amplification scheme.

In this letter, a wideband CMOS differential LNA based on the current amplification scheme, which reduces the transconductance nonlinearity, is proposed for high linearity using a 0.18-μm CMOS process. Moreover, in order to achieve both low NF and high linearity simultaneously, the noise-canceling technique based on the current amplifier is described.

II. Wideband LNA With Current Amplification Scheme

A. Common-Gate LNA With Positive Current Feedback

The input transistor transconductance of the traditional CG LNA is mainly determined by the input source impedance for matching. Therefore, the CG LNA suffers from a low gain and its low gain increases the noise contribution of the following stages in the tuner system. To eliminate the correlation between the input impedance and the transconductance of the input transistor in the CG LNA, a positive feedback can be added in parallel with the input of the CG LNA to provide a degree of freedom to optimize the input transistor [4]. However, since the feedback topology reported in [4] needs the voltage-to-current (V-I) conversion at the feedback path, the transconductance nonlinearity appears and thus the linearity is degraded. To overcome this problem, a CG LNA with the positive current feedback based on the current amplification scheme is proposed (Fig. 1). The linearity of the proposed LNA is highly improved by adopting the current amplifiers (M_2, M_3, and M_4), which is highly linear without regard to the bias.

The input impedance of the proposed LNA is given by

$$Z_{\mathrm{IN}} = \frac{1}{g_{m1} \cdot (1 - N_{\mathrm{PF}})} \tag{1}$$

where g_{m1} is the transconductance of M_1, and N_{PF} is the scaling ratio of the two current mirrors, M_2 and M_3. Equation

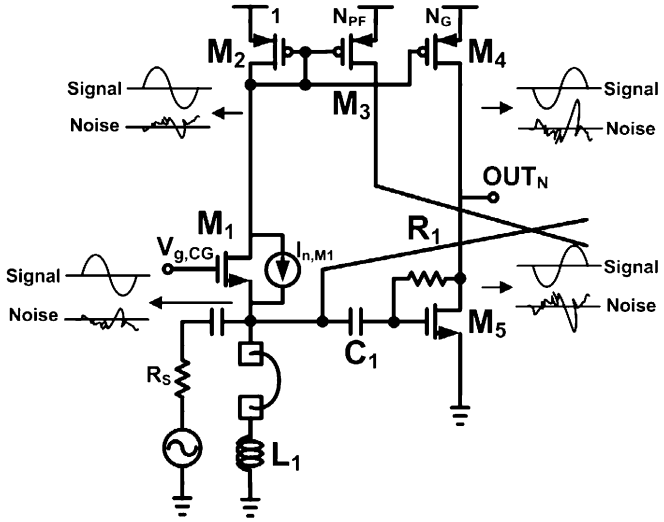

Fig. 2. Noise-canceling mechanism of the proposed LNA.

(1) indicates that the input impedance can be determined by $N_{\rm PF}$ as well as g_{m1}, and thus, the value of g_{m1} can be increased by more than 20 mS for high gain regardless of the input source impedance matching. In Fig. 1, an off-chip RF choke inductor, L_1, is employed to provide the dc current path of M_1 and high impedance at the input node.

B. Noise-Canceling Using Current Amplification Scheme

Fig. 2 illustrates the circuit schematic and noise-canceling mechanism of the proposed LNA using the current amplification scheme. The CG LNA shown in Fig. 1 is integrated in parallel with the common-source (CS) stage by inserting the current amplifier defined with the scaling ratio (N_G) of two current mirrors, M_2 and M_4 (shown in Fig. 2). The current of M_4 is reused for biasing of M_5 without additional current consumption. This LNA based on the linear current amplifier configuration reduces the thermal noise while increasing its linearity by minimizing the number of V-I conversions. The thermal noise current $(\mathrm{I}_{n,M1})$ introduced by M_1 generates two noise voltages that are out-of-phase at the source and drain of M_1. If the gain of the CG stage with current mirror loads (M_2 and M_4) is equal to the gain of the CS stage $(M_5)(g_{m5} = g_{m1}N_G)$, the thermal noise current of M_1 is destructed and at the same time the wanted signal is amplified at the output node, (see Fig. 2). Fig. 3 shows the complete circuit schematic of the proposed LNA. Considering the noise-canceling condition $(g_{m5} = g_{m1}N_G)$ and the thermal noise of the five transistors, $M_1 - M_5$, in Fig. 2, the NF is expressed as

$$\mathrm{NF} \approx 1+\frac{\gamma}{4R_S}\cdot(1+g_{m1}R_S)^2\cdot\left(\frac{1}{g_{m1}N_G}+\frac{2g_{m2}}{g_{m1}^2N_G}\right) \quad (2)$$

where γ is the transistor channel thermal noise factor, R_S is the source impedance, g_{m1} is the transconductance of M_1, g_{m2} is the transconductance of M_2, and N_G is the scaling ratio of the two current mirrors, M_2 and M_4. Note that the noise performance of the LNA can be additionally improved by increasing N_G for obtaining high gain.

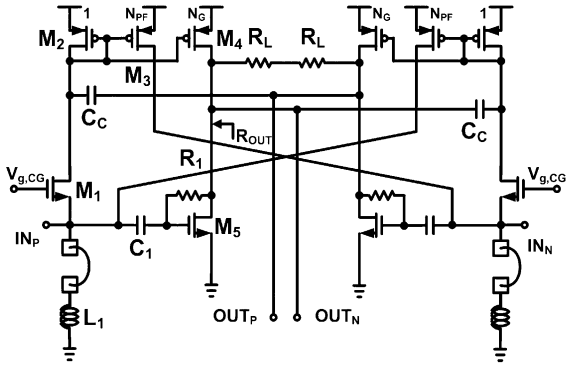

Fig. 3. Complete circuit schematic of the proposed LNA.

The LNA gain in Fig. 3 is presented as the sum of the term by the CG stage with the current mirror load and the term by the CS stage. When the input impedance is matched to the source impedance $(Z_{\rm IN} = R_S)$, the gain is written as

$$G|_{Z_{\rm IN}=R_S} = \frac{1}{2}\cdot(g_{m1}N_G + g_{m5})\cdot(R_L//R_{\rm OUT}) \quad (3)$$

where g_{m5} is the transconductance of M_5, R_L is the load resistor, and $R_{\rm OUT}$ is the output resistance of the LNA except for R_L. $R_{\rm OUT}$ is represented as $r_{O4}//r_{O5}$ (r_{O4} and r_{O5} are the output resistances of M_4 and M_5, respectively). Note that by increasing g_{m1} or N_G, the gain and noise performance of the LNA can be improved without affecting input impedance matching and sacrificing the linearity such as IIP2 and IIP3 [see (2) and (3)].

Typically, the current amplifier has the trade-off between gain and bandwidth [5]. The gain-bandwidth product of simple current amplifier consisting of two current mirrors is given by

$$\mathrm{Gain}\times\mathrm{BW}_{3\mathrm{dB}} \approx \frac{N}{N+1}\cdot\omega_T \approx \omega_T \quad (4)$$

where N is the scaling ratio of two current mirrors, ω_T is the frequency of the unity gain of a current mirror transistor. Under this gain-bandwidth trade-off, the N_G of 3.5 is chosen for the LNA gain of 20.5 dB. In order to further enhance the 3-dB bandwidth without adding an inductor, the LNA exploits the cross-coupling capacitor C_C that neutralizes parasitic capacitances of current mirror loads by connecting two nodes at in-phase, as shown in Fig. 3. By simulation, the 3-dB bandwidth is increased to 600 MHz, but there is a slight limitation of noise canceling at high frequencies above 1 GHz because C_C acts as a short circuit.

III. Experimental Results

The test chip of the LNA has been fabricated in a 0.18-μm RF CMOS process. Fig. 4 shows the chip micro-photograph, which has an active area of only 0.12 mm^2. The output buffer for measurement is integrated into the chip. The chip is measured with the chip-on-board (COB) prototype. Single-to-differential transformation of the input and output port for 50 Ω measurement equipments is done using wideband 1:1 balun of M/A-COM's MABACT0060. Fig. 5 shows the measured and simulated power gain (S_{21}) and noise figure of the LNA after

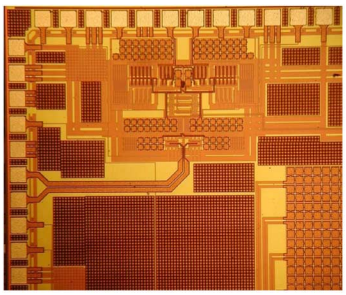

Fig. 4. Chip micro-photograph of the proposed LNA.

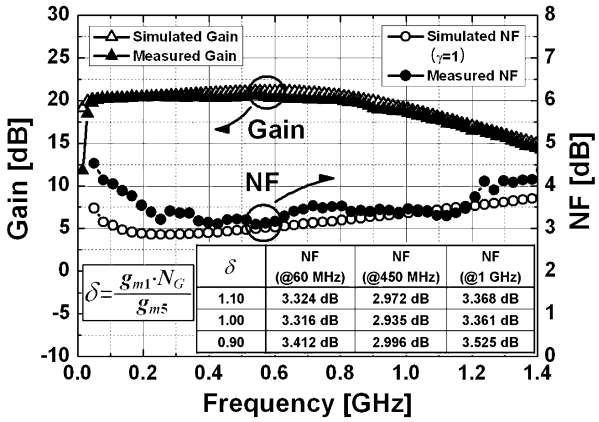

Fig. 5. Measured and simulated power gain (S_{21}) and NF. Table shows variations of NF by the gain mismatch between two paths in simulation.

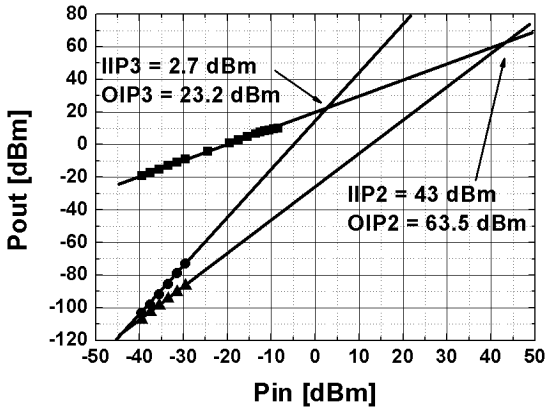

Fig. 6. IIP3 and IIP2 measured at maximum gain and 450 MHz.

de-embedding of balun and PCB interconnect losses. The maximum gain is 20.5 dB at 450 MHz and the 3-dB bandwidth is about 20–1175 MHz. The average noise figure is 3.3 dB over the operating frequencies. Simulated NF shown in Fig. 5 is obtained with a noise factor γ of 1. The table in Fig. 5 shows variations of NF by the gain mismatch between CG and CS paths in the simulation. It exhibits that NF of the LNA is not sensitive to the gain mismatch between two paths. The S_{11} and S_{22} are measured to be under -10 dB over operating frequencies (not shown). Fig. 6 shows IIP3 and IIP2 measured at maximum gain and 450 MHz. The IIP3 of 2.7 dBm (OIP3 of 23.2 dBm) and IIP2 of 43 dBm (OIP2 of 63.5 dBm) exhibit an excellent linearity performance at the maximum gain. The measured parameters of the proposed LNA are summarized and compared with the other wideband LNAs in Table I [6]–[8]. The linearity figures-of-merits (FOMs) defined as $10\cdot\log$ (OIP3(mW)/$P_{\rm dc}$ (mW)) are also compared in Table I, [5]. The proposed LNA with the current amplification scheme shows the best linearity FOM among previously reported wideband differential LNAs, and low average NF with the help of the noise-canceling technique.

TABLE I
PERFORMANCE COMPARISON TABLE OF THE PROPOSED LNA WITH THE REPORTED WIDEBAND LNAS

Reference	[2]	[6]	[7]	[8]	This work
BW [MHz]	2 - 1600	54 - 880	40 - 900	100 - 930	20 – 1175
Gain	13.7 dB	22 dB	20.3 dB	13 dB	20.5 dB
NF	2.5 dB	2.8 dB	4.0 dB	4.0 dB	3.3 dB
IIP3	0 dBm	-21 dBm	-10.8 dBm	-10.2 dBm	2.7 dBm
OIP3	13.7 dBm	1 dBm	9.5 dBm	2.8 dBm	23.2 dBm
IIP2	12 dBm	-	-	-	43 dBm
Differential	No	Yes	Yes	Yes	Yes
Area	0.08 mm^2	0.71 mm^2	0.57 mm^2	0.27 mm^2	0.12 mm^2
Technology	0.25μm CMOS	0.18μm CMOS	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS
Power	14mA@2.5V	23mA@1.8V	23.9mA@1.8V	0.6mA@1.2V	18mA@1.8V
Linearity FOM	0.670	0.030	0.207	2.646	6.448

IV. CONCLUSION

In this letter, a differential CG LNA with the positive current feedback is proposed for achieving high gain and good linearity. By utilizing the noise-canceling technique based on the current amplifier, the noise and linearity performance of the LNA are greatly improved. The 0.18-μm CMOS LNA for digital TV tuners exhibits a power gain of 20.5 dB, an IIP3 of 2.7 dBm, an IIP2 of 43 dBm, and an average NF of 3.3 dB, while consuming 32.4 mW from a 1.8 V supply with 0.12 mm^2 area.

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