

Thermal cycling reliability of Cu/SnAg double-bump flip chip assemblies for 100 μm pitch applications

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A thick Cu column based double-bump flip chip structure is one of the promising alternatives for fine pitch flip chip applications. In this study, the thermal cycling (T/C) reliability of Cu/SnAg double-bump flip chip assemblies was investigated, and the failure mechanism was analyzed through the correlation of T/C test and the finite element analysis (FEA) results. After 1000 thermal cycles, T/C failures occurred at some Cu/SnAg bumps located at the edge and corner of chips. Scanning acoustic microscope analysis and scanning electron microscope observations indicated that the failure site was the Cu column/Si chip interface. It was identified by a FEA where the maximum stress concentration was located during T/C. During T/C, the Al pad between the Si chip and a Cu column bump was displaced due to thermomechanical stress. Based on the low cycle fatigue model, the accumulation of equivalent plastic strain resulted in thermal fatigue deformation of the Cu column bumps and ultimately reduced the thermal cycling lifetime. The maximum equivalent plastic strains of some bumps at the chip edge increased with an increased number of thermal cycles. However, equivalent plastic strains of the inner bumps did not increase regardless of the number of thermal cycles. In addition, the z -directional normal plastic strain ϵ_{22} was determined to be compressive and was a dominant component causing the plastic deformation of Cu/SnAg double bumps. As the number of thermal cycles increased, normal plastic strains in the perpendicular direction to the Si chip and shear strains were accumulated on the Cu column bumps at the chip edge at low temperature region. Thus it was found that the Al pad at the Si chip/Cu column interface underwent thermal fatigue deformation by compressive normal strain and the contact loss by displacement failure of the Al pad, the main T/C failure mode of the Cu/SnAg flip chip assembly, then occurred at the Si chip/Cu column interface shear strain deformation during T/C. © 2009 American Institute of Physics. [DOI: 10.1063/1.3042236]

I. INTRODUCTION

In previous research, a Cu/SnAg double-bump structure was proposed and demonstrated for fine pitch flip chip applications on organic substrates.¹⁻³ To avoid bump bridging problem below 150 μm pitch, many researchers have studied Cu/SnAg double-bump structure consisting of thick Cu column and SnAg solder bumps.²⁻⁶ During the solder reflow of flip chip assembly processes, Cu bumps maintain their columnar shape, and SnAg solder bumps play a role of a wetting layer with metal pads of the substrate.

The Cu/SnAg double-bump structure provides three notable advantages in flip chip on organic boards assemblies. First, this structure enables finer pitch flip chip applications compared with conventional solder flip chip assembly. Second, it guarantees excellent electromigration reliability due to the high melting temperature and good electrical conductivity of Cu at the current crowded site.⁷ In the conventional solder flip chip, Sn reacts with Cu or Ni UBM (under bump

metallurgy) very rapidly due to its low melting temperature under current stressing. In particular, Sn and Cu or Ni atoms as UBM materials at the current-crowded site are severely consumed, thus degrading the reliability of the solder joint under current stressing.⁷⁻⁹ Finally, better thermal cycling (T/C) reliability of flip chip assemblies is expected at a higher stand-off bump height. In general, the maximum shear stress acting on flip chip joints is known to be inversely proportional to the stand-off height, which can be easily controllable by thicker copper plating at Cu/SnAg double-bump structure.¹⁰

The T/C test is one of the most common reliability tests especially for flip chip applications. Flip chip assemblies experience thermomechanical shear stressing by the thermal mismatch of a Si chip and organic substrates. In order to maintain the compliance of a Si chip and organic substrates, flip chip joints such as solder bumps or Cu/SnAg double bumps are highly stressed. This can cause plastic deformation when large stress exceeding or close to the yield stress of the flip chip joint is repetitively applied or inelastic strain

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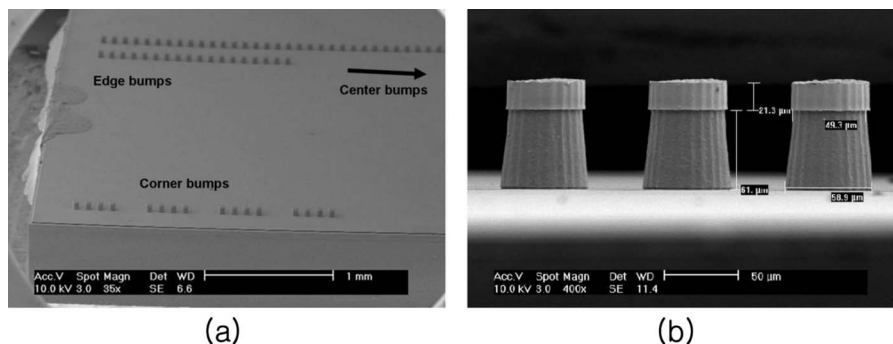


FIG. 1. Electroplated Cu/SnAg double bumps (a) tilted view and (b) side view of Cu column/SnAg bumps.

accumulated at flip chip joints during T/C. As a result, flip chip joints can fail physically and electrically.

Therefore, the evaluation of T/C reliability and the investigation of the T/C failure mechanism of the Cu/SnAg double-bump structure are essential for fine pitch flip chip applications. Furthermore, the T/C reliability of Cu/SnAg double-bump flip chip assemblies with various Cu column heights was also studied by a failure analysis. In this study, T/C test results and failure analyses of Cu/SnAg flip chip assemblies are investigated through the correlation of experimental results and finite element analysis (FEA).

II. EXPERIMENTS

In this study, a typical graphic memory chip design was chosen to prepare test chips. The size of the test chip is $9.8 \times 11.03 \text{ mm}^2$. The test chip has a mixed I/Os configuration at the middle of the chip and chip corners. Cu/SnAg double bumps at the chip corners are dummy bumps, which play a role in leveling the chip during flip chip bonding. The test chip has 128 bumps in the middle of the chip, and 92 bumps out of 128 middle bumps are arranged in a row. Figure 1 shows Cu/SnAg double bumps on a test chip used in this study. First of all, 600 \AA thick silicon oxide layer was deposited on an 8 in. silicon wafer by thermal oxidation, and a Ti(100 \AA)/TiN(200 \AA) layer was deposited on the silicon oxide layer as a stress buffer layer and an adhesion layer. Also then, $1 \text{ }\mu\text{m}$ thick Al layer was sputtered and patterned for metal pads and conductor lines. After the formation of $1 \text{ }\mu\text{m}$ thick Al chip pad of $60 \times 60 \text{ }\mu\text{m}^2$ size, $8 \text{ }\mu\text{m}$ thick polymer passivation is formed with $40 \text{ }\mu\text{m}$ opening size. A TiW(1000 \AA)/Cu(4000 \AA) layer is then deposited by sput-

tering and a thick photoresist is then patterned for Cu and SnAg bump formation. A $60 \text{ }\mu\text{m}$ thick Cu column and $20 \text{ }\mu\text{m}$ thick SnAg solder are then continuously deposited by an electroplating method. After photo resist (PR) stripping, seed layer etching, and chip singulation, a test chip with Cu/SnAg double bumps of $100 \text{ }\mu\text{m}$ pitch is flip chip assembled on an organic printed circuit board (PCB) substrate. Figure 2 shows a cross-sectional image of Cu/SnAg double-bump flip chip joints assembled on an organic substrate.

For the electrical continuity measurement, special PCB Cu conductor lines are used. As shown in Fig. 3, the contact resistance of a bump at a specific position can be detected using a four-point Kelvin structure. PCBs have 19 Kelvin structured groups, which are classified into three measuring groups: (1) at the chip center (three points, named center bumps), (2) at the chip edge (eight points, named edge bumps), and (3) at the chip corners (eight points, named corner bumps). T/C tests were carried out up to about 1000 cycles under a temperature range from $-55 \text{ }^\circ\text{C}$ (15 min) to $+125 \text{ }^\circ\text{C}$ (15 min) following the JEDEC standard JESD22-A-104-B. During the T/C test, the changes in the bump contact resistances were measured every 150–200 cycles. The failure criterion was defined as $100 \text{ m}\Omega$ of the bump contact resistance. After 1000 cycles, a failure analysis was conducted using a scanning electron microscope (SEM) and a scanning acoustic microscope (SAM).

A FEA using ABAQUS was performed to extract the applied plastic stress and strain distribution at the Cu/SnAg double-bump flip chip joints. To simplify the flip chip design, two-dimensional (2D) finite element model was con-

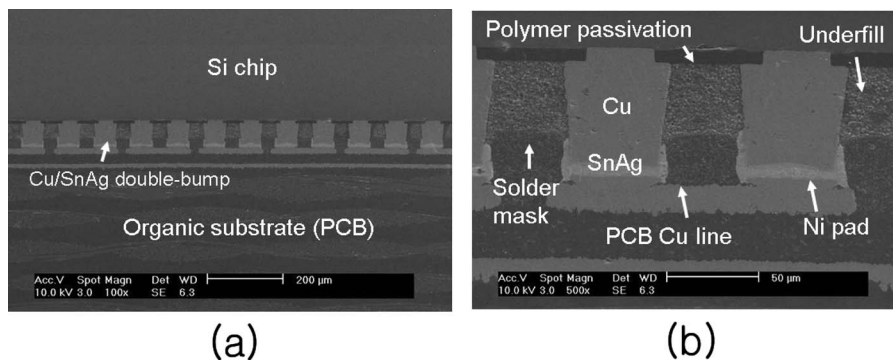


FIG. 2. (a) Cross-sectional image of Cu/SnAg double-bump flip chip assembly and (b) magnified image of (a).

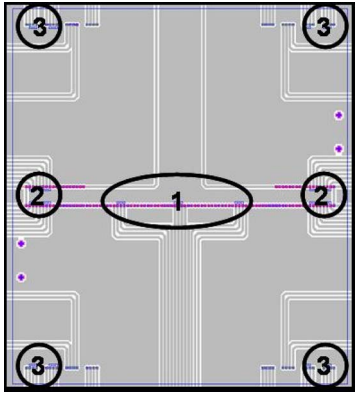


FIG. 3. (Color online) PCB Cu line design for bumps contact resistance measurement: (1) chip center, (2) chip edge, and (3) chip corner.

structed for half of 92 double-bump joints in the middle of a chip considering the symmetry as shown in Fig. 4. Table I presents the material properties applied in the FEA. In a FEA, there are four important assumptions. First, it was assumed that flip chip assemblies are in stress-free status at room temperature. In general, a flip chip assembly on an organic substrate has a flattened shape above glass transition temperature of an underfill material and is deformed to downward direction and eventually is warped into a cap (convex) shape when it is cooled down. However, in this case, the number of calculation was too large because of large thermal range ΔT of 180 °C under T/C test conditions from +125 °C to -55 °C. Therefore, stress-free temperature was considered as room temperature and thermal gradient ΔT was 100 °C during heating and 80 °C during cooling, respectively. Even though stress-free temperature is considered as room temperature, the deformed shape of a flip chip assembly in the low temperature region in FEA is almost the same as that of the T/C test. Both cases of FEA and the T/C test, a flip chip assembly is deformed to a convex shape toward a Si chip side but the amount of deformed shape such as warpage or the plastic strain will be different from each other because ΔT is not equal. The amount of the plastic deformation will increase in the actual case than the calcu-

lated values in FEA. However, this assumption is quite reasonable because it does not affect in investigating the accumulation of the plastic strain as well as relative deformation behaviors. Second, the yield strength of Cu is assumed as 69 MPa, yield strength of bulk Cu. The yield strength of electroplated Cu is dependent on grain size, impurities, plating current density, and so on. It has been reported from similar range with that of bulk Cu to 200–250 MPa.¹¹ However, the yield strength of Cu does not affect plastic strain below the yield strength of Cu and the plastic strain is directly related to T/C fatigue deformation. Therefore, the yield strength of Cu is set as 69 MPa, well-known yield strength of bulk Cu. Third, Al pads and TiW adhesion layer were ignored because they are very thin layers. Finally, creep deformation of Cu was ignored because it is much lower than that of lead-free solder. Creep shear deformation is dominant T/C failure mechanism in lead-free solder flip chip packages.¹² The creep shear rate of electroplated Cu is 10^{-36} – 10^{-14} at -50 °C–150 °C, 100 MPa as follows:

$$\dot{\epsilon} = 46.16 \frac{\mu}{T} \left[\sinh \left(458.4 \frac{\sigma}{\mu} \right) \right]^{4.8} \exp \left(\frac{-2.369 \times 10^4}{T} \right), \quad (1)$$

where T is temperature, s is creep stress, and \square is shear modulus, where

$$\mu = 4.713 \times 10^{10} [1 - 3.557 \times 10^{-4} T]. \quad (2)$$

On the other hand, the creep shear rate of SAC405 is given in the following:

$$\dot{\epsilon} = 4.41 \times 10^4 [\sinh(0.005 \times 10^6 \sigma)]^{4.2} \exp \frac{-4.4995 \times 10^4}{RT}, \quad (3)$$

where R is gas constant.

At equivalent stress and temperature range with Cu, creep shear rate of lead-free solder is 10^{-8} – 10^{-3} . Therefore, creep shear deformation of Cu is negligible.

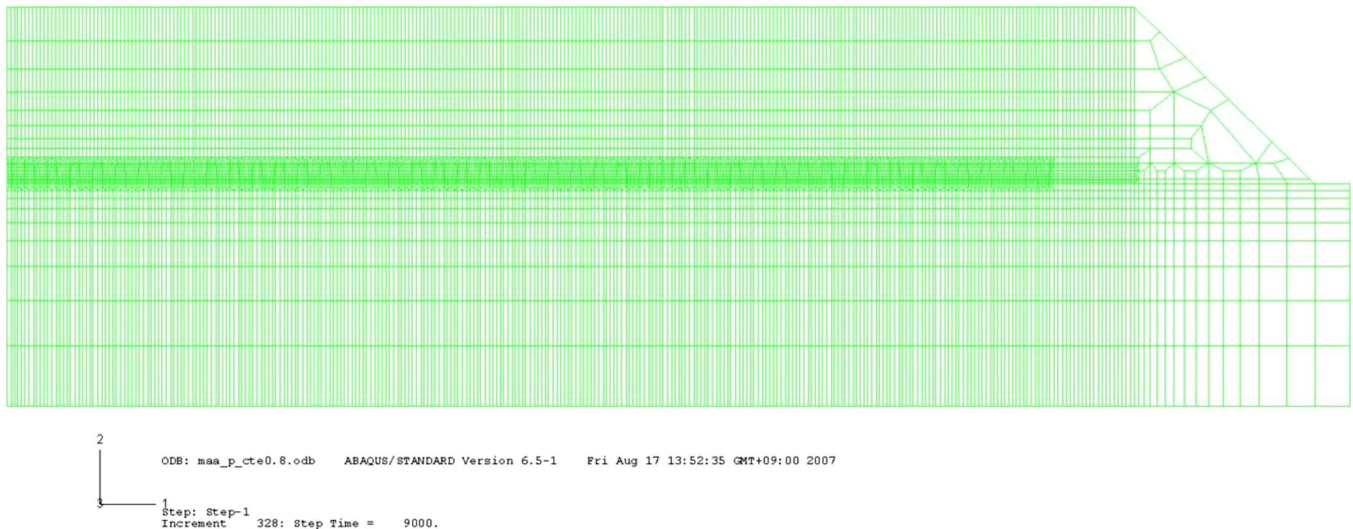


FIG. 4. (Color online) Mesh design for FEA.

TABLE I. Material properties used in 2D FEA.

Properties	Si	SnAg	Underfill	Passivation	Cu	Ni-P	FR4
Density (g/cm ³)	2.3	7.36	1.6	0.95	8.9	8.9	1.9
Young's modulus (GPa)	131	56	6	4.0 (25 °C) 1.2 (150 °C)	76	213	22
Poisson's ratio	0.3	0.4	0.35	0.35	0.35	0.2	0.28
CTE (ppm)	2.8	22	28/100 (T_g : 120 °C)	59 (α_1)	17	12.9	18.5
Thermal conductivity (W/m K)	148	22	1.7	None	393	92	1.7
Specific heat (J/kg K)	700	227	800	None	385	436	800
Yield strength (MPa) strain 0/0.01/0.1	Elastic	30/45/180 at 25 °C	Elastic	Elastic	69.0	45	Elastic

III. RESULTS AND DISCUSSION

Figure 5(a) presents the cumulative distribution of the failure rate after the T/C test. The Cu/SnAg double-bump flip chip assembly shows no increase in the contact resistance until 407 cycles. However, the bump contact resistances increase after 407 cycles, and about 35% of the Cu/SnAg double-bumps have contact resistance larger than 100 m Ω after 1000 cycles. Figure 5(b) shows the bump position dependency of the failure rate after the T/C test. As the distance from the chip center increases, the contact resistance of the Cu/SnAg double bumps increases rapidly. Cu/SnAg double bumps at the chip center do not fail even after 1000 cycles. However, the failure rate of the corner bumps exceeds 80% after 1000 cycles. The T/C failure rate of corner bumps as dummy bumps for flip chip bonding does not have significant meaning and it was just measured for data gathering and the investigation of bump position dependency. It has been argued that larger stress acts on the outmost bump joints during T/C.^{13–16}

To understand the T/C failure site and the failure mode, SAM analyses and cross-sectional SEM observations were carried out. Figures 6(a) and 6(b) show SAM C-scan images of the Si chip/Cu column interface after 85 °C/85% relative humidity (RH) test for 1000 h and 1002 T/C cycles, respectively. In the SAM analysis, black colored bumps maintain contact well, whereas white colored bumps show interface

failures such as delamination, voids, or cracks. In the 85 °C/85% RH test for 1000 h, no delamination occurs at the bump interface. On the other hand, after 1002 T/C cycles, delamination at the Si chip and Cu column bump interface, shown in white color in the SAM images, is observed at the corner and edge bumps. However, the center bumps maintain their initial contact even after 1000 T/C cycles. The contact resistance measurement results presented in Fig. 5(b) for the bump position agree well with the SAM images. Cross-sectional SEM images of a failed Cu/SnAg double bump presented in Fig. 7 show the bump failure mode after 1000 thermal cycles. Although the Cu/SnAg double-bump flip chip assemblies have solder bumps with much lower thickness than the conventional solder flip chip assemblies, mechanical degradations such as cracks or delamination are not observed around the SnAg solder. As shown in Fig. 7(b), the Al pad and Ti layer between the Si chip and Cu column bump still remain for the center bumps with no T/C failure even after 1000 cycles. In the case of the center bumps, the bottom surface of the Cu column at the Al/Cu interface is smooth and retains the original shape of the electroplated Cu/SnAg double bumps. On the other hand, in the case of failed bumps at the chip corners and chip edges, the Al pad and Ti layer are depleted after 1000 cycles as shown in Fig. 7(c), and the bottom surface of the Cu column becomes rough. It appears that the Al pad is mechanically damaged

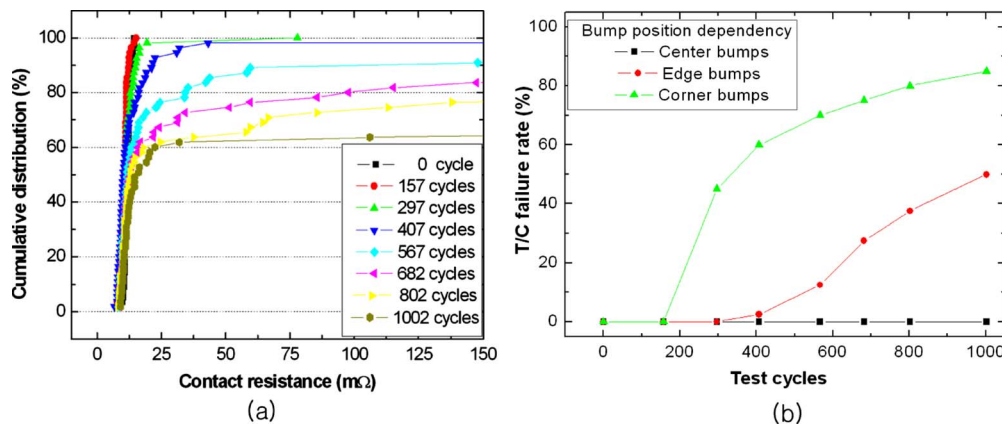


FIG. 5. (Color online) T/C test results of Cu/SnAg double-bump flip chip assembly (a) cumulative distribution and (b) the ratio of contact resistance of bumps over 100 m Ω at various bump positions.

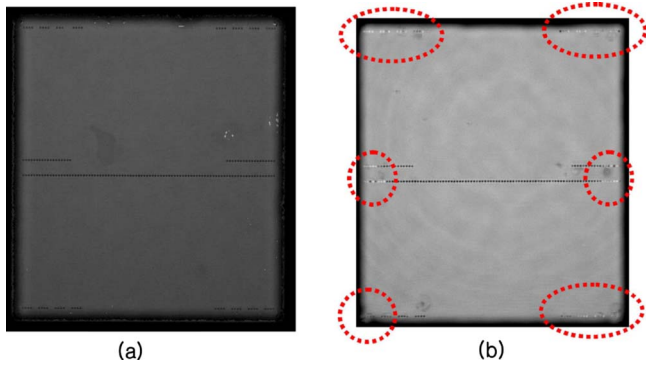


FIG. 6. (Color online) SAM C-scan images of Cu/SnAg double-bump flip chip assembly after (a) reliability tests 85 °C/85% RH, 1000 h and (b) T/C test, 1002 cycles.

during T/C presumably due to thermal fatigue deformation. The failure mode observed in Fig. 7 corresponds well with the failure site, as indicated by SAM C-scan images shown in Fig. 6(b), and the bump position dependency on T/C failures, as shown in Fig. 5(b).

FEA can provide information on the location of failure site and the governing stress and strain components related to the T/C failure mechanism. In addition, the stress/strain distribution and thermal fatigue lifetime can be predicted, which is useful for better T/C reliability. From the FEA results, the distribution of von Mises stress and the summation of normal stress and shear stress can be obtained during T/C. The flip chip assembly has a concave shape toward a Si chip side at room temperature and becomes flat above the glass transition temperature of the underfill material due to the thermal expansion of the organic PCB substrate. However, in this study, it was assumed that the flip chip assembly is in a stress-free state at room temperature for the convenience of the FEA.

Large stress is concentrated at the upper and lower corners of the Si chip contacting an underfill fillet. However, the highest stress concentration site, which can lead to T/C failure of the joints, is the Si/Cu interface, as shown in Fig. 8(a). The yield strength of Si is much higher than that of Cu, and thus it can be assumed in the FEA that the Si chip behaves nearly elastically. Therefore, it is found that the effective stress related to the plastic deformation is applied to the corner of the Cu column bumps in contact with polymer passivation and the Si chip. As a result, the Si/Cu interface may be the location that is most susceptible to plastic deformation during T/C. The von Mises stress distribution determined by the FEA agrees well with the failure site as determined by the T/C test results.

Figure 8(b) presents a graph of the von Mises stress acting on one element with the maximum stress at each Cu column bump according to T/C time. In this graph, n denotes the n th Cu/SnAg double bump from a chip edge. In other words, the first double bump indicates the outermost Cu/SnAg bumps and the 46th joint indicates a Cu/SnAg double bump at the chip center. Due to the thermal deformation of the Si chip and PCB substrate by coefficient of thermal expansion (CTE) mismatch, large von Mises stress is induced in the high temperature region during T/C and it is reduced in the low temperature region. From about the 10th–46th bumps, von Mises stresses on each Cu column bump are almost the same. However, the stress is not released for the 1st to 7th–10th Cu/SnAg double bumps at the chip edge, and they retain large von Mises stress in the low temperature region, as presented in Fig. 8(b). In particular, the first–fourth bumps at the chip edge show von Mises stress close to the Cu yield strength, which can result in permanent plastic deformation.

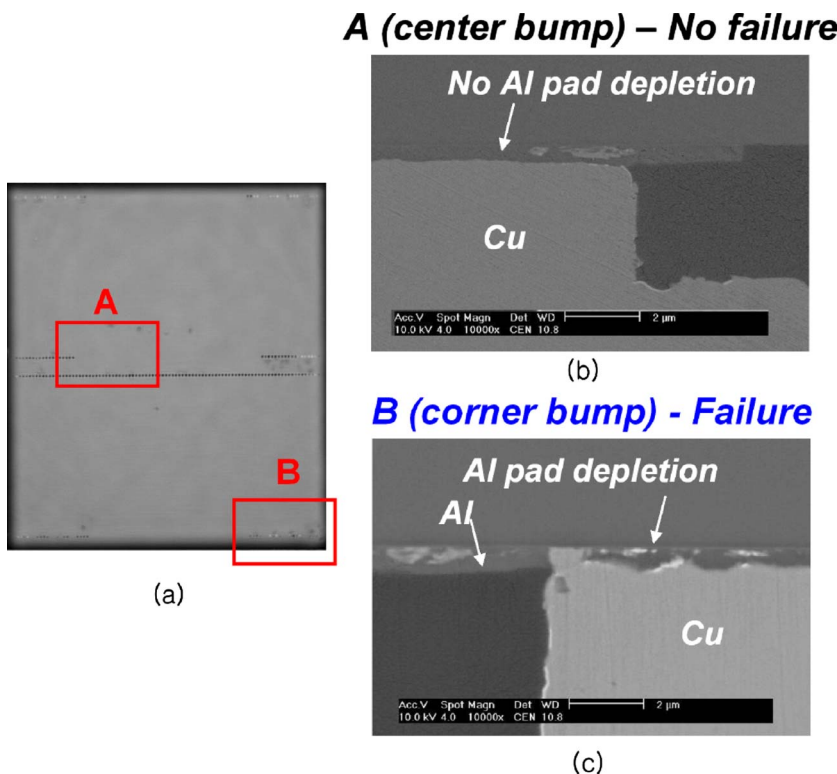


FIG. 7. (Color online) T/C failure of Cu/SnAg double-bump flip chip assembly: (a) SAM image, (b) cross-sectional image of A position (center bumps), and (c) cross-sectional image of B position (corner bumps).

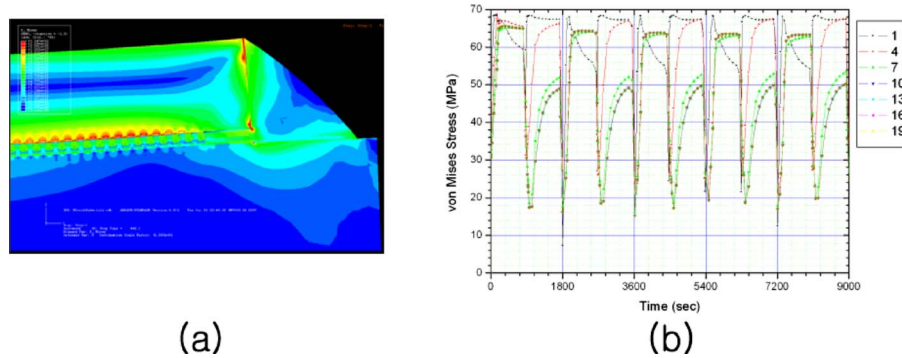


FIG. 8. (Color online) FEA results: (a) the deformation of a flip chip assembly at 125 °C and (b) Von-Mises stress distribution during T/C.

As mentioned before, Al pad depletion is the main failure mode of the Cu/SnAg double-bump flip chip assembly under T/C. However, in order to clearly investigate the Al pad depletion during T/C, an electron probe microanalysis (EPMA) mapping analysis was conducted for a failed sample. The EPMA mapping results shown in Fig. 9 clearly indicate the failure mode of the Cu/SnAg double-bump flip chip assembly during T/C. As shown in Fig. 9, the Al pad between the Si chip and a Cu column bump is displaced. The concentration of Al then becomes higher at the interface between the polymer passivation layer and the Si chip than at the Cu column and Si interface. The displacement of the Al pad to the region outside of the Cu column bump is the dominant failure mode during T/C.

From the equivalent plastic strain (PEEQ) and the dissipated energy density for the plastic deformation (PENER), the failed bump position and the effect of the plastic deformation on T/C failure can be investigated. The failure site can be determined from the von Mises stress distribution but thermal fatigue failure under T/C is generally analyzed and explained by the strain or dissipated energy for the plastic deformation.^{12,17,18}

In the FEA, the equivalent plastic strain (PEEQ) is defined as

$$\dot{\varepsilon}^{pl} = \sqrt{\frac{2}{3} \dot{\varepsilon}^{pl}_i \dot{\varepsilon}^{pl}_i}. \quad (4)$$

The dissipated energy by the plastic deformation (PENER) during T/C was calculated from

$$E = \sum_{i=1}^n W_i V_i, \quad (5)$$

where energy E , energy density W , and volume V are in J, J/m³, and m³, respectively, and n is the number of elements of interest. The dissipated energy density per cycle W is calculated from

$$\Delta W = \frac{\sum_{i=1}^n dE_i}{\sum_{i=1}^n V_i}, \quad (6)$$

where dE is an increase in E during a cycle at a stable stage.

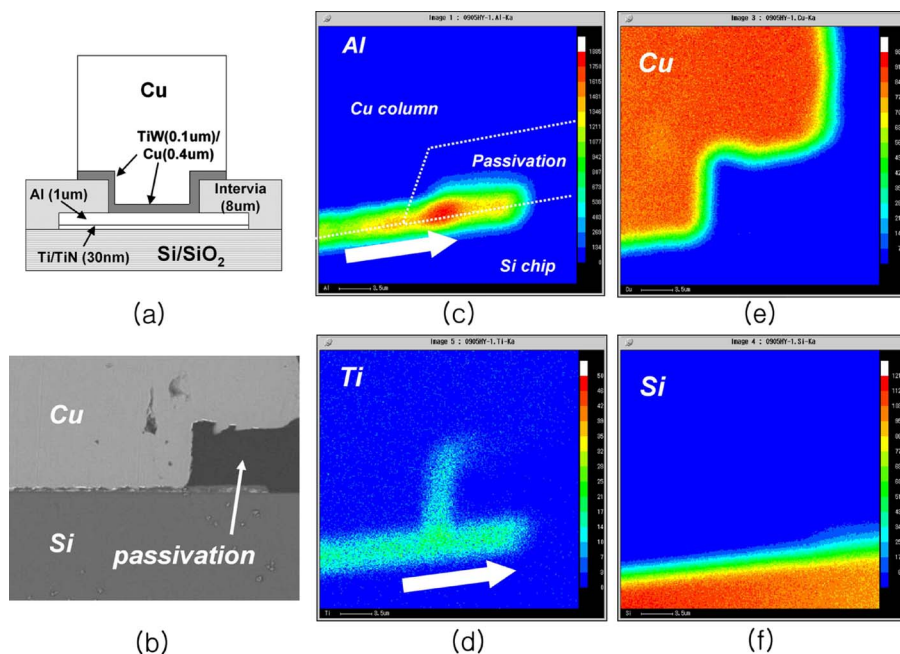


FIG. 9. (Color online) EPMA mapping results of Cu/SnAg double joints after T/C. (a) Schematic illustration of Cu/SnAg double bump, (b) SEM image of Si chip/Al pad/Cu column interface of corner bumps after 1002 thermal cycles, (c) Al mapping, (d) Ti mapping, (e) Cu mapping, and (f) Si mapping.

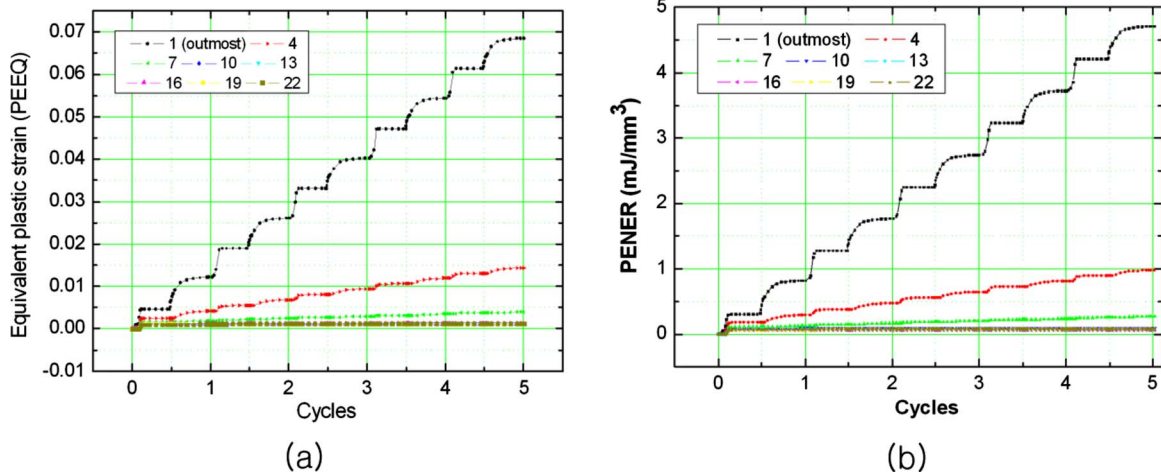


FIG. 10. (Color online) FEA results: (a) the equivalent plastic strain, PEEQ and (b) the dissipated plastic energy density.

As shown in Figs. 10(a) and 10(b), equivalent plastic strain (PEEQ) and dissipated plastic energy density (PENER) for the first to seventh bumps gradually increase with the number of T/C. While cyclic thermomechanical stress is repetitively added on the Cu column bumps, the accumulation of PEEQ and PENER can lead to irreversible plastic deformation during T/C. On the other hand, PEEQ and PENER are almost the same for the 10th–46th bumps from the chip edge. Therefore, the inner bumps are less susceptible to T/C fatigue failure. However, the accumulation of plastic strain at edge bumps (first to seventh bumps) leads to shorter T/C lifetime according to low cycle fatigue model, which is given by the Coffin–Manson equation as follows:

$$N_f^m = \Delta \epsilon_p = C, \tag{7}$$

where N_f is the number of cycles to failure, $\Delta \epsilon_p$ is the plastic strain, and m and C are constant.

The FEA results regarding PEEQ and PENER agree well with the T/C test results presented in Figs. 5(b) and 6(b). Therefore, it can be concluded that T/C failure is caused by the accumulation of plastic strain and energy dissipation for plastic deformation on Cu column bumps at chip edge.

In addition, by separating each stress and strain components, the factors affecting T/C fatigue failure related to the failure mechanism can be understood. Figure 11 shows three strain components for one element of a Cu column bump in contact with a Si chip during T/C. ϵ_{11} is the plastic normal

strain parallel to a chip, corresponding to the x -direction in the 2D FEA and ϵ_{22} is the plastic normal strain of the z -direction perpendicular to the chip. ϵ_{12} is the shear strain. As shown in Fig. 11(a), Cu column bumps are under compression mode at the transverse direction (parallel direction to the Si chip: x -direction). On the other hand, at the longitudinal direction (perpendicular direction to the Si chip: z -direction), the Cu column shows tensile normal plastic strain at high temperature region and compressive strain at the low temperature region, as shown in Fig. 11(b). At the high temperature region, the normal plastic strain decreases with an increased number of thermal cycles except for the outermost bump. However, the normal plastic strain in the z -direction becomes higher in the low temperature region and it dominantly affects the thermal fatigue failure. Figure 12 shows the maximum plastic strain in the z -direction at the low temperature region. The outermost bump at the chip edge has very high compressive strain and it is almost the same regardless of T/C time. In this case, the Cu column bump tends to be plastically deformed because its calculated von Mises stress is greater than the yield strength of Cu even though the plastic strain is not accumulated. In the case of the second to fourth bumps at the chip edge, the normal plastic strain in the z -direction gradually increases to the compressive direction and then accumulated at the low temperature region as the T/C time increases. In addition, shear strain of the outermost Cu column bumps gradually increases

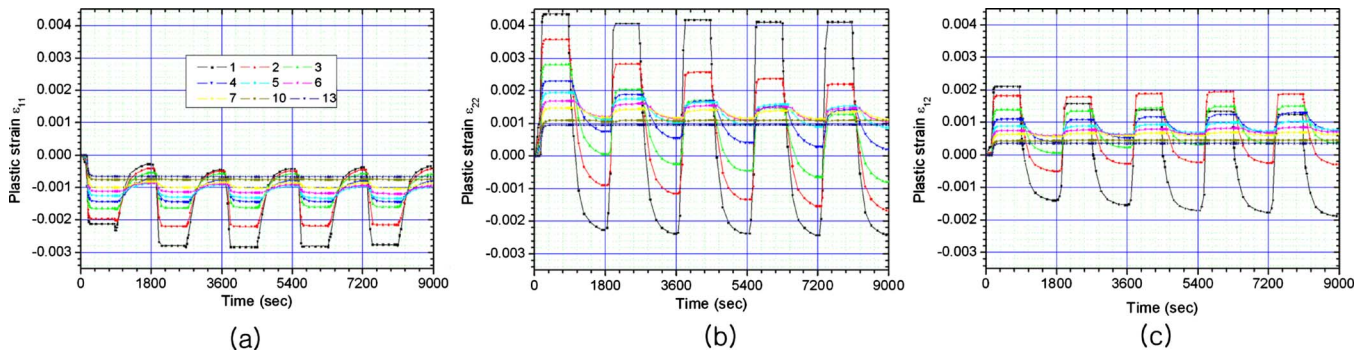


FIG. 11. (Color online) Strain components on Cu column bumps. (a) ϵ_{11} —plastic normal strain in the x -direction (transverse direction of a Si chip), (b) ϵ_{22} —plastic normal strain in the z -direction (perpendicular direction of a Si chip), and (c) ϵ_{12} —plastic shear strain.

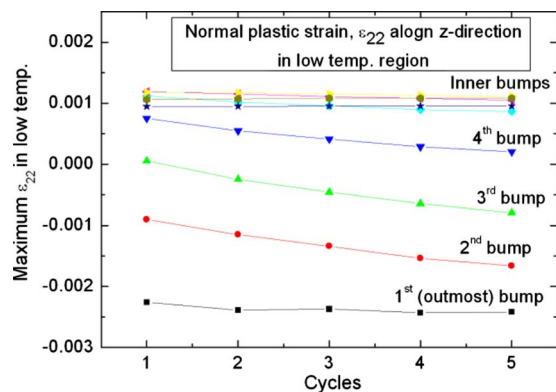


FIG. 12. (Color online) Maximum normal plastic strain on Cu column bumps in the z -direction in low temperature region (ϵ_{22}),

to the compressive direction. When compressive normal plastic strain in the z -direction is accumulated on Cu column bumps, thermal fatigue deformation occurred at the Si chip/Cu column interface. At this moment, the Al pad between the Si chip and the outmost Cu column bump is displaced to the outside of Cu column bumps by shear strain and an electrical and physical failures between an Al pad and a Cu column bump occur by the contact loss. After the contact loss of the Al pad/Cu column interface occurs at the outmost bump, the location of stress concentration can be shifted to the second bump of the chip edge and the second Cu column bump can also fail. For the third and fourth bump at the chip edge, it is expected that the thermal fatigue failure similarly occurs by compressive normal strain of the z -direction and shear strain concentration.

Therefore, the Al pads between the Si chip and Cu column bumps cannot withstand the compressive normal stress and strain in the z -direction, resulting in the thermal fatigue deformation of the Cu column bumps and are then displaced by shear strain. In other words, the displacement failure of the Al pads, as shown in Figs. 7 and 9, results from the compressive normal strain in the z -direction and shear strain. This is the major T/C failure mechanism in double-bump flip chip assemblies using thick Cu column bumps.

IV. CONCLUSION

In this study, the T/C reliability and failure mechanisms of Cu (60 μm)/SnAg (20 μm) double-bump flip chip assemblies with 100 μm pitch were investigated through correlation of T/C test results and a FEA. During the T/C test, the failures of Cu/SnAg double bumps occurred at the Si chip/Cu column interface, where the highest stress concentration occurs in the FEA. The Al pads between the Si chip and Cu column bumps were displaced to the outside region of the Cu column bumps, resulting in subsequent T/C fatigue failure. From the FEA, the equivalent plastic strain continuously increased as the number of thermal cycles increased. In particular, it was found that the plastic strains of the Cu

column bumps increased for the first to seventh to tenth bumps at the chip edge with the number of thermal cycles. Therefore, the accumulation of plastic strain was the main cause of thermal fatigue failure because, according to the low-cycle fatigue model, the time to failure decreased as the plastic strain increased. The distribution of bumps having higher equivalent plastic strain and dissipated plastic energy for plastic deformation in the FEA corresponds well with the number of failed bumps during the T/C test. In addition, the compressive normal stress in the perpendicular direction to the Si chip ϵ_{22} was the dominant strain component determining the thermal fatigue failure of Cu/SnAg double-bump flip chip joints. By the accumulation of plastic strain in the z -direction in the low temperature region ϵ_{22} , the compressive normal strain and stress were applied at the Si chip/Cu column interface. As a result, the Al pads between the Si chip and Cu column bumps cannot withstand the compressive normal stress and strain in the z -direction during T/C.

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