Vertically Integrated Nanowire-Based Zero-Capacitor Dynamic Random Access Memory

Byung-Hyun Lee,[a,b] Min-Ho Kang,[c] Dae-Chul Ahn,[a] and Yang-Kyu Choi[a,z]

[a] *School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Yuseong-gu, Daejeon 34141, Korea*
[b] *Department of Memory Business, Samsung Electronics, Hwasung-City, Gyeonggi-Do 18448, Korea*
[c] *Department of Nano-process, National Nanofab Center (NNFC), Yuseong-gu, Daejeon 34141, Korea*

This paper demonstrates a breakthrough for DRAM scaling: A vertically integrated gate-all-around (GAA) silicon nanowire (SiNW) channel-based dynamic random access memory (DRAM) without a cell capacitor for data storage, i.e., a zero-capacitor DRAM unlike the conventional DRAM. Vertical integration of the SiNW was attained by a one-route all-dry etching process (ORADEP), resulting in stiction-free stability and simplicity in the fabrication process. High performance that is suitable for high packing density integration is presented with vertically integrated multiple channels, which reveals a potential for an ultimate scaling of DRAM toward the end of the roadmap.
© The Author(s) 2016. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution Non-Commercial No Derivatives 4.0 License (CC BY-NC-ND, http://creativecommons.org/licenses/by-nc-nd/4.0/), which permits non-commercial reuse, distribution, and reproduction in any medium, provided the original work is not changed in any way and is properly cited. For permission for commercial reuse, please email: oa@electrochem.org. [DOI: 10.1149/2.0011701jss]
All rights reserved.

Manuscript submitted September 6, 2016; revised manuscript received November 1, 2016. Published December 6, 2016. This was Paper 1850 from the Honolulu, Hawaii, Meeting of the Society, October 2–7, 2016.

With the advent of 20 nm dynamic random access memory (DRAM),[1] manufacturers of DRAM encounters the immense challenge of continuous scaling of a cell area, e.g., beyond $6F^2$ where F denotes a feature size. In particular, the cell capacitor for data storage in DRAM is a bottleneck that impedes continuous scaling. Under these circumstances, reconsidering a zero-capacitor DRAM (ZRAM) that consists of only one transistor (1T) is a timely approach.[2,3] Compared to conventional DRAM, the main advantages of the ZRAM is cell size reduction and nondestructive reading. Moreover, one of the greatest advantages of ZRAM is that there is no need to make a sense amplifier for identifying a data state. This can allow a versatile core and periphery circuit architecture that enhances the device performance because the area presumably occupied by the sense amplifier is no longer needed. Additionally, high sensing current or a sensing margin (I_{ON}/I_{OFF}) as large as possible is preferred for stable memory operation. In this regard, the notable increment of data sensing current based on the vertically integrated multi-stacked channels is very attractive for future DRAM technology.[4]

On the other hand, short-channel effects (SCEs) have been considerably problematic in aggressive miniaturization of the transistor.[5,6] Such a trend cannot be exceptional in the scaling of a memory device. With respect to the suppression of the SCEs, a structural optimization of the transistor, i.e., multi-gated structures such as double-gate or tri-gate structures, have been considered as a successful approach.[7–9] In particular, the gate-all-around (GAA) silicon nanowire (SiNW) configuration is reportedly the most superior for suppressing I_{OFF} due to its excellent gate controllability,[10] which enabled a demonstration of extremely scaled transistors up to sub-10 nm.[11,12] In addition, the versatile SiNW configuration itself has attracted attention for various applications.[13–15] But, the extreme scaling of the SiNW inevitably sacrifices I_{ON} due to a decrease in the cross-sectional channel area. Accordingly, an implementation of such a configuration requires a compromise between the controllability of I_{OFF} and the drivability of I_{ON}.[16] In this respect, a vertically integrated multi-stacked channel can recover the sacrificed I_{ON} that occurs with the scaling of the SiNW without a sacrifice of the scalability.[4,17]

In this study, the vertically integrated multi-stacked ZRAM with GAA SiNW channels (which is abbreviated as VI-ZRAM) is demonstrated. The vertical integration of the SiNW has been reported to meet a high performance, effective suppression of SCEs, and excellent scalability.Unlike previous studies,[18–23] the one-route all-dry etching process (ORADEP) in this study permitted a stable completion of the vertically integrated multiple channels with reproducibility. To fabricate the vertically integrated multiple nanowire channels, previous works employed dual material-stacked structure, e.g., silicon for a structural layer and silicon germanium for a sacrificial layer,[18–20] and additional processes such as oxidation and wet etching process.[22] Such approach is problematic in terms of process complexity and stiction fail. In addition, previous works still need to be further improved for uniformity and clear separation of each nanowire.[21,23] Compared to those, due to the removal of the wet etching and oxidation process in the ORADEP, a stiction-free process was built up with process simplicity. Images of the fabricated devices were clearly identified with the aid of high-resolution transmission electron microscopy (TEM). The fundamental performances of the VI-ZRAM including write/erase/read operations, switching endurance for reliability, and data retention time were assessed. For fair comparison, both a 1-channel (1-story) SiNW device and a 3-channel (3-story) SiNW device were fabricated as a control group. A 5-channel (5-story) SiNW device was fabricated as an experimental group. Furthermore, the ZRAM characteristics depending on the number of SiNWs were compared, resulting in broadened sensing margin for memory window with the larger numbers of SiNW.

Experimental

In the full processes, fabricating the vertically integrated SiNW structure is one of the most critical processes. As previously mentioned, the structure was completed by the development of the ORADEP, which has high reproducibility and high stability.[4,17] As shown in the schematic of Figure 1a, one cycle of the ORADEP consists of two steps that are based on an in-situ process in a single etching chamber. One is C_4F_8 polymer passivation and the other is an isotropic dry etching process using SF_6 gas. During the isotropic dry etching process, a passivated polymer created by the C_4F_8 process serves as a protector for a pre-patterned SiNW and the sidewall of the SiNW to be formed. The schematic shows that the number of cycles is equal to that of integrated SiNW. Figure 1b shows scanning electron microscopy (SEM) images of the SiNWs fabricated by the ORADEP. The images demonstrate that unique integration of multiple SiNW channels is possible via control of the number of the cycles. Since the ORADEP does not require the carving oxidation and subsequent wet etching to separate the SiNWs, a stiction-free device was fabricated without use of wet etching and with process simplicity. The full process to fabricate the VI-ZRAM is illustrated in Figure 2. A boron-doped (100) bulk-silicon wafer was used as a substrate. After the formation

[z] E-mail: ykchoi@ee.kaist.ac.kr

Downloaded on 2017-09-12 to IP 143.248.123.126 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

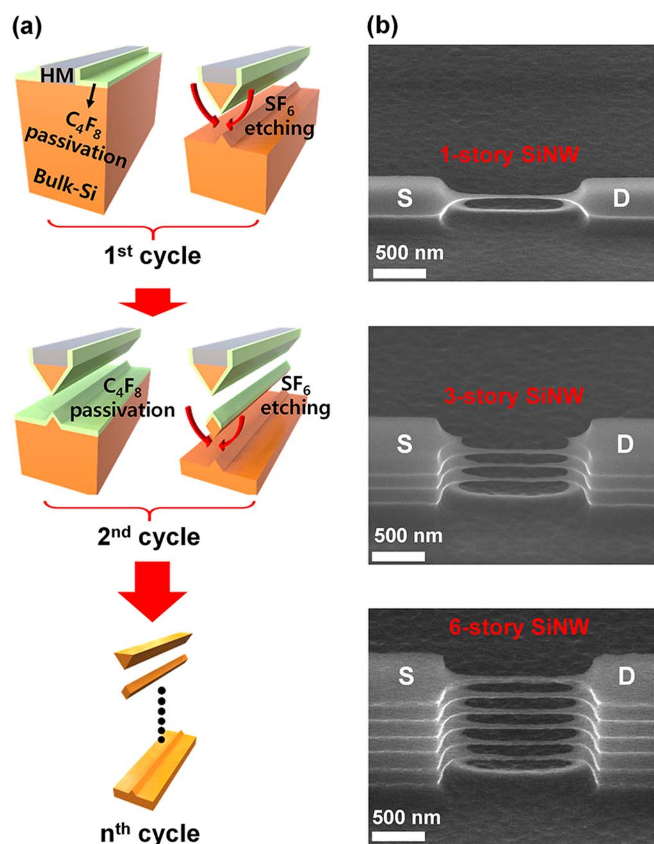

Figure 1. Fabrication of the vertically integrated SiNW structure. (a) Schematic of the ORADEP. (b) SEM images conforming that iterative etching cycles of the ORADEP permit multi-story SiNWs.

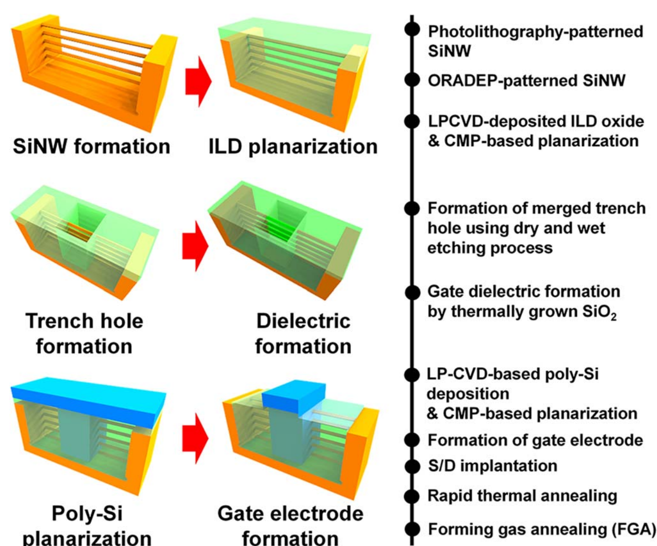

Figure 2. Schematic to explain the fabrication process of the VI-ZRAM.

of the SiNW by the ORADEP mentioned above, interlayer dielectric (ILD) oxide for isolation of each transistor was deposited and then planarized using a chemical-mechanical polishing (CMP) process. Fabricating the gate electrode was another critical process owing to the tall height of the vertically integrated SiNW, which was resolved by adopting an embedded gate structure. Unlike the fabrication process of single SiNW-based FET, in the proposed process, a "trench hole" mask designed for the vertically integrated SiNW-based FET enabled completion of an embedded gate structure. Thermally grown silicon dioxide (SiO_2) was formed to serve as the gate dielectric. The ion implantation process to form source and drain (S/D) electrode was done followed by rapid thermal annealing (RTA) process to activate the implanted dopant and to cure the ion implantation-induced damage. With the implementation of forming gas annealing process (FGA) to improve Si/SiO_2 interface state, the fabrication of the VI-ZRAM was completed. All processes are fully compatible with silicon CMOS (complementary metal-oxide-semiconductor) process and were progressed in clean FAB.

The schematic of the fabricated device are shown in Figure 3. Figure 3a shows a schematic of the VI-ZRAM and its cross-sectional images along with each direction, i.e., a-a′ (parallel to the gate length) and b-b′ (parallel to the SiNW length). Figure 3b concisely shows the operation of the VI-ZRAM, which is based on an accumulation of holes in the p-type SiNW body. The cross-sectional TEM images of the VI-ZRAM along the a-a′ direction of Figure 3a are shown in Figures 4a and 4b, where the VI-ZRAMs with three- and five-channels are respectively identified. With the aid of the ORADEP, uniform SiNW channels without stiction failure are completed, showing a clear separation of the SiNWs. One of SiNWs in Figure 4b is shown in Figure 4c. Poly-Si for the gate electrode fully wraps the SiNW with thermally grown SiO_2, demonstrating a complete GAA configuration. The energy-dispersive spectrometer (EDS) mapping image in Figure 4d clearly shows the separation of each layer, i.e., poly-Si for the gate, SiNW for the channel, and SiO_2 for the gate dielectric. Figure 4e shows the fast-Fourier transform (FFT) image that identifies the crystallinity of each layer. The FFT image of the SiNW, which shows an image of single-crystal, is obviously

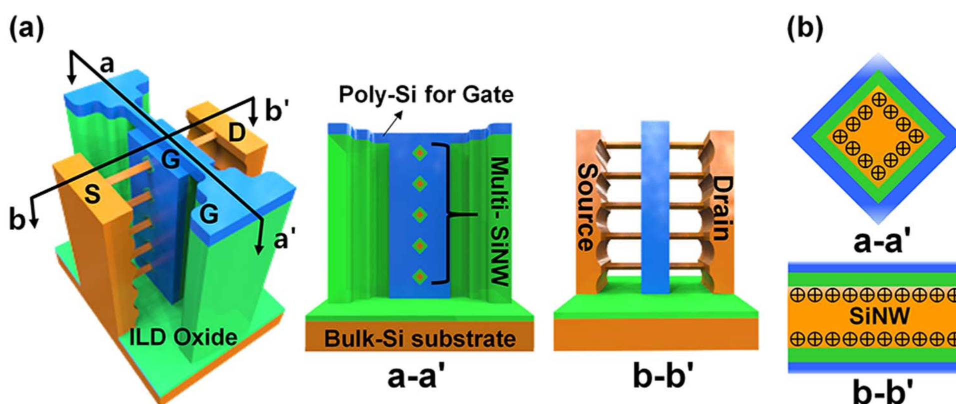

Figure 3. Schematic of the VI-ZRAM. (a) Schematic of the VI-ZRAM including cross-sectional profiles along the a-a′ and b-b′ directions. (b) Holes stored in the SiNW channel that activates the VI-ZRAM.

Downloaded on 2017-09-12 to IP 143.248.123.126 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

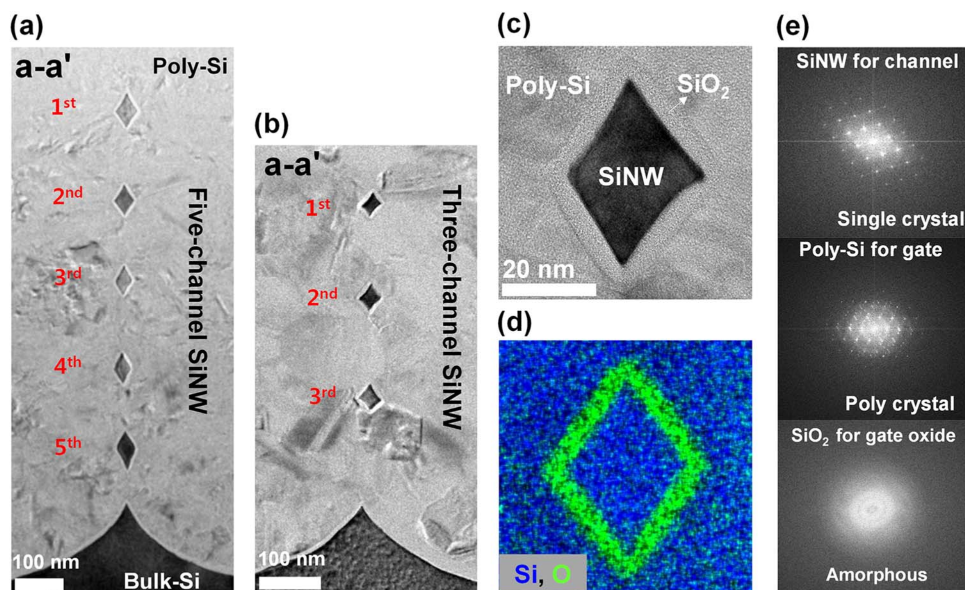

Figure 4. TEM images of the VI-ZRAM. (a) TEM image of the VI-ZRAM with five-SiNW channels. (b) TEM image of the VI-ZRAM with three-SiNW channels. (c) Close-up image of the SiNW. (d) EDS mapping image of the SiNW. (e) FFT images of the SiNW for the channel, poly-Si for the gate, and SiO_2 for the gate dielectric.

distinguished from that of the poly-crystalline Si. Despite the iterative dry etching process during the ORADEP, which may be a somewhat harsh condition compared to the typical one time dry etching process, the FFT image of the single crystal-SiNW proves the stability of the ORADEP.

Results and Discussion

Figure 5a exhibits the drain current-gate voltage (I_D-V_G) characteristic of the fabricated devices. The VI-ZRAM with five-channels exhibits the most enhanced performance over the single-channel and three-channel devices. The results correspond to the number of SiNW

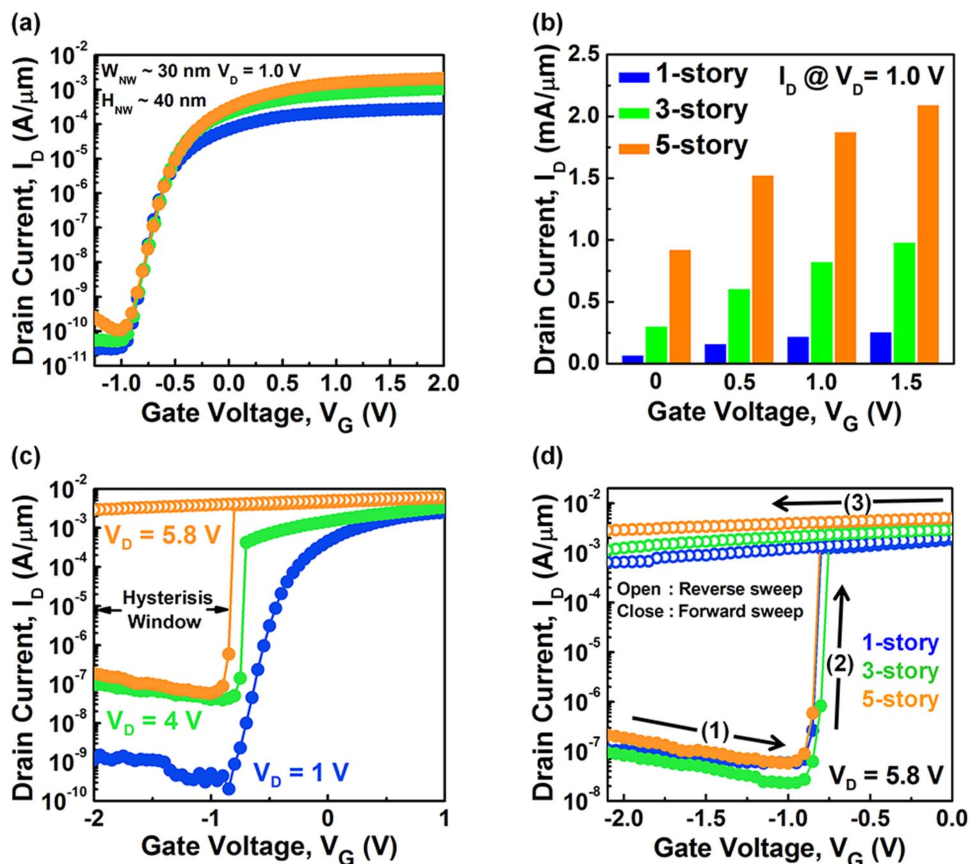

Figure 5. Electrical characteristics. (a) Transfer characteristic of each device. (b) Comparison of current drivability. (c) ZRAM operation in the five-channel device. (d) Double-sweep transfer characteristic of each device.

Downloaded on 2017-09-12 to IP 143.248.123.126 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

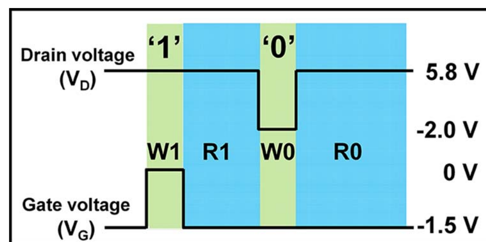

Figure 6. The bias conditions of the ZRAM operation. "W0" and "R0" mean the writing and reading operation of a data "0", respectively. Similarly, "W1" and "R1" denote such operations for a data "1".

channels, which is due to an increase of an effective channel width without an increase of a footprint area. No notable degradation of other device parameters was observed in such an enhanced transfer characteristic. Current drivability with the number of the SiNW channels is compared in Figure 5b. The double-sweep transfer characteristic of the VI-ZRAM with five-channels is shown in Figure 5c. While the device had a normal I-V characteristic at low drain voltage of 1 V, its current abruptly increased at a high drain voltage, showing a steep subthreshold slope (SS) of nearly 0 mV/dec. This result is due to hot electron-induced impact ionization,[24] which is the fundamental mechanism of the ZRAM operation. A number of holes were generated by the impact ionization and thus accumulated in the SiNW body. Finally, the accumulated holes activated a parasitic bipolar junction transistor (BJT) that consisted of the emitter (n^+-source), the base (p-SiNW body), and the collector (n^+-drain). And the parasitic BJT sustained a high I_D even when the gate as in an off state. During forward and reverse sweeps of V_G, the hysteresis curve shown in Figure 5c results from a positive feedback mechanism due to the parasitic BJT mentioned above, which is called the single transistor latch (STL) behavior.[25] Figure 5d shows the ZRAM operation of the fabricated devices. At a drain voltage that was enough to trigger impact ionization, during the forward sweep of the V_G (1), I_D rapidly increased due to the impact ionization-induced parasitic BJT (2), resulting in the retention of a high I_D at a subthreshold state during the reverse sweep of the V_G (3). As a result, bi-stable state arose at a particular V_G, e.g., -1 V for a read operation, where a difference in the current is regarded as a sensing memory window. A return to a low current state (1) is attained by removing the accumulated holes with application of a negative drain voltage (V_D). In the ZRAM operation, the procedure to trigger impact ionization (for high I_D) is a write operation of data "1", whereas removal of the accumulated holes (for low I_D) is an erase operation of data "1" and simultaneously a write operation of data "0". Figure 6 shows voltage conditions for the VI-ZRAM operation mentioned above. While activating a parasitic BJT by impact ionization, which accumulates the holes in the SiNW body, denotes the operation of "Write 1", removing the accumulated holes denotes the erase operation of data "1", simultaneously resulting in the operation of "Write 0".

The periodic write/erase operation of each device is presented in Figure 7a with a clear comparison of the sensing current ($-I_S$). Note that $-I_S$ of the VI-ZRAM is superior to that of the single channel-based ZRAM and thus is capable of identifying the data state without the sense amplifier. In terms of chip size reduction, this feature becomes increasingly important with continuous DRAM scaling. In addition, an opportunity to newly implement other versatile circuit architectures

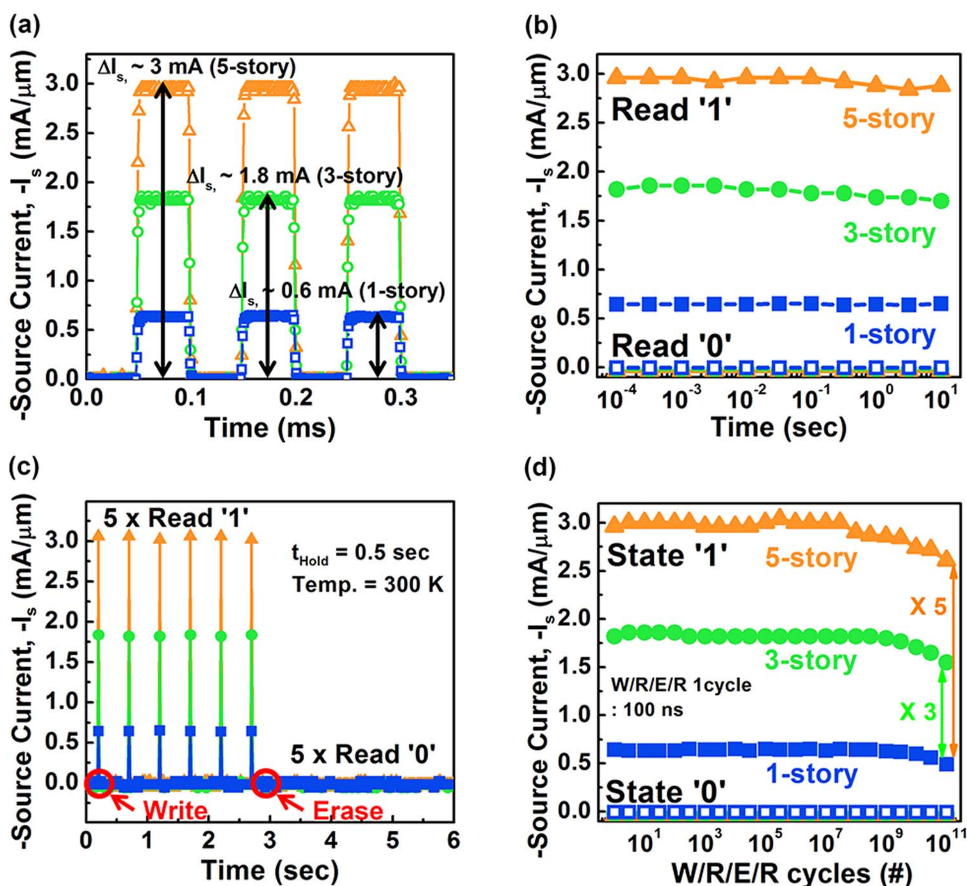

Figure 7. Comparison of each ZRAM operation. (a) Transient measurement of each ZRAM with write/read/erase operation as a function of periodic pulse time, where ΔI_S denotes a sensing memory window. (b) Retention characteristic. (c) Multi-reading operations with the periodic hold state, where t_{hold} indicates the hold time. (d) Post-cycling endurance characteristic, where W/R/E represents write, read, erase operations, respectively.

Downloaded on 2017-09-12 to IP 143.248.123.126 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

by replacing the area occupied by the sense amplifier is considerably attractive. Figure 7b shows a stable read operation of the VI-ZRAMs, when a BJT method was applied.[26] The method is effective for stable data retention with a wide sensing memory window and is beneficial to a non-destructive data read operation. In Figure 7c, multiple read operations showing a robust hold time, which is compared to the static retention time in conventional DRAM, are allowed in the VI-ZRAM without the loss of programmed data. This approach is useful for determining the period of the read operation using the BJT method, which improves the power efficiency. Figure 7d shows the switching endurance characteristic of each device. With regard to the hot carrier injection (HCI) stress-induced damage during the switching endurance test,[27] the sensing current of the zRAMs with the multi-stacked channels tend to be more degraded than that of the zRAM with a single channel. It may be ascribed to the process variability and an increase of total channel area originated from the multi-stacked configuration. Nevertheless, the VI-ZRAM still maintains a higher $-I_S$ even after iterative write/erase operation of 10^{11} cycles, compared to the zRAM with single channel. Considering the multi-stacked configuration, even with 5-story channels, this result proves the stability of the full process including the ORADEP.

Conclusions

In summary, the ZRAM with the vertically integrated multi-stacked SiNW channels was developed for further scaling of DRAM, where the ORADEP supported the completion of the device via the fabrication of stable vertical integration of the SiNW without stiction failure. The VI-ZRAM exhibited a remarkably improved sensing memory window with an increased number of integrated SiNW channels, showing a high performance without sacrifice of scalability. This result enables the removal of the sense amplifier, thereby showing the feasibility of chip size reduction, high packing density, and versatile circuit architecture. In addition, the fabricated VI-ZRAM showed a reliable data retention characteristic controlled by the base opened BJT operation and robust switching endurance. It demonstrated high stability and high completeness of the fully compatible CMOS process. With the advent of aggressive miniaturization of the DRAM, our study provides a timely milestone toward ultimate DRAM scaling.

Acknowledgments

This work was supported by the IT R&D program of MSIP/IITP. [B0126-16-1023, Development on Semi-conductor based Smart Antenna for future mobile communications].

References

1. J. M. Park, Y. S. Hwang, S.-W. Kim, S. Y. Han, J. S. Park, J. Kim, J. W. Seo, B. S. Kim, S. H. Shin, C. H. Cho, S. W. Nam, H. S. Hong, K. P. Lee, G. Y. Jin, and E. S. Jung, *Tech. Digest IEEE Electron Devices Meet.*, 26.5-1 (2015).
2. S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, *IEEE Electr. Device. L.*, **23**, 85 (2002).
3. E. X. Zhang, D. M. Fleetwood, M. L. Alles, R. D. Schrimpf, F. E. Mamouni, W. Xiong, and S. Critoloveanu, *Solid State Electron.*, **51**, 1155 (2010).
4. B.-H. Lee, M.-H. Kang, D.-C. Ahn, J.-Y. Park, T. Bang, S.-B. Jeon, J. Hur, D. Lee, and Y.-K. Choi, *Nano Lett.*, **15**, 8056 (2015).
5. D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, *P. IEEE*, **89**, 259 (2001).
6. K. Rim, J. L. Hoyt, and J. F. Gibbons, *IEEE T. Electron Dev.* **47**, 1406 (2000).
7. J.-P. Colinge, *Solid State Electron.*, **48**, 897 (2004).
8. M. C. Lemme, T. Mollenhauer, W. Henschel, T. Wahibrink, M. Baus, O. Winkler, R. Granzner, F. Schwierz, B. Spangenberg, and H. Kurz, *Solid State Electron.*, **48**, 529 (2004).
9. U. Schwalke, T. Krauss, and F. Wessely, *ECS J. Solid State Sci. Technol.*, **2**, 88 (2013).
10. N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D.-L. Kwong, *IEEE Electr. Device. L.*, **27**, 383 (2006).
11. H. Lee, L.-E. Yu, S.-W. Ryu, J.-W. Han, K. Jeon, D.-Y. Jang, K.-H. Kim, J. Lee, J.-H. Kim, S. C. Jeon, G. S. Lee, J. S. Oh, Y. C. Park, W. H. Bae, H. M. Lee, J. M. Yang, J. J. Yoo, S. I. Kim, and Y.-K. Choi, *VLSI Symp. Tech. Dig.*, 58 (2006).
12. Y.-H. Lu, P.-Y. Kuo, Y.-HL Wu, Y.-H. Chen, and T.-S. Chao, *IEEE Electr. Device. L.*, **32**, 173 (2011).
13. C. J. Barrelet, A. N. Greytak, and C. M. Liber, *Nano Lett.*, **4**, 1981 (2004).
14. L. Hood, J. R. Heath, M. E. Phelps, and B. Lin, *Science*, **306**, 640 (2004).
15. Y. Qin, Y. Liu, and Y. Wang, *ECS J. Solid State Sci. Technol.*, **5**, 380 (2016).
16. S. Kyogoku, J. Iwata, and A. Oshiyama, *A. Phys. Rev. E*, **87**, 165418 (2013).
17. B.-H. Lee, J. Hur, M.-H. Kang, T. Bang, D.-C. Ahn, D. Lee, K.-H. Kim, and Y.-K. Choi, *Nano Lett.*, **16**, 1840 (2016).
18. W. W. Fang, N. Singh, L. K. Bera, H. S. Nguyen, S. C. Rustagi, G. Q. Lo, N. Balasubramanian, and D.-L. Kwong, *IEEE Electr. Device L.*, **28**, 211 (2007).
19. C. Dupre', A. Hubert, S. Becu, M. Jublot, V. Maffini-Alvaro, C. Vizioz, F. Aussenac, C. Arvet, S. Barnola, J.-M. Hartmann, G. Garnier, F. Allain, J.-P. Colonna, M. Rivoire, L. Baud, S. Pauliac, V. Loup, T. Chevolleau, P. Rivallin, B. Guillaumot, G. Ghibaudo, O. Faynot, T. Ernst, and S. Deleonibus, *Tech. Digest IEEE Electron Devices Meet.*, 1 (2008).
20. E. Bernard, T. Ernst, B. Guillaumot, N. Vulliet, P. Coronel, T. Skotnicki, S. Deleonibus, and O. Faynot, *IEEE T. Electron Dev.*, **56**, 1243 (2009).
21. D. Sacchetto, M. H. Ben-Jamaa, G. D. Micheli, and Y. Leblebici, *ESSDERC Proceedings of the European*, 245 (2009).
22. K. D. Buddharaju, N. Singh, S. C. Rustagi, S. G. H. Teo, L. Y. Wong, L. J. Tang, C. H. Tung, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, ESSDERC 2007, DOI:10.1109/ESSDERC.2007.4430938
23. M. D. Marchi, D. Sacchetto, J. Zhang, S. Frache, P.-E. Gaillardon, Y. Leblebici, and G. D. Micheli, *IEEE T. Nanotechnol*, **13**, 1029 (2014).
24. K.-S. Shim, I.-Y. Chung, and Y. J. Park, *IEEE Electr. Device. L.*, **33**, 14 (2012).
25. M. S. Parihar, D. Ghosh, and A. Kranti, *J. Appl. Phys.*, **113**, 184503 (2013).
26. J.-W. Han, D.-I. Moon, D.-H. Kim, and Y.-K. Choi, *IEEE Electr. Device. L.*, **30**, 1108 (2009).
27. P. Heremans, R. Bellens, G. Groeseneken, and H. E. Maes, *IEEE T. Electron Dev.*, **35**, 2194 (1988).

Downloaded on 2017-09-12 to IP 143.248.123.126 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).