KAIST Approach for Submicron Device Modeling

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ABSTRACT

A new semi-empirical device modeling has been developed for modern submicron NMOS and PMOS devices. The characteristics are that it is based on device physics, that its expression is analytical for the entire bias range, and its parameter extraction is very straitforward. Our model is composed of UCCM(Unified Charge Control Model) and UMM(Universal Mobility Model) and incorporates all important physical aspects of short channel MOSFETs such as velocity saturation, channel length modulation, drain induced barrier lowering effect, sub and near threshold characteristics, and parasitic source and drain parasitic resistances. Moreover, our models guarantee the continuity of I-V and C-V as well as their derivatives, which give appreciable computation efficiency for circuit simulation. They are incorporated in our newly developed circuit simulator named AIM-spice as well as in SPICE 3, and compared with BSIM model.

I. Introduction

Semiconductor device modeling is an important component of modern semiconductor VLSI technologies in such areas as device and circuit design, to establish fabrication technology and process integration, and to provide process characterization data required to maintain proper yield, Quality Control (QC), and Quality Assurance (QA). The models help establish parameter lists for circuit simulation, design rules and, sometimes, in-house circuit simulation models. These tasks require physics-based, simple, and accurate device models. Device parameters should be extractable in an easy and unambiguous manner. This last requirement is especially important for statistical yield analysis, QC and QA. At the present time, the parameter extraction for most of the existing models relies on numerical optimization. However, such an approach makes it difficult to trace the observed electrical characteristics back to the fabrication process. Moreover, using numerical optimization, it is almost impossible to obtain statistical device data.

We try to meet challenging demands for fast computation time and guaranteed conversion combined with ease and reproducibility of parameter extraction, which of cource is based on device physics. For efficient computation time, our I-V model is continuous for the entire gate and drain bias. We have also developed new analytical ; which allow us to incorporate parasitic resistanc device models. Direct incorporation of the resistances is necessary for deep submicron devic their resistance values become comparable to tl channel resistance. This is also very crucial bo frequency analog and digital circuits, especiall device sizes and for statistical and reliability mod extrinsic models lead to enormous savings of com This is crucial for simulating large circuits.

II. UCCM(Unifed Chrage Control Model UMM(Universal Mobility Model).

The following UCCM's for short channel N PMOS are shown to describe subthreshold, near threshold regions simultaneously using an analytic as follows[1-5],

$$V_{GS}-(V_{tho}-\sigma V_{ds})-\alpha V_F \approx \eta V_T \ln(n_s/n_0) + a\cdot(n_s -$$

$$-V_{GS}+(V_{tho}-\sigma V_{ds})+\alpha V_F \approx \eta V_T \ln(p_s/p_0) + a\cdot(p_s$$

Figures 3, 4 and 7 show the comparison of the V_{GS} characteristics between the measurement usin method and calculated results using UCCM for lo MOSFET, whose parameters are extracted as in Fig.2[2]. Our UCCM is also compared with classi contol model in Fig.7, which shows that the la accuarate enough for thin gate dielectric.

We also find from accurate device physics[3 electron(hole) mobility was found to be universally on the

$$F_{eff} \cong \frac{C_{ox}}{2\varepsilon_{Si}}(V_{GS}+V_{th}) \quad \text{for electron,}$$

$$F_{eff} \cong \frac{C_{ox}}{3\varepsilon_{Si}}(V_{GS}+2V_{tho}-6\phi_F) \quad \text{for hole.}$$

The fonctional dependence is found to be simple as

$$\mu_\perp = \mu_0 - \mu_1 (V_{GS}+V_{th}) \quad \text{for electron,}$$

$$\frac{1}{\mu_\perp} = \frac{1}{\mu_0} - \frac{1}{\mu_1}(V_{GS}+2V_{tho}) \quad \text{for hole.}$$

Figures 5 and 6 shows the accuracy of our UMM. I our expression is different from the conventional dependencies, which have been widely used. Figur that our long channel I-V model developed using U UMM agree extremely well with the experimental n

III. Unified I-V model for short channel MOSFETs[4,5].

The following unified I-V medels are developed for short channel devices in the triode region.

$$I_{DS} = \frac{1}{R_n} \frac{a \cdot n_S V_{DS} - \frac{\alpha^*}{2} V_{DS}^2}{\sqrt{V_{DS}^2 + V_L^2}} \quad \text{for nMOS,}$$

$$I_{DS} = -\frac{1}{R_n} \frac{a \cdot p_S V_{DS} + \frac{\alpha^*}{2} V_{DS}^2}{V_L - \zeta V_{DS}} \quad \text{for pMOS.}$$

In the saturation region, we have

$$I_{D(SAT)} = I_{DSAT}\left\{1 + \frac{V_L V_\lambda}{V_{DSAT}^2 + V_L^2} \times \ln\left[\sqrt{1 + \left(\frac{V_{DS} - V_{DSAT}}{\theta V_\lambda}\right)^2} - \frac{V_{DS} - V_{DSAT}}{\theta V_\lambda}\right]\right\} \quad \text{for nMOS,}$$

$$I_{D(SAT)} = I_{DSAT}\left\{1 + \frac{V_\lambda}{V_L - V_{DSAT}} \times \ln\left[\sqrt{1 + \left(\frac{V_{DS} - V_{DSAT}}{\theta V_\lambda}\right)^2} + \frac{V_{DS} - V_{DSAT}}{\theta V_\lambda}\right]\right\} \quad \text{for pMOS.}$$

In short channel devices, the parasitic source and drain resistances are very important. Moreover, the parameters are extracted from the extrinsic I-V characteristics. We expand our I-V model for the extrinsic MOSFETs. Here we make the following approximations.

$$V_{GS} = V_{gs} - I_{DS} \cdot R_S,$$

$$V_{DS} = V_{ds} - I_{DS} \cdot (R_S + R_D).$$

Substituting the above relationships into intrinsic unified current-voltage model , we can obtain the 2nd-order analytical equation for the drain current. And by solving this equation, we obtain the extrinsic I-V characteristics.

IV. Parameter extraction and I-V characterization

Our parameter extraction starts from the experimental determination of saturation voltage and current. In deep saturation region, our model is written by the following equation

$$I_{DSAT} \frac{\partial V_{ds}}{\partial I_{DSAT}} \cong \frac{V_{DSAT}^2 + V_L^2}{V_L V_\lambda} (V_{ds} - V_{dsat}) \quad \text{for nMOS,}$$

$$I_{DSAT} \frac{\partial V_{ds}}{\partial I_{DSAT}} \cong \frac{V_L - \zeta V_{DSAT}}{V_\lambda} (V_{ds} - V_{dsat}) \quad \text{for pMOS.}$$

From this results, as shown in Fig. 9 and 10, (V_{dsat}, I_{DSAT}) can be extracted from linear extrapolation of $I_{DSAT} \frac{\partial V_{ds}}{\partial I_{DSAT}}$ versus V_{ds} plot. Moreover, the parameter V_λ is extracted from the slope of this plot.

It is not difficult to show that the drain current can be written as follows at saturation point.

$$\frac{V_{GT}}{V_{DSAT}} = \frac{\alpha(2+\gamma)}{2} + R_n^2 \frac{\gamma I_{DSAT}^2}{V_{GT} V_{DSAT}} \quad \text{for nMOS,}$$

$$\frac{V_{GT}}{V_{DSAT}} - \frac{I_{DSAT}}{WC_{ox}} \frac{L_{eff}}{V_{DSAT}^2} \frac{1}{\mu_S} = \frac{\alpha}{2} + \zeta R_n \frac{I_{DSAT}}{V_{DSAT}} \quad \text{for pMOS.}$$

The parameters α, v_{sat} and ζ can be extracted from F 11 and 12.

The measured and calculated I_{DS}-V_{GS} characte for our devices are compared in Figures 13-18. calculation has been done using parameters fror parameter extraction technique. As can be seen in figures, the agreement between the measured an calculated curves is excellent for the entire regi MOSFET operation. In particular, the subthreshold reg reproduced quite accurately.

The calculated output resistances are shown in Fi 19 and 20, which are continuous throughout the entire of the drain voltage and in good agreement witl experimental data.

IV. Unified C-V model

Figures 21-23 show the comparison of our C-V m based on UCCM and compared with the popular BSIM with our experimental data. Our new model includes th charge and it is more accurate in the subthreshold regir is based on the Quasi-Static Approximation (QSA) provides very smooth *C-V* expressions for all gate, and bulk biases, from subthreshold to the above-thre regime, and from the linear to the saturation regime. same time, our model is simple enough to be useful for simulation.

A detailed description of this new *C-V* model is giv Rho and Lee in this conference. Their idea was to rela bulk charge to the threshold voltage variation described body plots. This allows us to express the MOS capacit in terms of the parameters γ_N and Γ_N which can read obtained from the threshold voltage measurements. inversion charge is determined by integrating the U equation. Once the inversion charges is obtained, "partitioned" between the source and drain contacts, with 60 % of the inversion charge going to the sourc 40 % going to the drain at the saturation point independent device capacitances are calculated a derivatives of the source and drain inversion charges ar bulk charge with respect to the terminal voltages.

V. Conclusion

Based on unified charge control model, univ mobility model and field-velocity relationship, we deve new unified current-voltage model for subm MOSFETs.The characteristics are that it is based on d physics, that its expression is analytical for the entire range, and its parameter extraction is very straitforward model is composed of UCCM(Unified Charge Co Model) and UMM(Universal Mobility Model) incorporates all important physical aspects of short ch MOSFETs such as velocity saturation, channel l modulation, drain induced barrier lowering effect, sul near threshold characteristics, and parasitic source and parasitic resistances. Our experimental data for n- a MOSFETs with effective submicron gate lengths agree with the calculated results for different substrate biases values of the extracted parameters also agree well with independent measurement results and they are very phy The simplicity as well as the accuracy of our model parameter extraction methods indicate that they are suitable for circuit simulation and statistical pr characterization. They are incorporated in our n

developed circuit simulator named AIM-spice as well as in SPICE 3, and compared with BSIM model.

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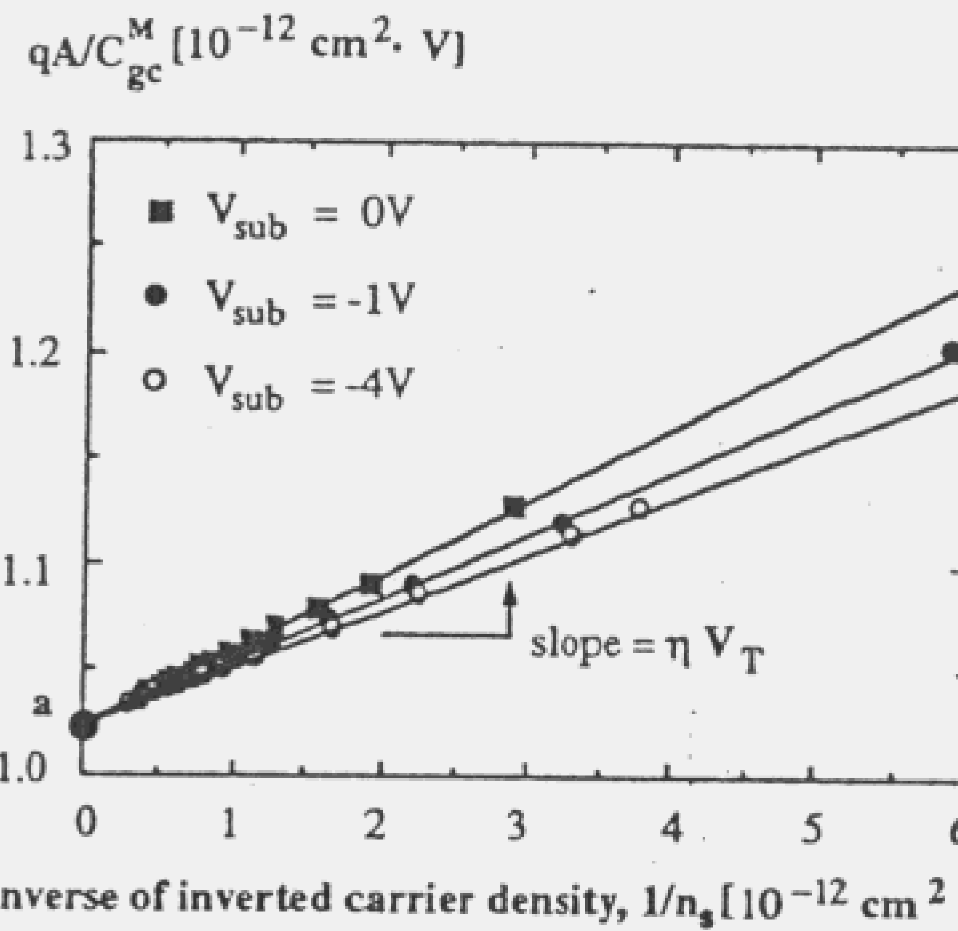

Fig. 1 qA/C$^M_{gc}$ vs. 1/n_s plot. η and a can be found from the slope and y-intercept, respectively.

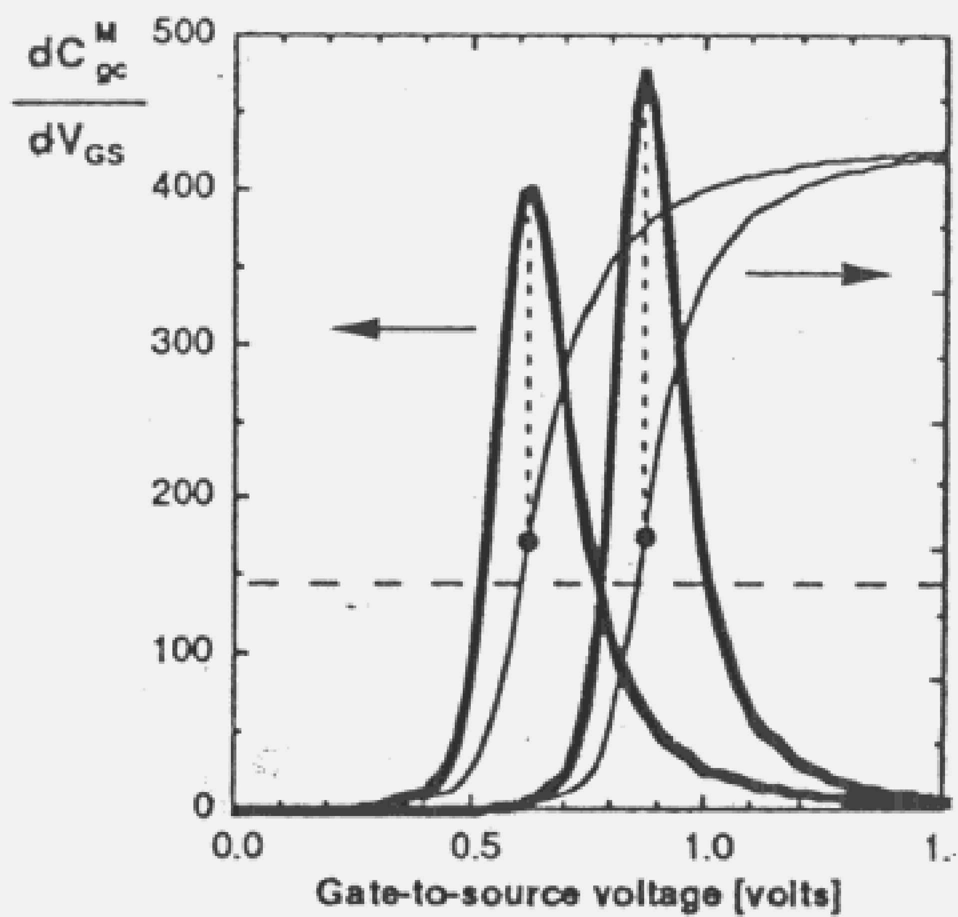

Fig. 2 Experimental C$^M_{gc}$ and dC$^M_{gc}$/dVgs vs. Vgs for Vsub=0, -1V. This shows Vgs where of dCgc/dVgs is maximum almost conici Vgs where Cgc=Cgc,max/3.

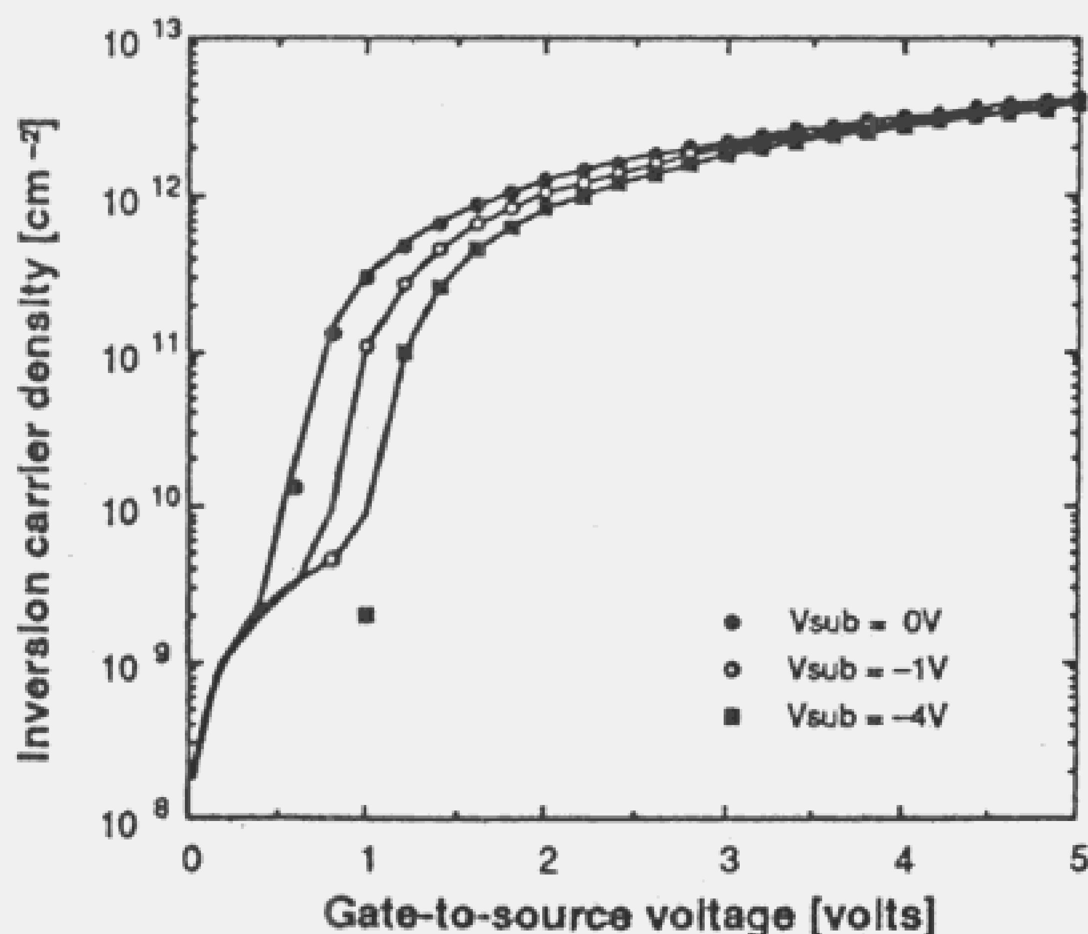

Fig. 3 Comparison of n_s (log scale) vs. Vgs chacteristics experimetal measurement (solid lines) and UCCM(dots)

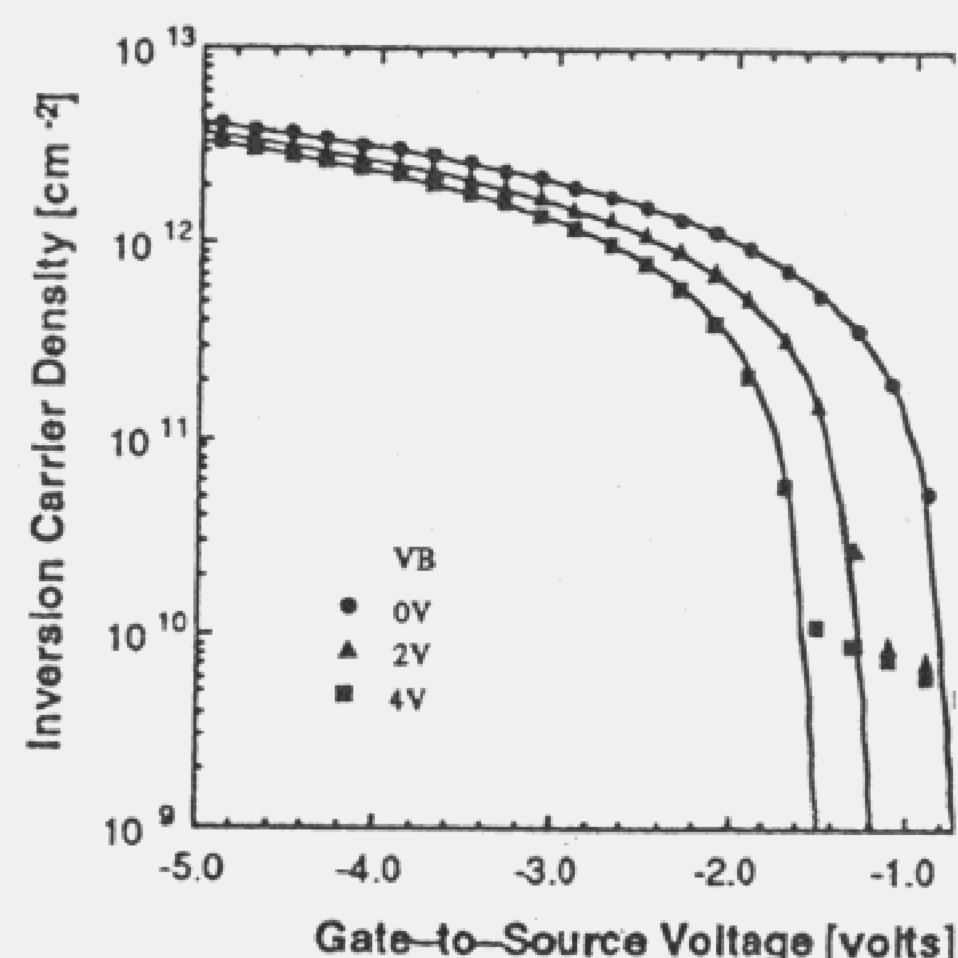

Fig. 4 Comparison of p_s (log scale) vs. Vgs chacte experimetal measurement (solid lines) and UCCM(closed dots)

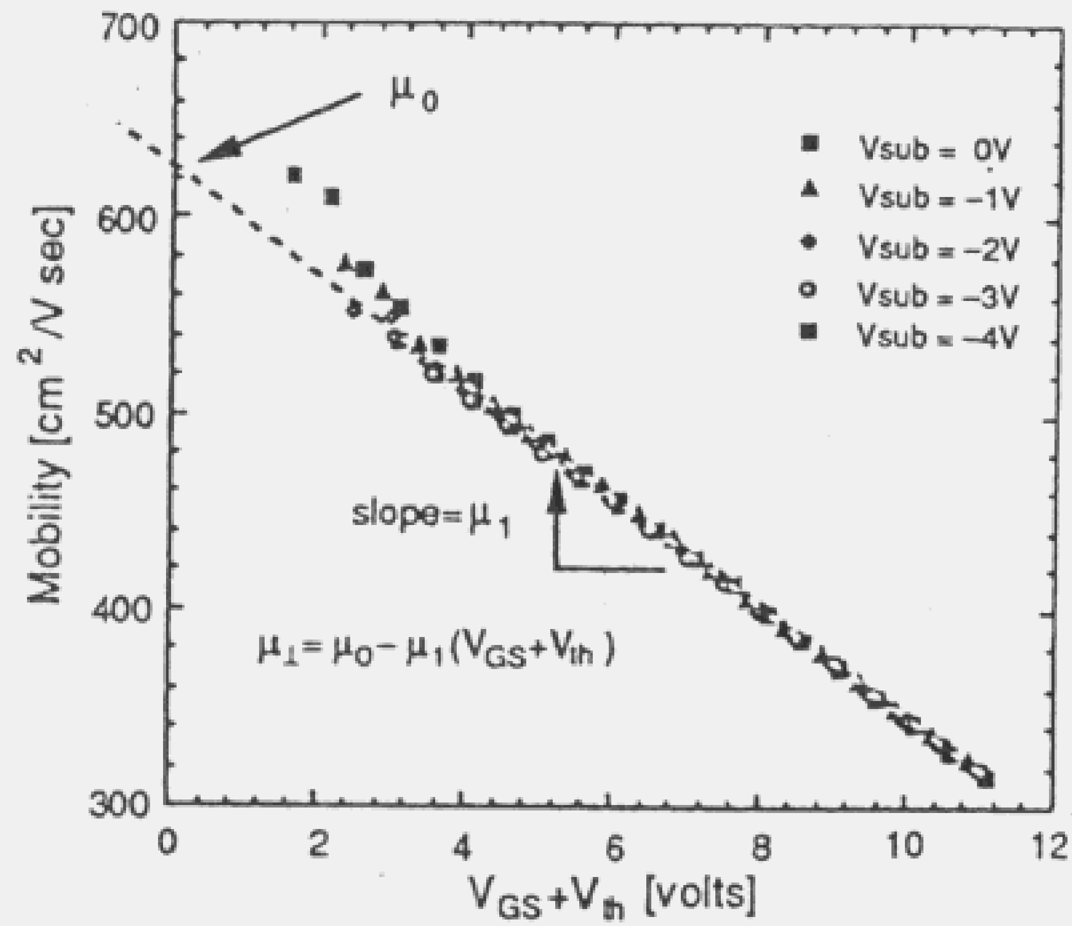

Fig. 5 Experimetally measured mobility vs. Vgs+Vth plot for different substrate bias, showing univeral, and linear dependece of $\mu_\perp$ on Vgs+Vth for nMOS.

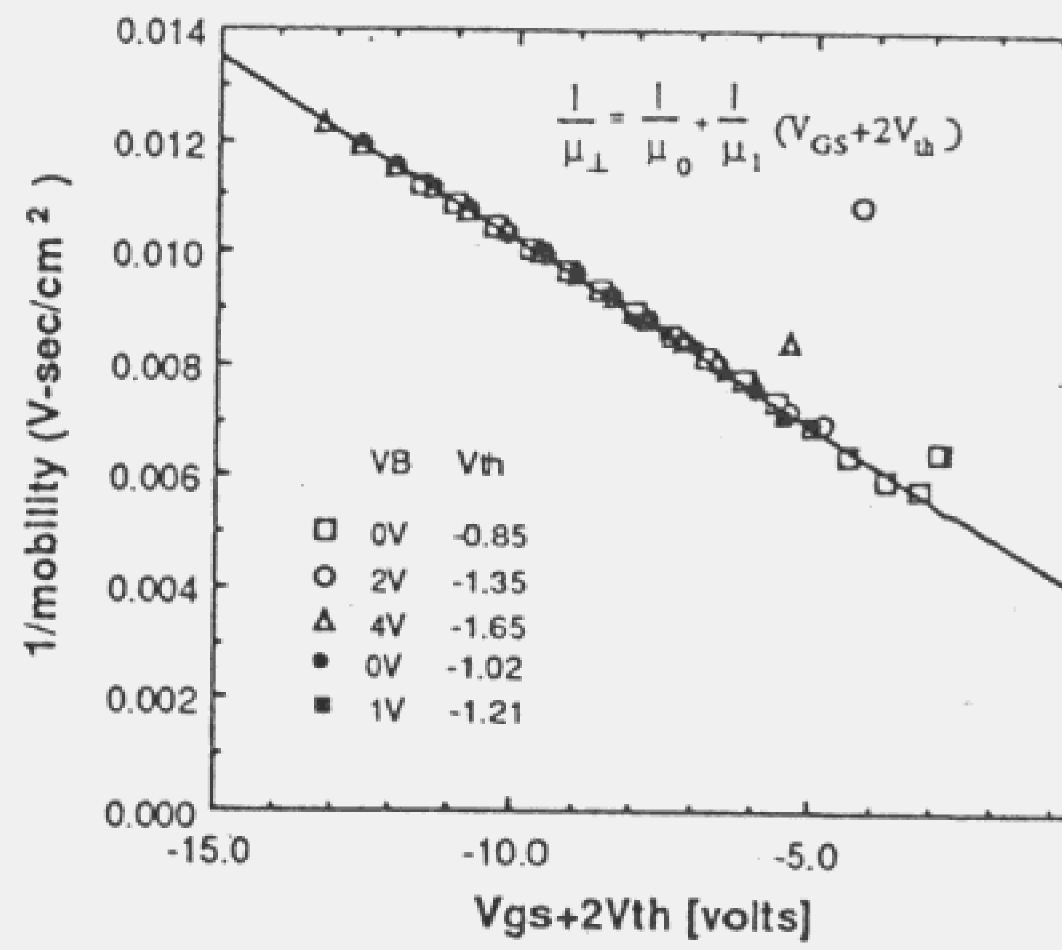

Fig. 6 Experimetally measured 1/mobility vs. Vgs+2Vth plot for different substrate bias, showing univ eral, and linear dependece of $1/\mu_\perp$ on Vgs+2Vth for pMOS.

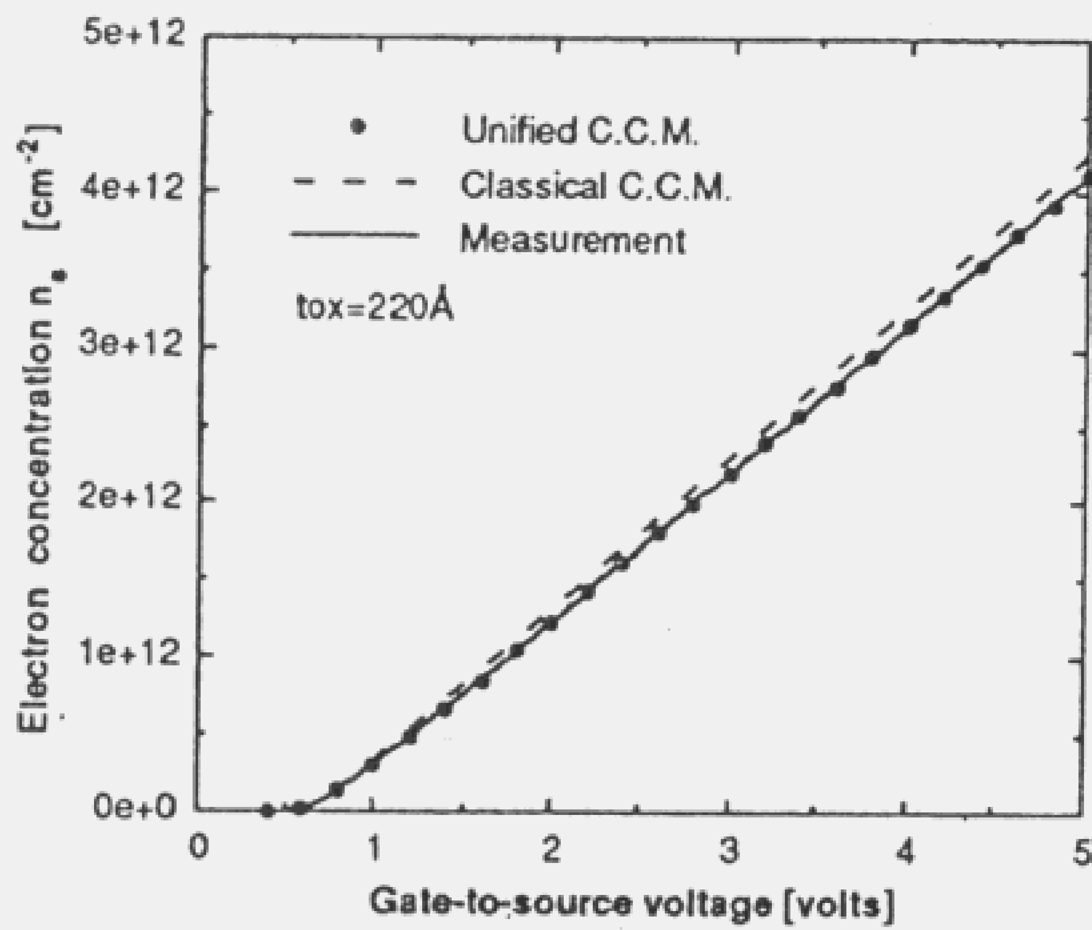

Fig. 7 Comparison of n_s (linear scale) vs. Vgs characteristics between experimental measurement (solid line) and UCCM (solid dots) and classical charge control model for Vsub=0V, nMOS.

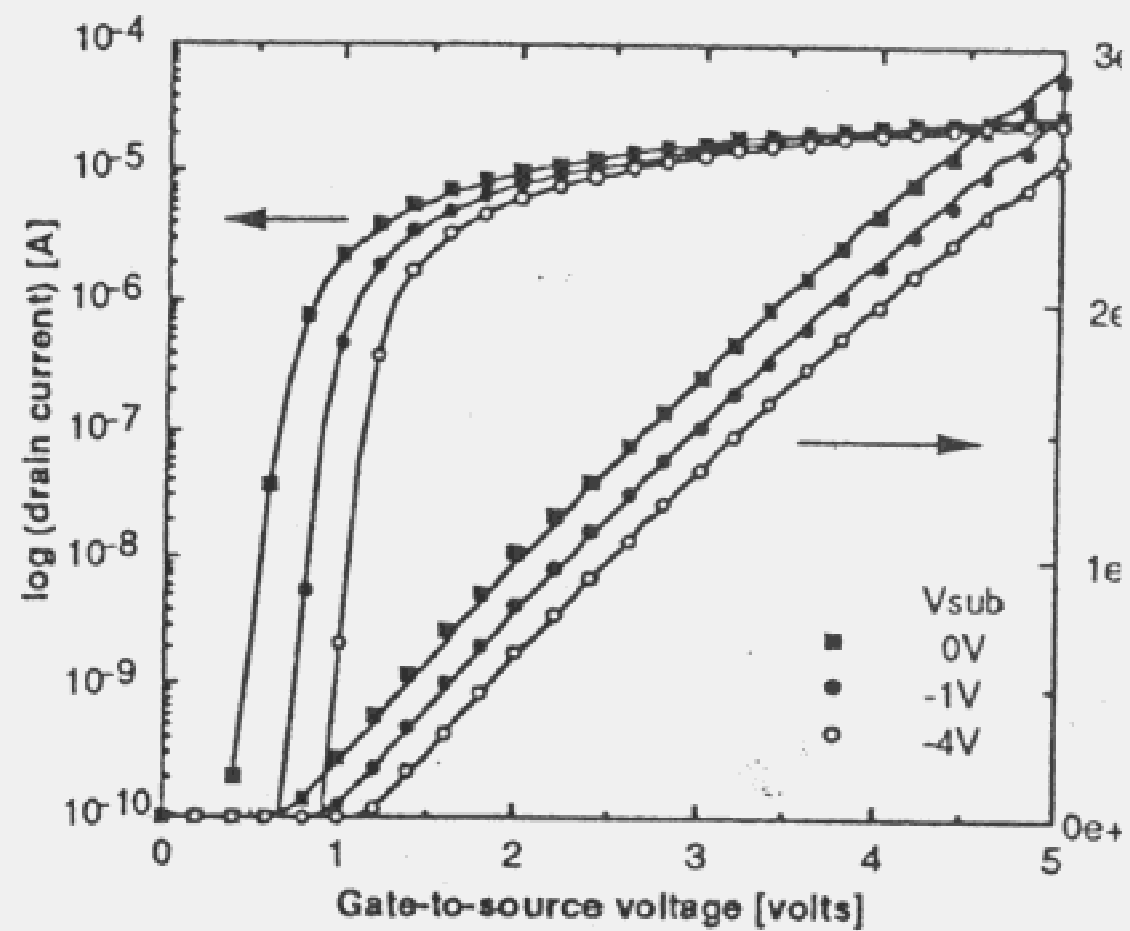

Fig. 8 Drain current vs. Vgs characteristics at linear region (vds=0.1V) for 20μm/20μm nMOS. Points: experimental measurement. Solid lines: I-V model.

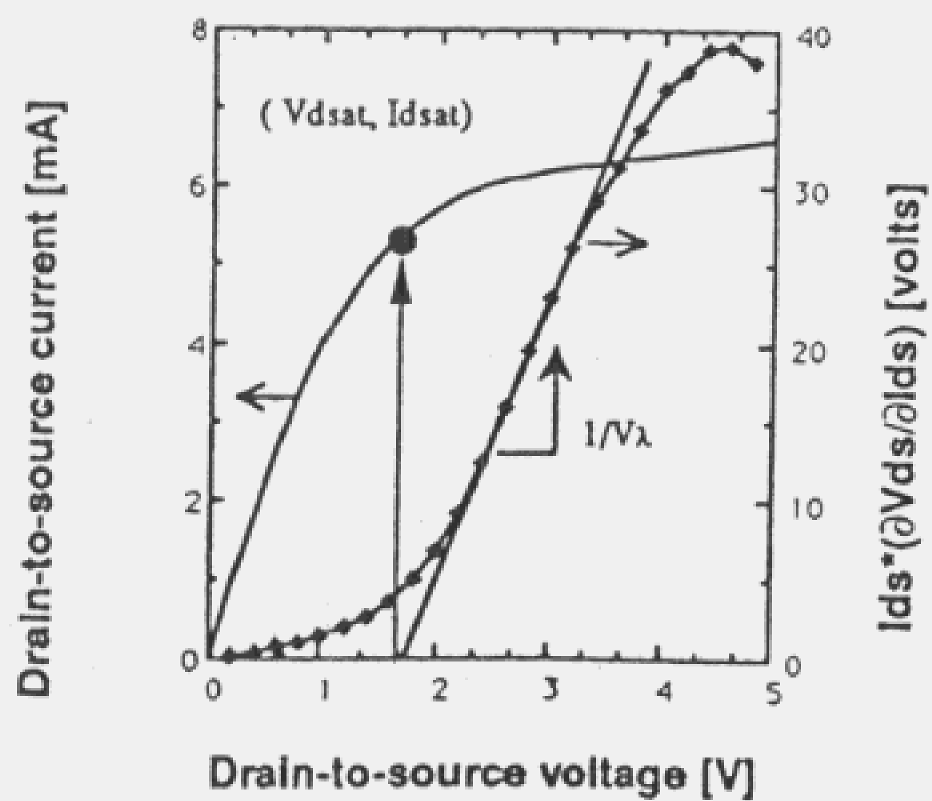

Fig. 9 An example of experimetal determination of saturation voltage and current from Ids*(dVds/dIds) vs. Vds plot for nMOS.

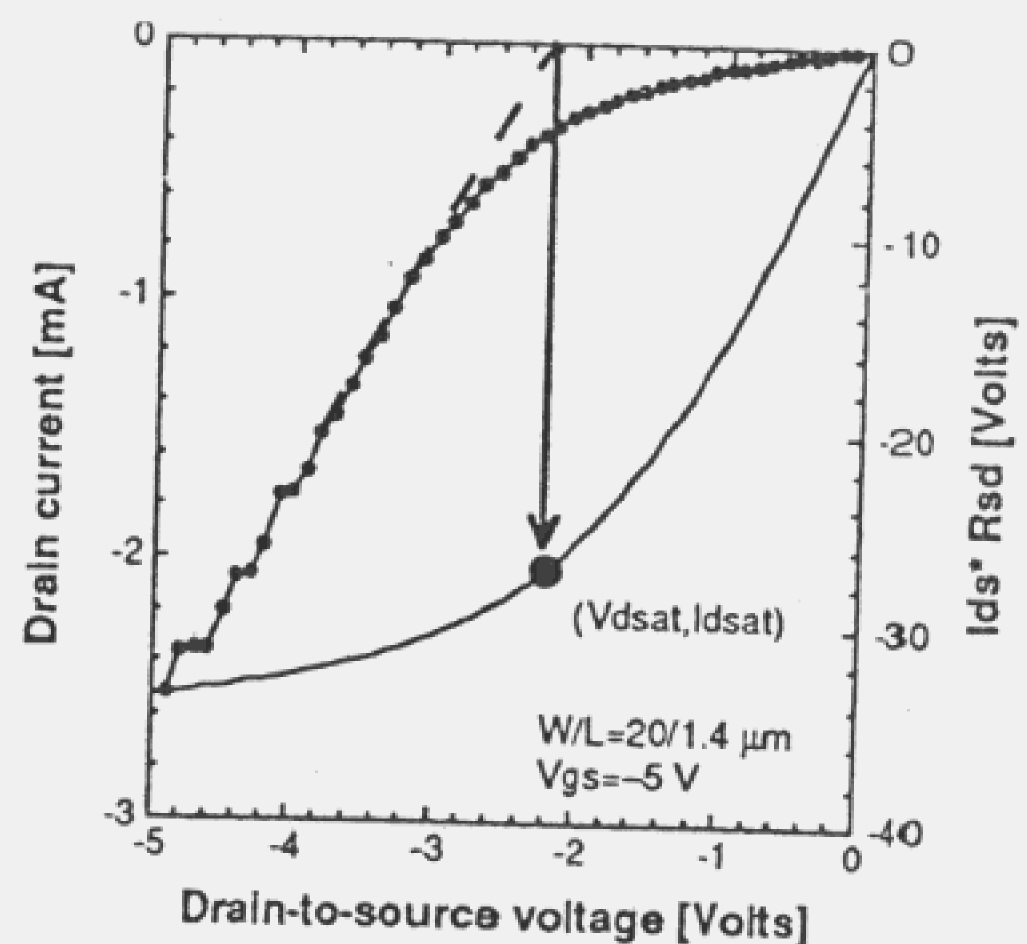

Fig. 10 An example of experimetal determination of saturation voltage and current from Ids*(dVds/dIds) vs. Vds plot for pMOS.

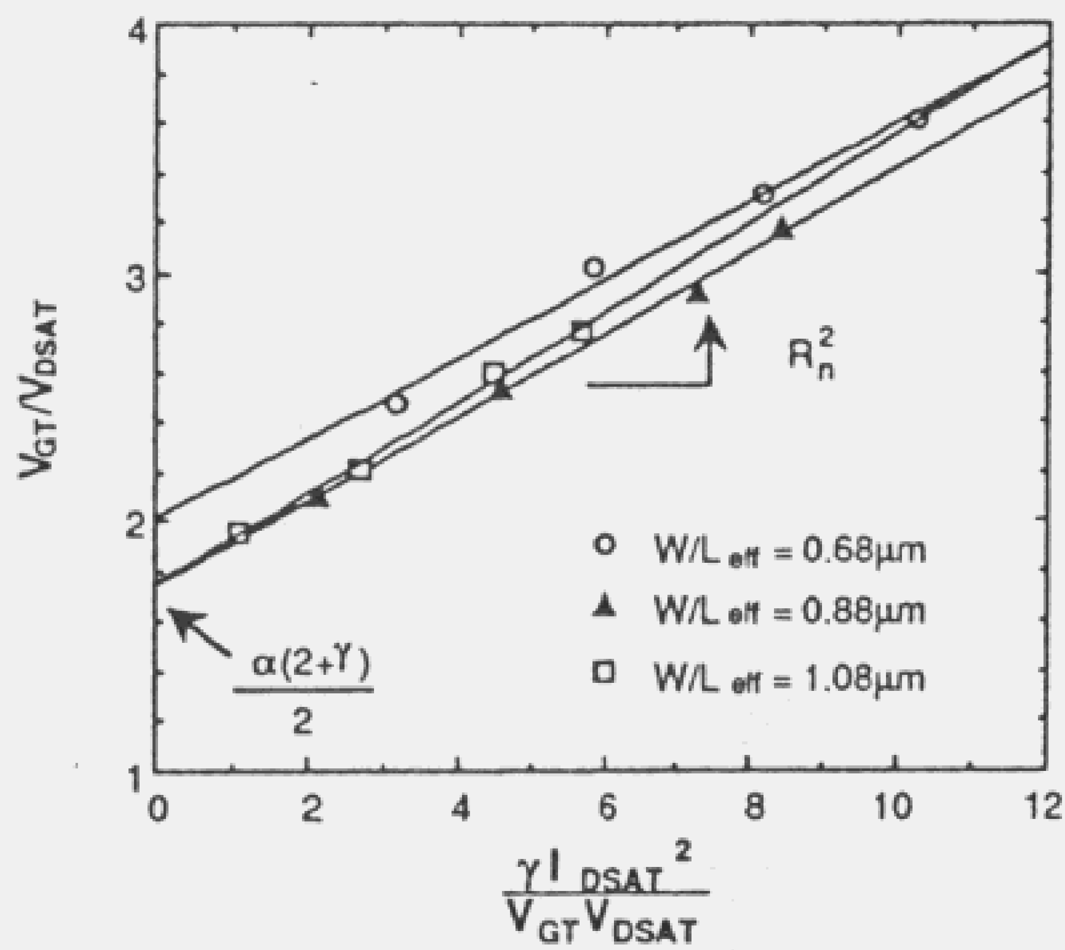

Fig. 11 $\alpha(2+\gamma)/2+R_n^2*\gamma^2*Idsat/(Vgt*Vdsat)$ vs. Vgt/Vdsat plot for determination of paramter α and γ of nMOS.

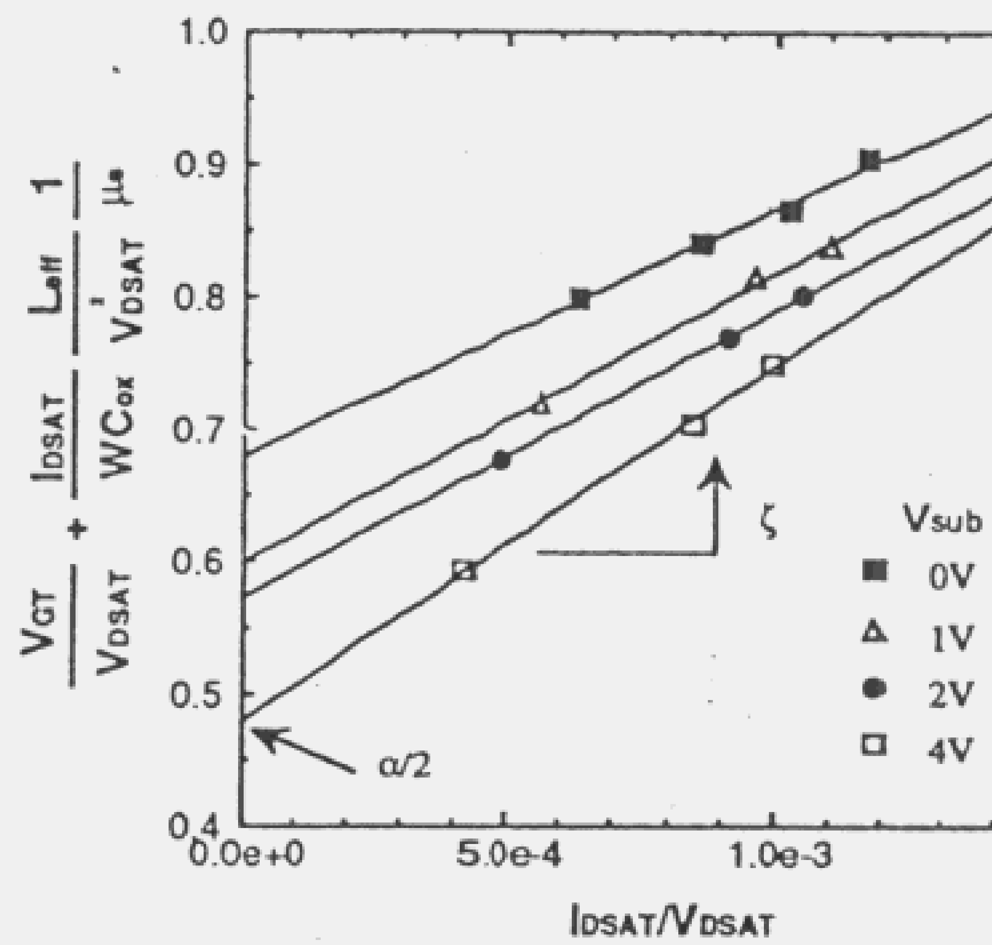

Fig. 12 Vgt/Vdsat_Idsat/WCox*Leff/$Vdsat^2$*1/μs vs. Idsat/Vdsat plot for determination of paramter α and ζ of pMOS.

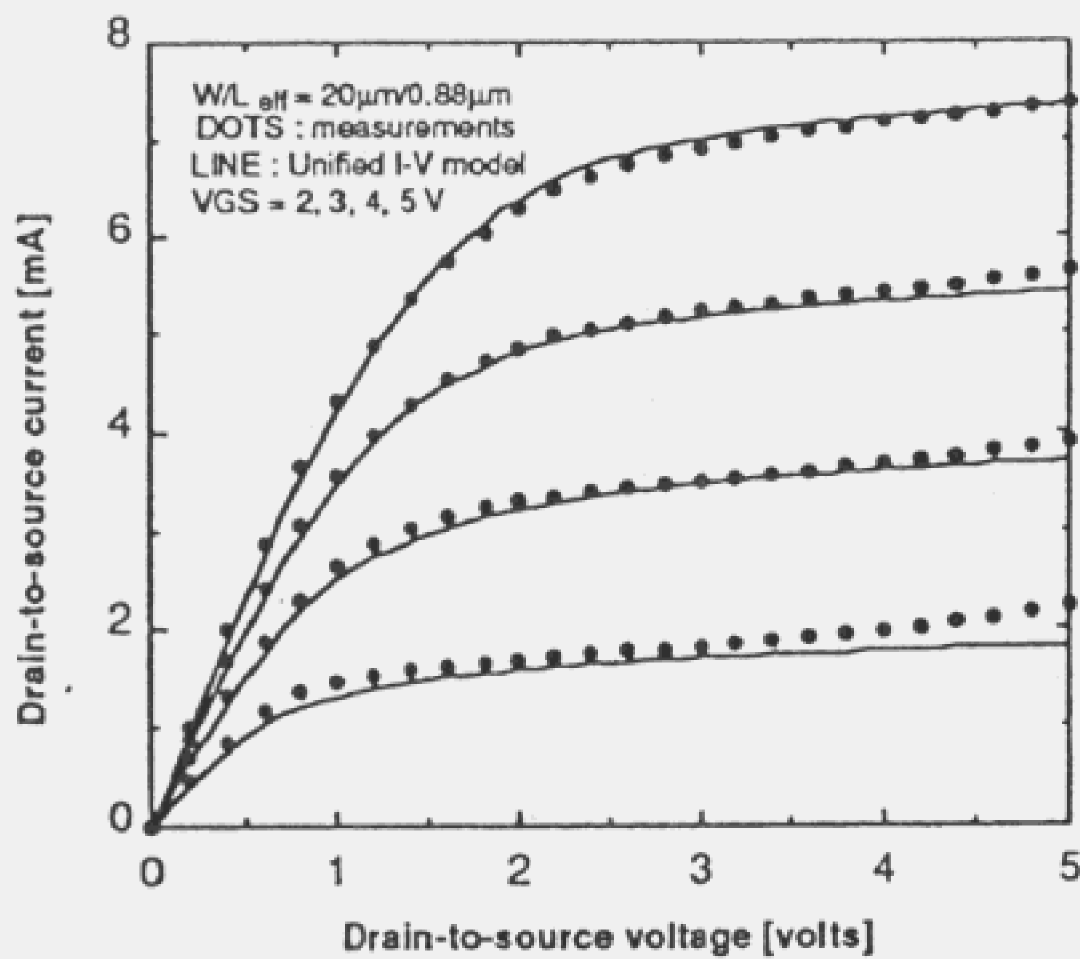

Fig. 13 Measured(dots) and aclculated(solid lines) Ids vs. Vds characteristics at strong inversion region for nMOS.

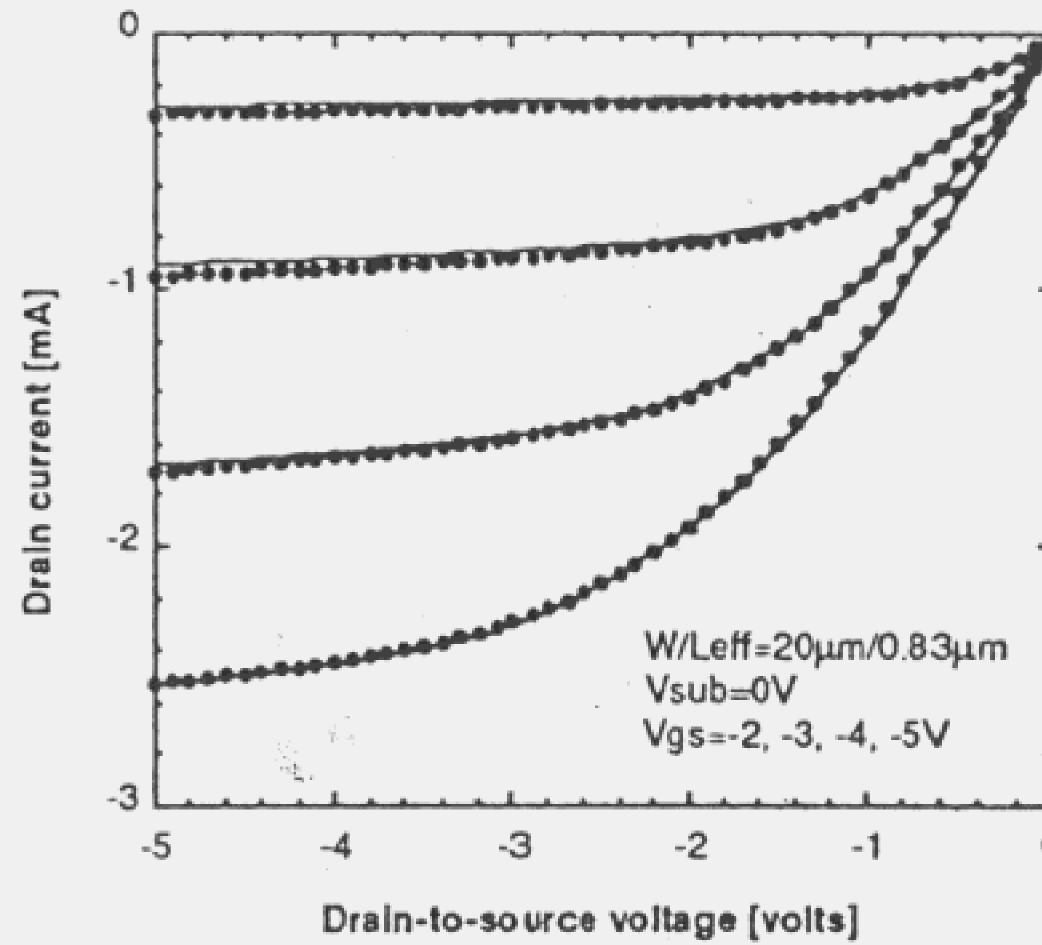

Fig. 14 Measured(dots) and aclculated(solid lines) Ids vs. Vds characteristics at strong inversion region for pMOS.

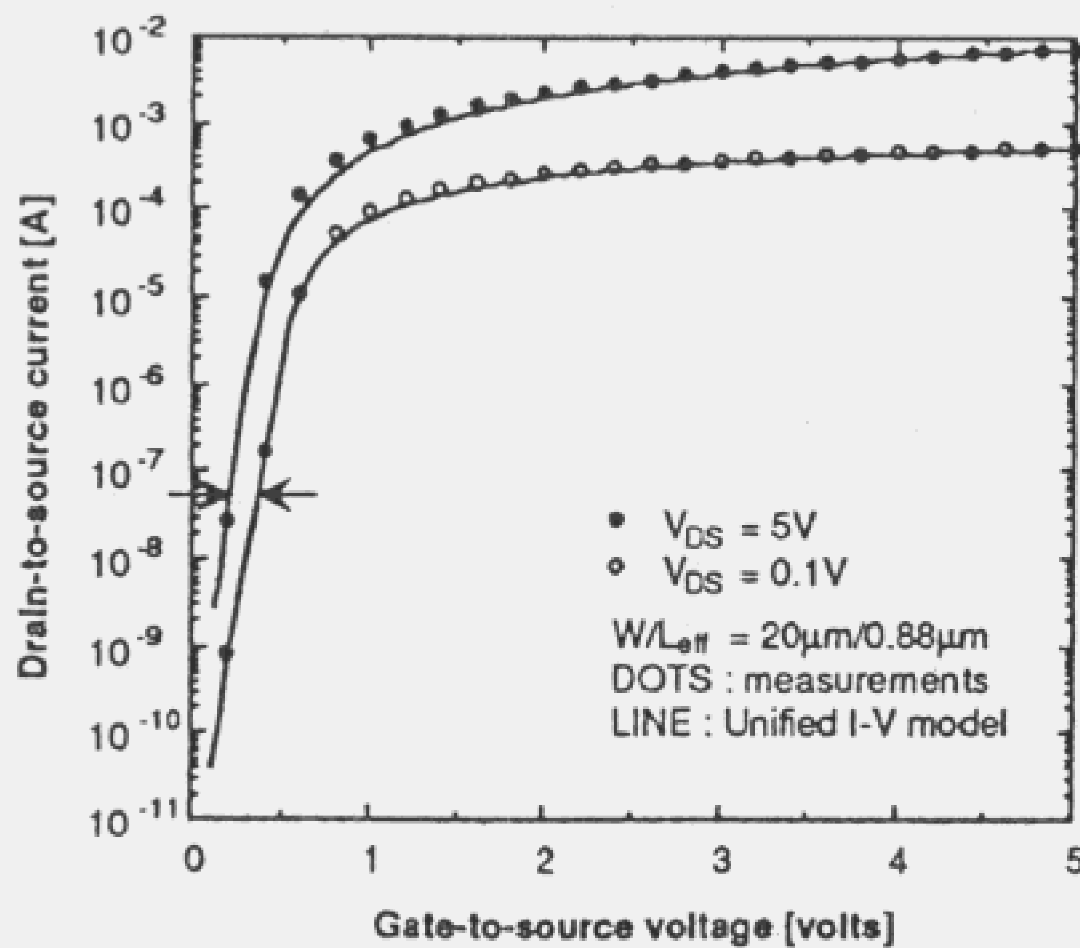

Fig. 15 Measured(dots) and calculated(solid lines) Ids-Vgs characteristics at Vds=0.1V, 5V for nMOS.

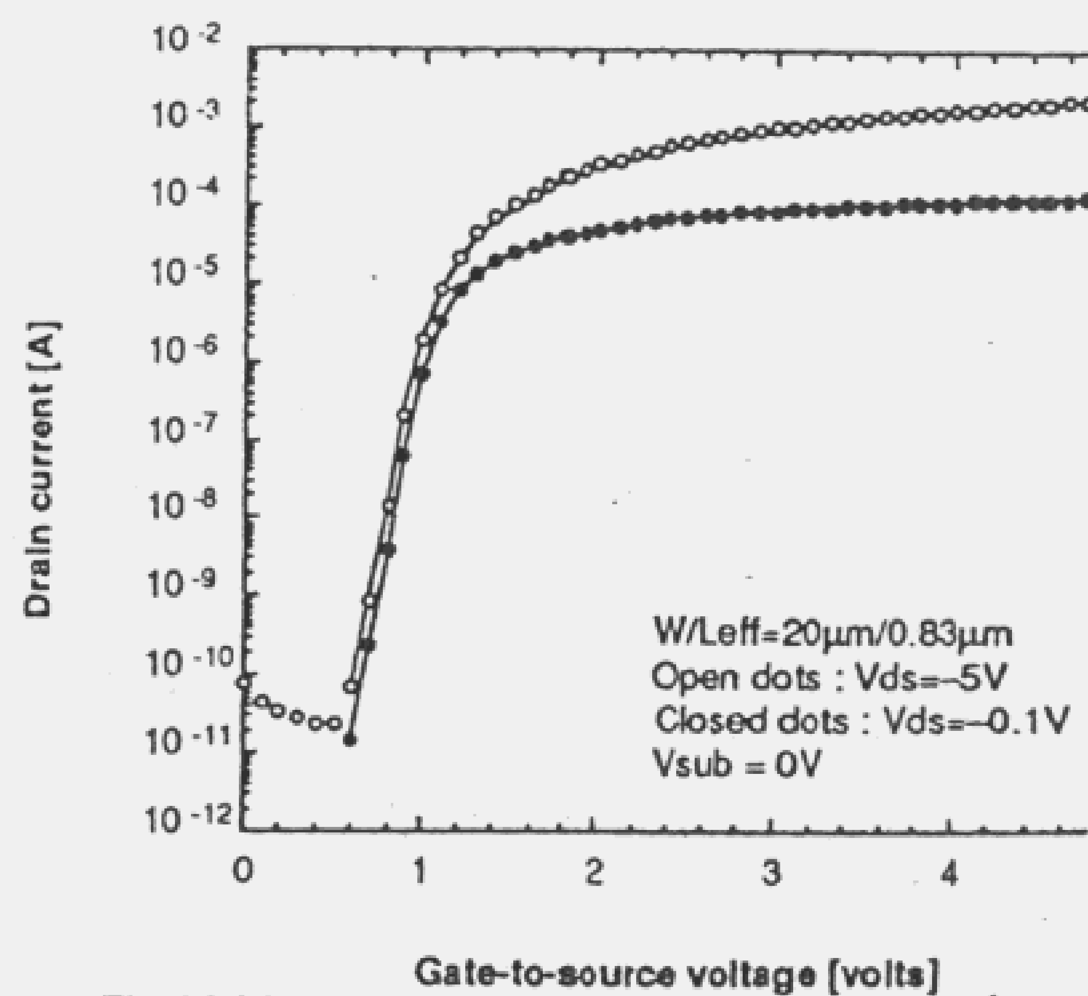

Fig. 16 Measured(dots) and calculated(solid lines) Ids-Vgs characteristics at Vds=-0.1V, -5V for pMOS.

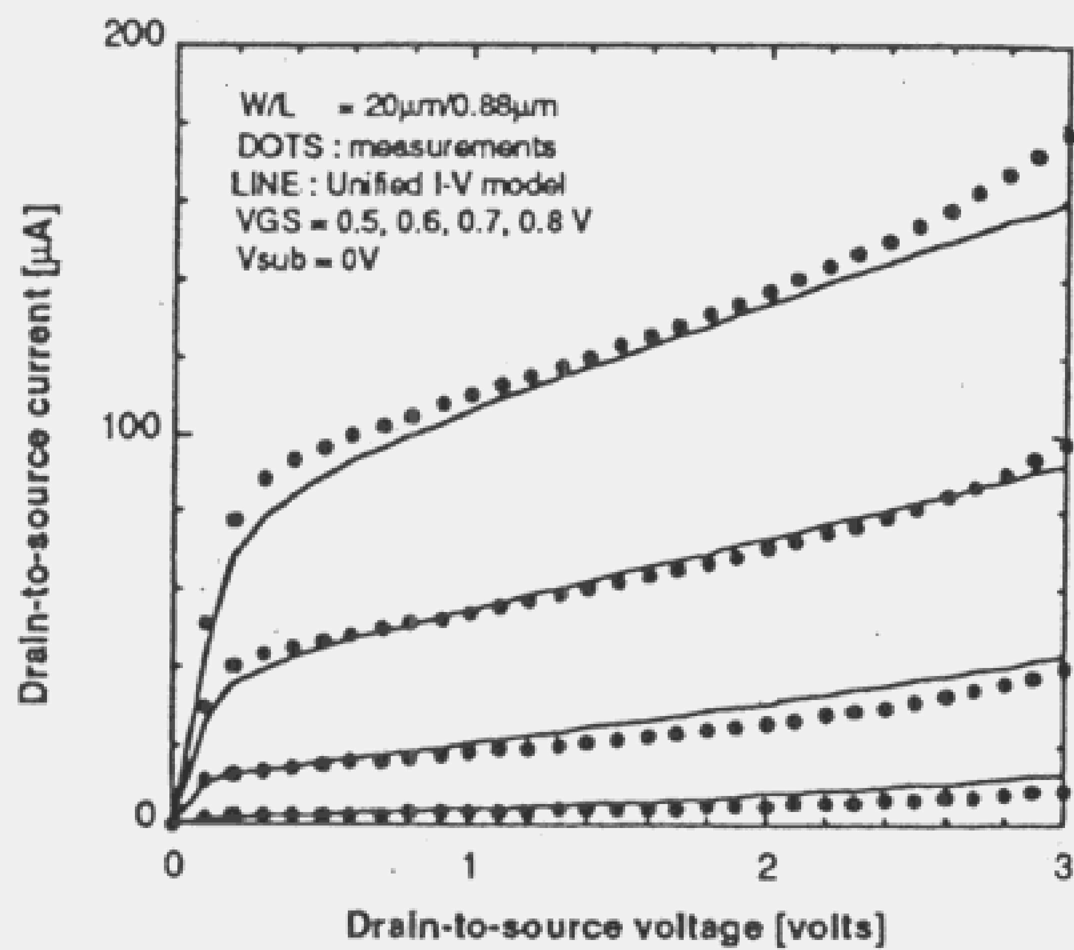

Fig. 17 Measured(dots) and calculated(solid lines) Ids-Vds characteristics at near threshold region for nMOS.

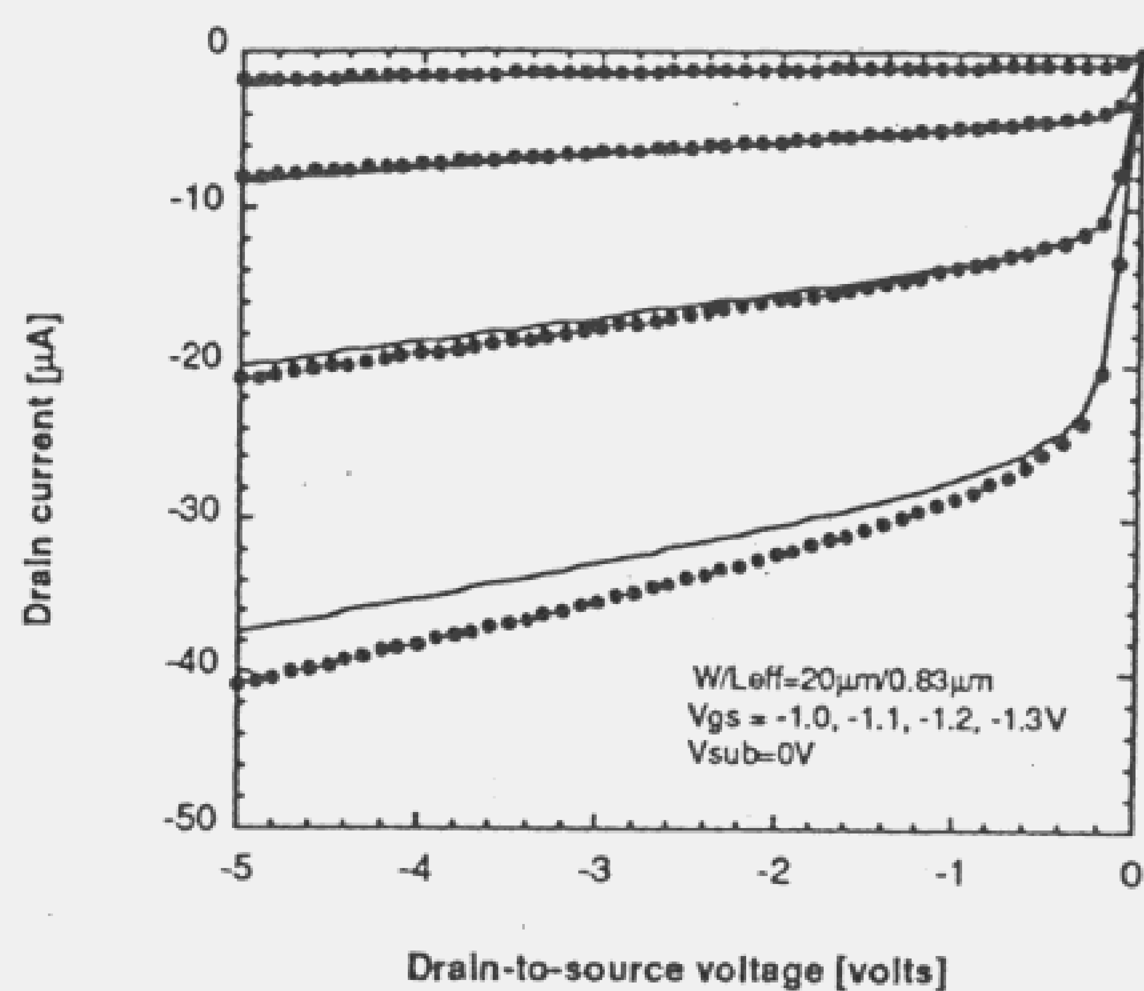

Fig. 18 Measured(dots) and calculated(solid lines) Ids-Vds characteristics at near threshold region for pMOS.

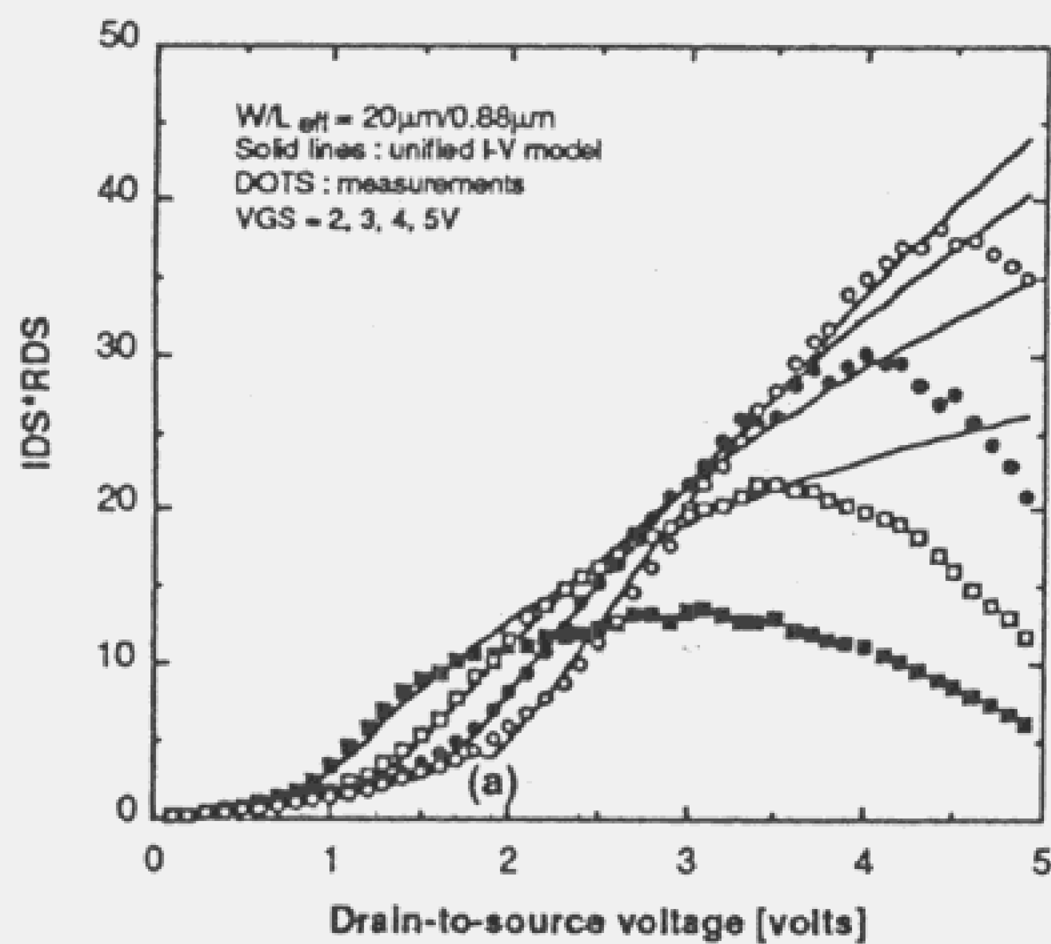

Fig. 19 dVds/dIds*Ids vs. Vds plot for nMOS.
Dots: experimental measurements
Solid lines: calcuration results.

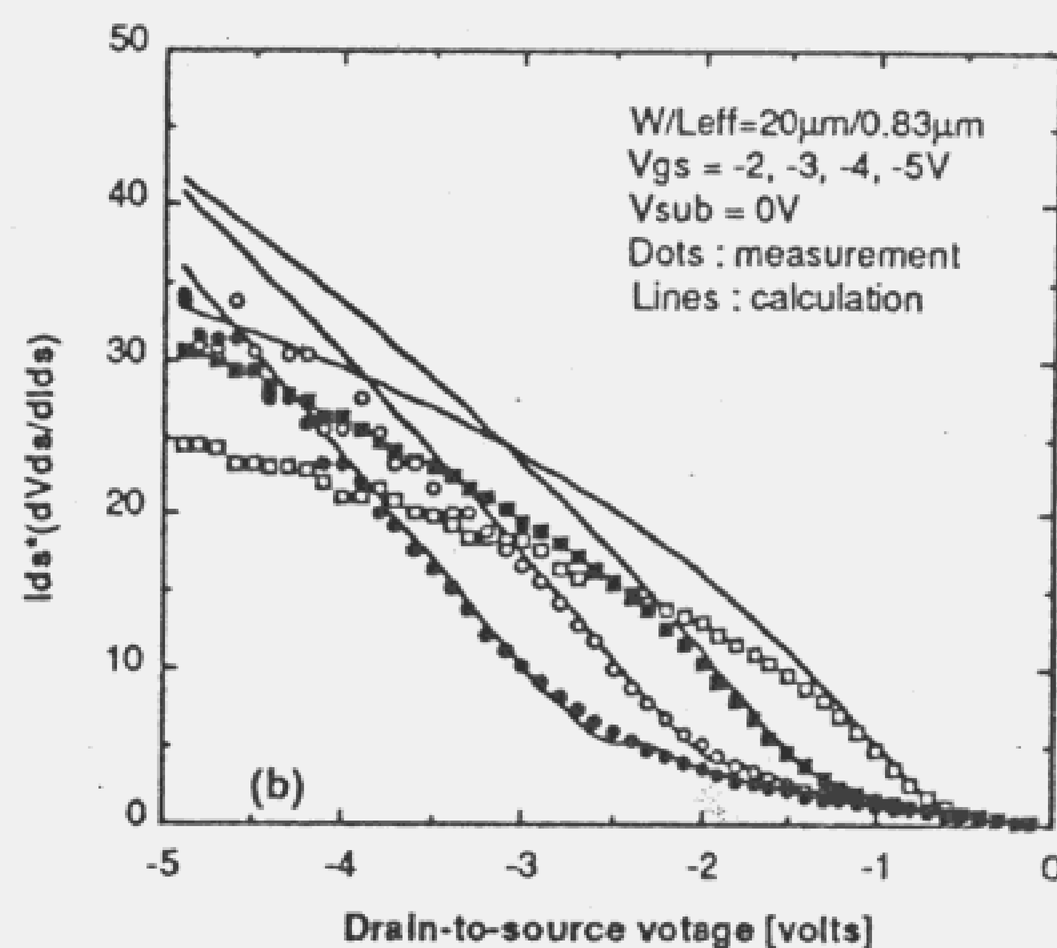

Fig. 20 dVds/dIds*Ids vs. Vds plot for nMOS.
Dots: experimental measurements
Solid lines: calcuration results.

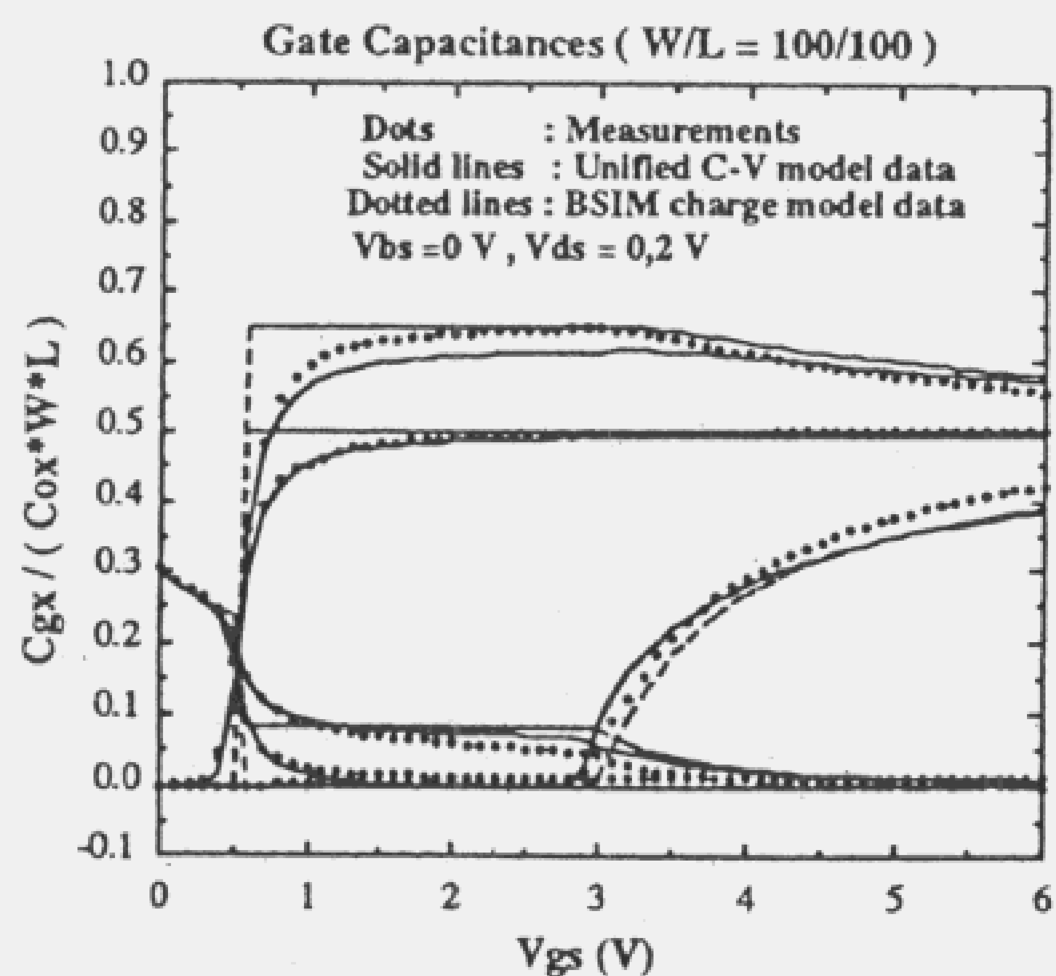

Fig. 21 Comparison of nomarlized gate capacitances vs. Vgs characteristics for different drain bias (Vbs=0V). Points: measurements. Solid lines: Unified C-V model. Dotted lines: BSIM model.

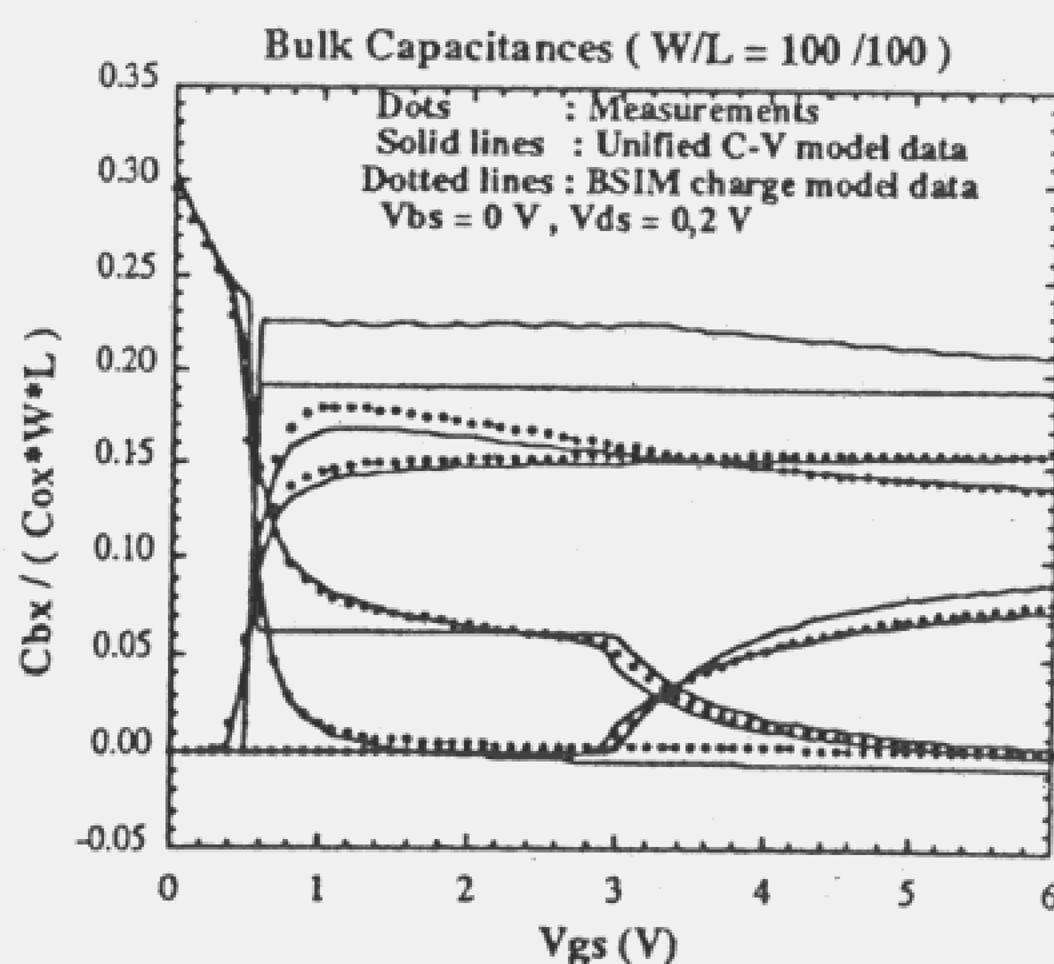

Fig. 22 Comparison of normalized bulk capacitances vs. Vgs characteristics for different drain bias. (Vbs=0V) Points: measurements. Solid lines: unified C-V model. Dotted lines: BSIM model.