Design Methodology of Baseband Analog Chain to Maximize a Spurious Free Dynamic Range for ATSC Terrestrial and Cable Digital TV Tuner

Kuduck Kwon, Hong-Teuk Kim, and Kwyro Lee, *Member*, IEEE

Abstract — *This paper presents a fully integrated tunable CMOS baseband analog (BBA) chain optimized for advanced television systems committee (ATSC) terrestrial and cable digital TV tuner integrated circuits (ICs). To maximize the spurious free dynamic range (SFDR) of the BBA chain for both standards, the design guideline is introduced with respect to the optimized allocation of the gain of each block. The bandwidth is selectable from 3 MHz, 3.5 MHz, or 4 MHz. Fabricated in a 0.18-μm CMOS process, it provides a minimum input referred noise density of 15.5 nV/$\sqrt{Hz}$ with 62 dB gain and out-of-channel output referred third-order intercept point (OIP3) of 33 dBm, while it drains an average current of 89 mA from 3.3 V. The total chip area is 1 mm $\times$ 1.2 mm.*[1]

Index Terms — Baseband analog (BBA), ATSC, cable, terrestrial, spurious free dynamic range (SFDR), tuner

I. INTRODUCTION

Digital television broadcasting has gained more attention in recent years mainly due to the demand for high quality contents and regulation for digital broadcasting. In most of the countries, the existing analog TV system will be replaced with digital TV system. In response to this major transition all around the world, demand for low-cost CMOS single chip tuner integrated circuits (ICs) suitable for digital TV system will increase. For advanced television systems committee (ATSC) terrestrial and cable digital TV standards, a broad VHF/UHF frequency band from 48 MHz to 862 MHz is used, where hundreds of broadcasting channels simultaneously come into the digital TV tuner. From each desired channel's perspective, the channels outside the desired one are referred to as the interferers. Therefore, in RF front-end, those unwanted channels need to be filtered out to obtain good receiver characteristic. However, it is hard to integrate a highly linear and low noise filter that operates in the VHF/UHF band. Hence, the linearity requirement of the digital TV tuner is stringent.

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Kuduck Kwon is with the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, Daejeon, Korea (e-mail : kaistdong@gmail.com)

Hong-Teuk Kim is with the LG Electronics Institute of Technology, Seoul, Korea

Kwyro Lee is with the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, Daejeon, 305-701 Korea, and also with the LG Electronics Institute of Technology, Seoul, Korea (e-mail : krlee@ee.kaist.ac.kr)

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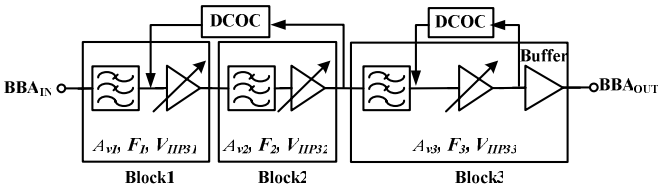


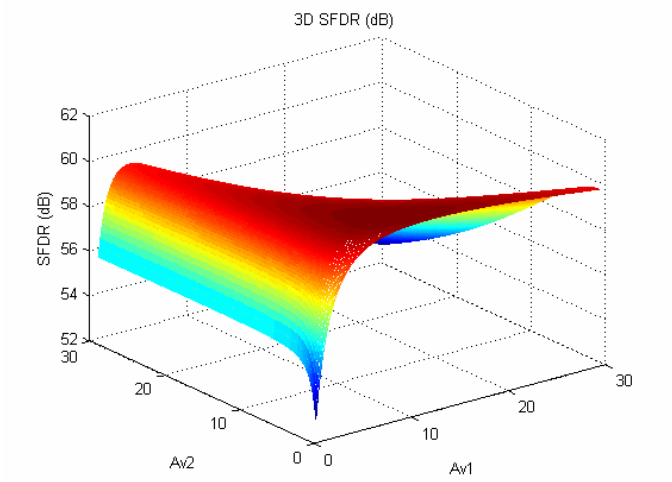
Fig. 1. Block diagram of the BBA chain (A_v is voltage gain, F is noise factor and V_{IIP3} is input referred third-order intercept point).

Especially, the performance of the baseband analog (BBA) chain has a large impact on the performance of the whole receiver such as the noise figure (NF) and linearity since most of the channels come to the BBA chain almost without filtering and the nature of broadband channels limits an allowable gain of the RF-frond end. In fact, the BBA chain must itself be low noisy so as not to degrade the overall receiver noise figure, while sustaining sufficient linearity not to get affected by inter-modulation distortion products generated by large adjacent channels and interferers. Therefore, it is crucial to optimize the spurious free dynamic range (SFDR) of the BBA chain for the receiver performance.

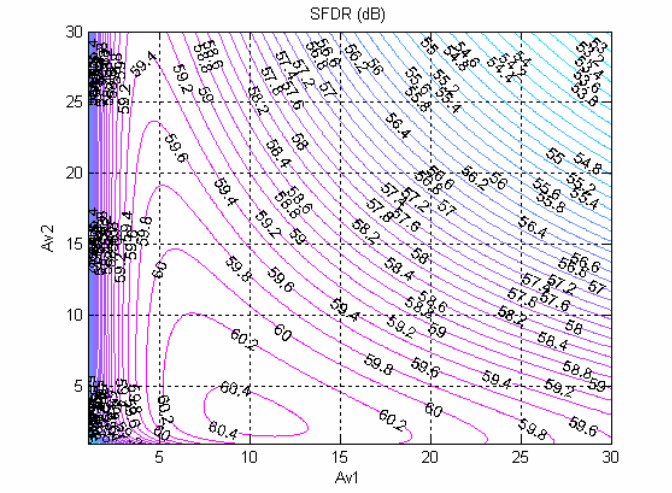
In this paper, a highly integrated CMOS BBA chain, which is optimized with respect to SFDR, is designed and implemented in 0.18-μm CMOS technology. Section II describes the design methodology to maximize SFDR of the BBA chain for ATSC terrestrial and cable digital TV tuner ICs. The detailed circuit designs in the BBA chain are discussed in section III. Section IV reports the experimental results of the BBA chain. Finally, section V concludes this paper.

II. DESIGN METHODOLOGY OF BBA CHAIN TO MAXIMIZE SFDR FOR ATSC TERRESTRIAL AND CABLE DIGITAL TV TUNER

To maximize SFDR in the BBA chain, the NF should be minimized whereas the input referred third-order intercept point (IIP3) has to be as high as possible. However, for a given current consumption, there is a trade-off between the noise performance and the linearity in the BBA chain. Accordingly, to optimize SFDR of the BBA chain, alternation of filter stages with amplifier stages [1] and the optimum allocation of the gain of each block will be the appropriate choice [2]. In addition, for a given amount of current, scaling of the input impedance level and power consumption of the blocks in the BBA chain is required. The NF of the first block dominates



(a)



(b)

Fig. 2. (a) 3-dimensional contour and (b) 2-dimensioanl contour for SFDR of the BBA chain in ATSC terrestrial with changes of A_{v1} and A_{v2}.

the overall NF of the BBA chain, so its input impedance level must be very low. Therefore, by providing more current to the first block, both NF and linearity performance can be improved simultaneously. As the stage goes on, the input impedance level becomes higher and power consumption gets lower.

A. Optimal SFDR in ATSC Terrestrial

Since our system requires 75dB attenuation at the sampling frequency of ADC of 25MHz in the anti-aliasing low-pass filter (LPF), a 6th-order LPF is selected. The BBA chain is modeled as the three cascaded blocks shown in Fig. 1. Each block consists of a biquad LPF and a programmable gain amplifier (PGA).

In ATSC terrestrial, broadcasting channels are scattered apart from 48MHz to 862MHz, where $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ products are dominant in deciding the third order distortion. The expression of SFDR which is related by the noise figure, linearity, and gain of each block can be expressed in ATSC terrestrial as follows [3]:

$$SFDR_{ATSC} = \left(\frac{IIP_{3,casc}}{F_{casc}\ KTB}\right)^{\frac{2}{3}} \propto DR_{casc}^{\frac{2}{3}} . \tag{1}$$

$SFDR_{ATSC}$ is proportional to the cascaded dynamic range of the BBA chain, DR_{casc} and it is expressed as

$$\begin{aligned}\frac{1}{DR_{casc}} &= \frac{F_{casc}}{V_{IIP3,casc}^2} \\ &= (F_1 + \frac{F_2 - 1}{A_{V1}^2} + \frac{F_3 - 1}{A_{V1}^2 A_{V2}^2})(\frac{1}{V_{IIP31}^2} + \frac{A_{V1}^2}{V_{IIP32,Fil}^2} + \frac{A_{V1}^2 A_{V2}^2}{V_{IIP33,Fil}^2}) \\ &\cong \frac{F_1}{V_{IIP31}^2} + \frac{F_2}{V_{IIP32,Fil}^2} + \frac{F_3}{V_{IIP33,Fil}^2} + \frac{F_1 A_{V1}^2}{V_{IIP32,Fil}^2} + \frac{F_1 A_{V1}^2 A_{V2}^2}{V_{IIP33,Fil}^2} \\ &\quad + \frac{F_2}{A_{V1}^2 V_{IIP31}^2} + \frac{A_{V2}^2 F_2}{V_{IIP33,Fil}^2} + \frac{F_3}{A_{V1}^2 A_{V2}^2 V_{IIP31}^2} + \frac{F_3}{A_{V2}^2 V_{IIP32,Fil}^2} \\ &= \frac{1}{DR_1} + \frac{1}{DR_2} + \frac{1}{DR_3} + \alpha\end{aligned} \tag{2}$$

and

$$\begin{aligned}\alpha = &\frac{F_1 A_{V1}^2}{V_{IIP32,Fil}^2} + \frac{F_1 A_{V1}^2 A_{V2}^2}{V_{IIP33,Fil}^2} + \frac{F_2}{A_{V1}^2 V_{IIP31}^2} + \frac{A_{V2}^2 F_2}{V_{IIP33,Fil}^2} \\ &+ \frac{F_3}{A_{V1}^2 A_{V2}^2 V_{IIP31}^2} + \frac{F_3}{A_{V2}^2 V_{IIP32,Fil}^2}\end{aligned} , \tag{3}$$

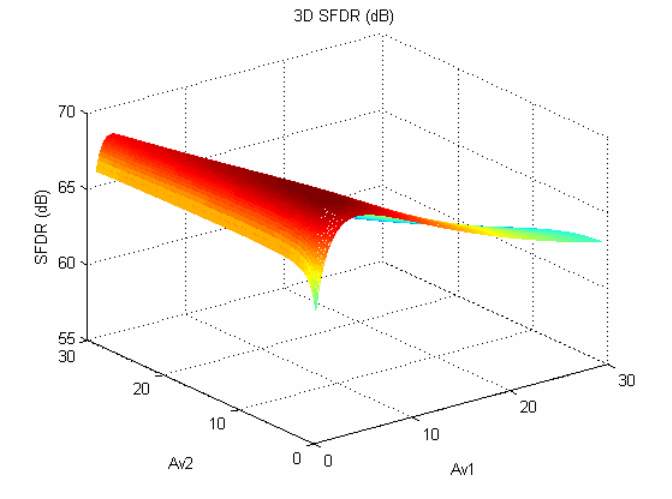
where A_{Vi} is the voltage gain of the ith block, F_i is the noise factor of the ith block, and V_{IIP3i} is the input referred third-order intercept point of the ith block. $V_{IIP32,Fil}$ and $V_{IIP33,Fil}$ are the input referred third-order intercept points including filtering effect of proceeding LPFs in the BBA chain [4] and can be expressed as:

$$V_{IIP32,Fil} = \frac{V_{IIP32}}{\sqrt{r_{11}^2 r_{12}}} = \frac{V_{OIP32}}{A_{V2}\sqrt{r_{11}^2 r_{12}}} \tag{4}$$

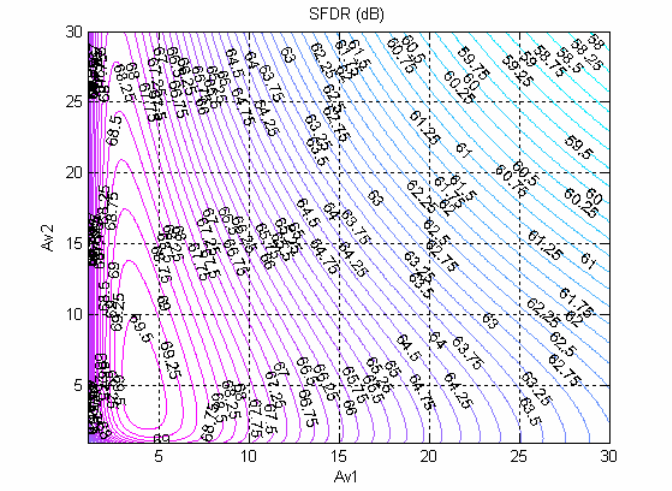
and

$$V_{IIP33,Fil} = \frac{V_{IIP33}}{\sqrt{r_{11}^2 r_{12} r_{21}^2 r_{22}}} = \frac{V_{OIP33}}{A_{V3}\sqrt{r_{11}^2 r_{12} r_{21}^2 r_{22}}} . \tag{5}$$

In these expressions, V_{OIP3i} is the output referred third-order intercept point of the ith block and r_{i1} and r_{i2} ($r_{i1} < 1$ and $r_{i2} < 1$) are rejection rates of the LPF of the ith block when two tones at the frequency of ω_1 and ω_2 are applied to the BBA chain, respectively. From (2), A_{V1} and A_{V2} have a dominant effect on DR_{casc} whereas A_{V3} is directly decided by the value of A_{V1} and A_{V2} given the overall gain of BBA chain. As a result, the appropriate allocation of the gain of each block in the BBA chain is the most important factor in maximizing SFDR. When the partial differential of α to A_{V1} and A_{V2}, $\partial\alpha/\partial A_{V1}$ and $\partial\alpha/\partial A_{V2}$,



(a)



(b)

Fig. 3. (a) 3-dimensional contour and (b) 2-dimensioanl contour for SFDR of the BBA chain in cable with changes of A_{v1} and A_{v2}.

are zero, α is minimized and then DR_{casc} is maximized. From the above analysis, the SFDR of the BBA chain in ATSC terrestrial is optimized in the condition of $A_{V1} = 10$ (20 dB) and $A_{V2} = 2.85$ (9 dB). This result is obtained through Matlab simulation and presented in Fig. 2. The simulation conditions are listed in Table I. Rejection rates r_{i1}, r_{i2}, and r_{i3} are determined by the characteristics of the butterworth biquad filter whose quality factor (Q) is 0.7.

B. Optimal SFDR in Cable

In the broadband cable system, a maximum of 130 channels with channel bandwidth of 6 MHz are placed abutting each other from 48 MHz to 862 MHz. Therefore, composite third order inter-modulation distortion which is well known as composite triple beat (CTB) is important in multi-carrier systems such as cable. In general, $\omega_1 \pm \omega_2 \pm \omega_3$ products are 6dB higher than $2\omega_1 \pm \omega_2$ products. For the case of equally spaced carriers, the number of CTB beats is the greatest in the middle of the band and is simplified to $3N^2/8$ where N is the number of channels [5].

TABLE I
SIMULATION CONDITIONS OF BBA FOR ATSC TERRESTRIAL AND CABLE

Parameter	Value	Parameter	Value
Total BBA gain	62 dB	Corner frequency of blocks	3 MHz
$F_1(NF_1)$	100 (20 dB)	In-channel OIP31	35 dBm
$F_2(NF_2)$	500 (27 dB)	In-channel OIP32	35 dBm
$F_3(NF_3)$	1000 (30 dB)	In-channel OIP33	35 dBm
r_{i1} at 6 MHz	0.44 (-7.1 dB)	r_{i2} at 10 MHz	0.18 (-14.9 dB)
r_{i3} at 16 MHz	0.07 (-23.1 dB)		

If the BBA chain does not have any filtering effect, its optimum allocation of the gain in cable is the same as that in ATSC terrestrial. However, because the effect of filtering two tones on SFDR is different from that of filtering three tones, the optimum condition of the gain of each block in the BBA chain in cable is different from the one in ATSC terrestrial. In cable, the expression of SFDR is modified to

$$SFDR_{Cable} = \left(\frac{IIP_{3CTB,casc}}{F_{casc}\ KTB}\right)^{\frac{2}{3}} \propto DR_{CTB,casc}^{\frac{2}{3}}. \tag{6}$$

$IIP_{3CTB,casc}$ is the modified input referred third-order intercept point whose third-order components are $\omega_1 \pm \omega_2 \pm \omega_3$ products. Cascaded dynamic range, $DR_{CTB,casc}$ of the BBA chain in cable can be expressed as

$$\begin{aligned}
\frac{1}{DR_{CTB,casc}} &= \frac{F_{casc}}{V_{IIP3CTB,casc}^2} \\
&= \left(F_1 + \frac{F_2 - 1}{A_{V1}^2} + \frac{F_3 - 1}{A_{V1}^2 A_{V2}^2}\right) \times \\
&\quad \left(\frac{1}{V_{IIP3CTB1}^2} + \frac{A_{V1}^2}{V_{IIP3CTB2,Fil}^2} + \frac{A_{V1}^2 A_{V2}^2}{V_{IIP3CTB3,Fil}^2}\right) \\
&\cong \frac{F_1}{V_{IIP3CTB1}^2} + \frac{F_2}{V_{IIP3CTB2,Fil}^2} + \frac{F_3}{V_{IIP3CTB3,Fil}^2} \\
&\quad + \frac{F_1 A_{V1}^2}{V_{IIP3CTB2,Fil}^2} + \frac{F_1 A_{V1}^2 A_{V2}^2}{V_{IIP3CTB3,Fil}^2} + \frac{F_2}{A_{V1}^2 V_{IIP3CTB1}^2} \\
&\quad + \frac{A_{V2}^2 F_2}{V_{IIP3CTB3,Fil}^2} + \frac{F_3}{A_{V1}^2 A_{V2}^2 V_{IIP3CTB1}^2} + \frac{F_3}{A_{V2}^2 V_{IIP3CTB2,Fil}^2} \\
&= \frac{1}{DR_{1CTB}} + \frac{1}{DR_{2CTB}} + \frac{1}{DR_{3CTB}} + \beta
\end{aligned} \tag{7}$$

and

$$\begin{aligned}
\beta = &\frac{F_1}{V_{IIP3CTB1}^2} + \frac{F_2}{V_{IIP3CTB2,Fil}^2} + \frac{F_3}{V_{IIP3CTB3,Fil}^2} + \frac{F_1 A_{V1}^2}{V_{IIP3CTB2,Fil}^2} + \frac{F_1 A_{V1}^2 A_{V2}^2}{V_{IIP3CTB3,Fil}^2} \\
&+ \frac{F_2}{A_{V1}^2 V_{IIP3CTB1}^2} + \frac{A_{V2}^2 F_2}{V_{IIP3CTB3,Fil}^2} + \frac{F_3}{A_{V1}^2 A_{V2}^2 V_{IIP3CTB1}^2} + \frac{F_3}{A_{V2}^2 V_{IIP3CTB2,Fil}^2},
\end{aligned} \tag{8}$$

where A_{Vi} is the voltage gain of the ith block, F_i is the noise factor of the ith block, and V_{IIP3i} is the input referred third-

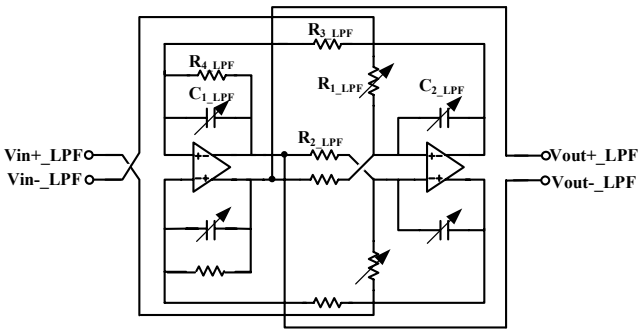


Fig. 4. Schematic of the Tow Thomas low-pass filter.

order intercept point of the ith block. $V_{IIP3CTB2,Fil}$ and $V_{IIP3CTB3,Fil}$ are the input referred third-order intercept points including filtering effect of proceeding LPFs in the BBA chain and can be expressed as:

$$V_{IIP3CTB2,Fil} = \frac{V_{IIP3CTB2}}{\sqrt{r_{11}r_{12}r_{13}}} = \frac{V_{OIP3CTB2}}{A_{V2}\sqrt{r_{11}r_{12}r_{13}}} \tag{9}$$

and

$$V_{IIP3CTB3,Fil} = \frac{V_{IIP3CTB3}}{\sqrt{r_{11}r_{12}r_{13}r_{21}r_{22}r_{23}}} = \frac{V_{OIP3CTB3}}{A_{V3}\sqrt{r_{11}r_{12}r_{13}r_{21}r_{22}r_{23}}} \ . \tag{10}$$

In these expressions, $V_{OIP3CTBi}$ is the output referred third-order intercept point of the ith block and r_{i1}, r_{i2}, and r_{i3} ($r_{i1} < 1$, $r_{i2} < 1$, and $r_{i3} < 1$) are rejection rates of the LPF of the ith block when multi-tones at the frequency of ω_1, ω_2, and ω_3 are applied to the BBA chain, respectively. When the partial differential of β to A_{V1} and A_{V2}, $\partial\beta/\partial A_{V1}$ and $\partial\beta/\partial A_{V2}$, are zero, β is minimized and then $DR_{CTB,casc}$ is maximized. Consequently, the *SFDR* of the BBA chain in cable is optimized in the condition of $A_{V1} = 4$ (12 dB) and $A_{V2} = 4.5$ (13 dB). This result is obtained through Matlab simulation and presented in Fig. 3. The simulation conditions are listed in Table I.

III. DESIGN OF BBA CIRCUITS

A. Low- pass filter

The main function of the LPF is both channel selection and anti-alias filtering for the ADC. The fully differential 6th-order butterworth LPF, which consists of three biquad (called Tow Thomas biquad [6] presented in Fig. 4.) filters in Fig. 1, satisfies attenuation specification of 75 dB at the sampling frequency of ADC of 25 MHz. Because the butterworth has excellent group delay characteristic, an additional group delay equalizer (all pass filter) is not required. The 3-dB bandwidth can be adjusted to one of 3 MHz, 3.5 MHz, and 4 MHz respectively. In digital TV tuner applications, the LPF should have both good linearity and low noise performance. Among the many filter architectures, an active-RC filter has excellent linearity because it uses a feedback system with an operational amplifier (op-amp) having the high open loop gain and linear passive elements. The higher the open loop gain of the op-amp, the better the linearity of the filter from the following equation

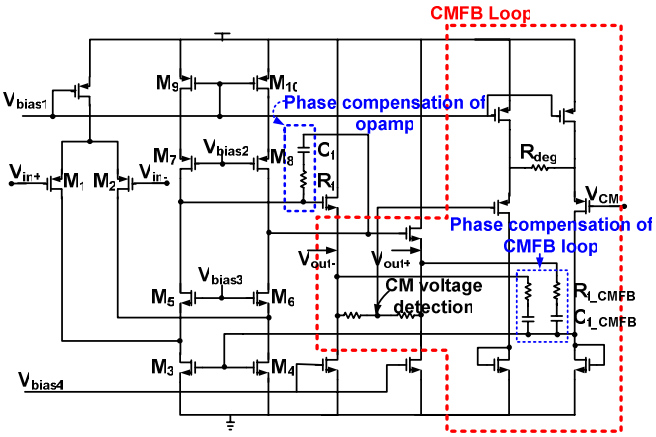


Fig. 5. Schematic of folded-cascode operational amplifier with common mode feedback loop.

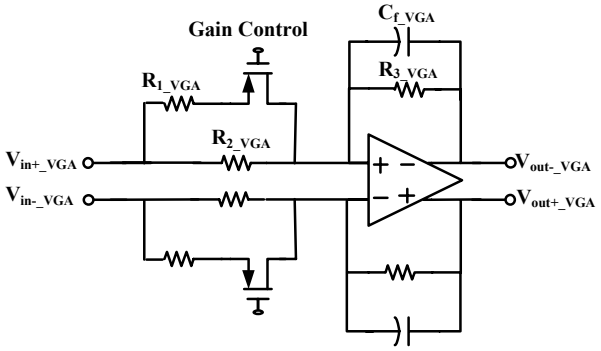


Fig. 6. Schematic of the programmable gain amplifier.

[7],

$$V_{IIP3}(\ after\ f/b\ ) = V_{IIP3}(\ before\ f/b\ ) \times (1 + A_0\beta)^{3/2}\ , \tag{11}$$

where A_0 is the open loop gain of the op-amp and β is the feedback factor. Because the op-amp has to have the high open loop gain, the folded-cascode amplifier [8], [9] in Fig. 5 is adopted. The input referred noise voltage per unit bandwidth of the second-order LPF is given by:

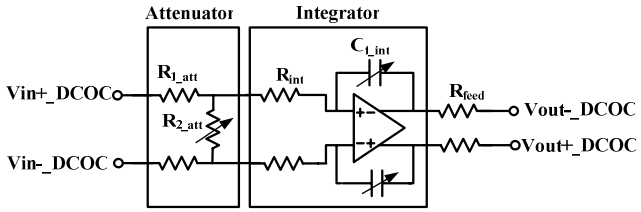
$$\overline{V_{n,LPF}^2} \cong \overline{V_{n,opamp}^2} + 4KTR_{1\_LPF} + 4KTR_{2\_LPF} \tag{12}$$

and

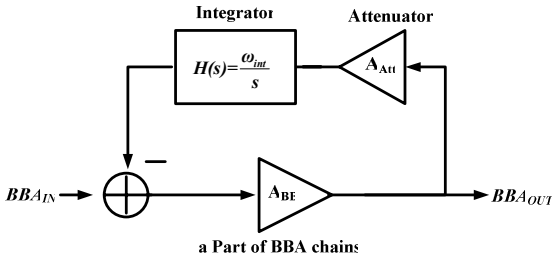
$$\begin{aligned}\overline{V_{n,opamp}^2} \cong 8kT\Big(&\frac{2}{3g_{m1,2}} + \frac{2}{3}\frac{g_{m3,4}}{g_{m1,2}^2} + \frac{2}{3}\frac{g_{m9,10}}{g_{m1,2}^2}\Big) \\ &+2\frac{K_P}{(WL)_{1,2}C_{ox}f} + 2\frac{K_N}{(WL)_{3,4}C_{ox}f}\frac{g_{m3,4}}{g_{m1,2}^2} \\ &+2\frac{K_P}{(WL)_{9,10}C_{ox}f}\frac{g_{m9,10}}{g_{m1,2}^2},\end{aligned} \tag{13}$$

where K_N and K_P denote the flicker ($1/f$) noise coefficient of NMOS and PMOS devices, respectively. To optimize the NF

of the LPF, R_{1_LPF} and R_{2_LPF} must be as small as possible. In direct conversion receivers, the flicker noise is also critical, so transistors (M_1, M_2, M_3, M_4, M_9, and M_{10}) of the op-amp should



(a)



(b)

Fig. 7. (a) Schematic of dc offset correction (DCOC) circuit. (b) Block diagram of DCOC feedback loop.

have large sizes. To drive a capacitive and resistive load, a source follower is used in every op-amp as the output buffer. Due to the required high linearity performance and 2 V input and output swing range, the 3.3 V supply voltage is used. In addition, the phase margin of the op-amp has to be compensated by a left half plane zero, which is embodied by the miller capacitance, C_f and resistance, R_f. The output common mode voltage level of the op-amp has to be maintained constantly. The common mode feedback (CMFB) loop of the op-amp in Fig. 5 performs this function. In order to stabilize the CMFB loop, the gain of the CMFB loop is reduced by a source degeneration resistor, R_{deg} and its phase margin is improved by the miller capacitor, C_{f_CMFB} and resistor, R_{f_CMFB}. Each filter has a 5-bit capacitor array, which can be switched by a digitally controlled signal. This capacitor array will compensate the variation of process, supply voltage and temperature. Tuning range from 2 MHz to 5 MHz is achieved, and it is sufficient enough to cover those variations.

B. Programmable Gain Amplifier (PGA)

The PGA should also be highly linear. As mentioned before, since negative feedback lowers the second-order and third-order nonlinearities [7], the PGA in Fig. 6 is used. The op-amp shown in Fig. 5 is used in the PGA. The gain control can be functioned by switching the resistors in the forward path and in the feedback path. In addition, C_{f_VGA} in the feedback path is added to have the small low-pass filtering effect. PGAs in the BBA chain have a gain range of 56dB from 6dB to 62dB through 8-bit control and a gain step of 0.25dB.

C. DC- Offset Cancellation

For the BBA chain used in dual conversion or direct conversion receivers, DC-offset generated mainly due to self

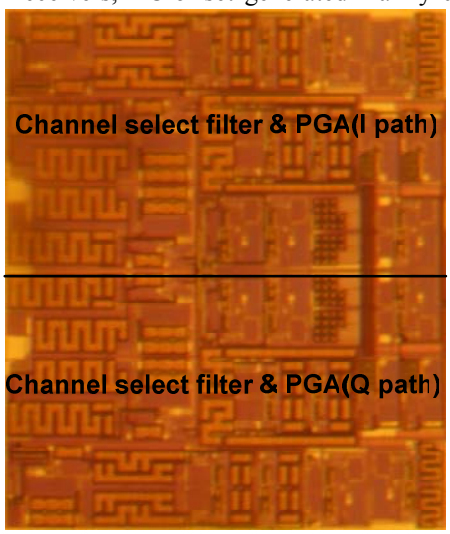


Fig. 8. Chip microphotograph of the BBA chain.

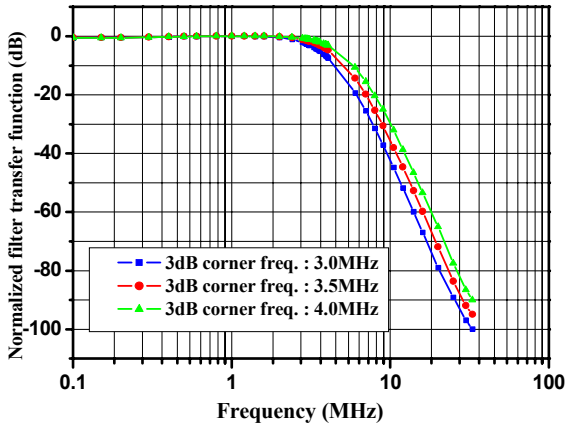


Fig. 9. Measured frequency response of the tunable analog channel select filter.

mixing in down conversion mixer and device mismatches is problematic because the gain of the BBA chain is high. Therefore, DC-offset correction is required. A static and dynamic DC-offset correction (DCOC) circuit shown in Fig. 7 (a) consists of the active RC integrator and attenuator using resistive division and two local DCOC are realized in the BBA chain of Fig. 1. Low-pass filtering in the feedback path causes high-pass filtering in the overall closed loop. Thus, it rejects DC-offset. The closed loop transfer function is

$$H_{FB}(s) \approx A_{BB} \cdot \frac{\dfrac{s}{A_{BB}A_{atten}\omega_{\text{int}}}}{\left(1+\dfrac{s}{A_{BB}A_{atten}\omega_{\text{int}}}\right)} \quad . \tag{14}$$

From (14), the 3-dB cut-off frequency of HPF is $A_{BB}A_{atten}\omega_{int}$ and due to $A_{atten} < 1$, a large time constant required in high-pass filtering can be made with relatively small capacitance

and resistance. However, as A_{atten} is getting smaller, the offset of the op-amp used in the integrator of the DCOC loop is amplified more into the output of the BBA chain. Compared to the global DCOC loop, two local DCOC loops have better performance in terms of stability and the amount of cancellation. In addition, the high-pass corner frequency is tunable. Since the settling time of DCOC loop should be short, the high-pass corner frequency is increased to high frequency in power-up mode whereas it is decreased to low frequency in normal mode.

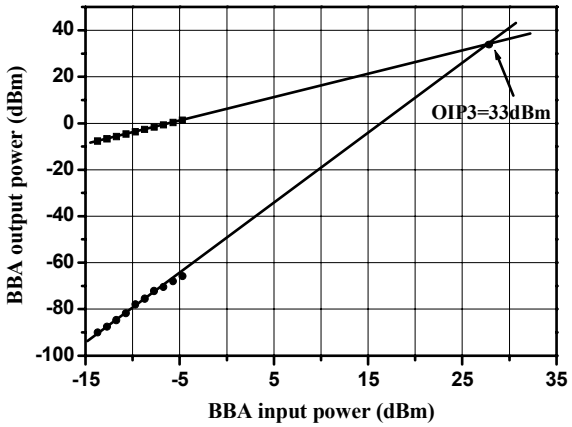


Fig. 10. Measured out-of-channel OIP3 characteristics of the BBA chain at minimum gain setting of 6dB when two tones at 6 MHz and 10 MHz are applied.

TABLE II
SUMMARY OF MEASURED PERFORMANCE

Parameter	Value
Technology	0.18-μm 1P6M CMOS process
Chip area	1 mm×1.2 mm
Gain range	6~62 dB (0.25 dB step)
Cut-off frequency	3 MHz, 3.5 MHz, 4 MHz
Input referred noise density	15.5 nV/$\sqrt{\text{Hz}}$
Out-of-channel OIP3 (two tones at 6 MHz and 10 MHz)	33 dBm
SFDR	58.1 dB
Group delay	148 ns
Current consumption	89 mA
Supply voltage	3.3 V

IV. MEASUREMENT RESULTS

The BBA chain in Fig. 1 which consists of three blocks has been fabricated in 0.18-μm CMOS technology. Each block is composed of the second order LPF and PGA. The methodology introduced in section II is utilized in the design process. Fig. 8 shows the microphotograph of the BBA chain. The chip size of the BBA chain including the LPFs, PGAs, bias circuit and buffer is 1 mm × 1.2 mm. It operates at a supply voltage of 3.3 V and its total current consumption is 89mA. Fig. 9 shows the measured frequency response of the BBA chain. The 3-dB cut-off frequency of the BBA chain can be adjusted to one of 3 MHz, 3.5 MHz and 4 MHz. The group delay is 148ns. The gain dynamic range is 56 dB from 6 dB to 62 dB with a 0.25 dB gain step. Out-of-channel OIP3 of 33 dBm is obtained at the minimum gain setting of 6 dB. For out-of-channel linearity test, 6 MHz and 10 MHz input signals are applied. The plot for the BBA linearity characteristics is presented in Fig. 10. The measurement results of the implemented BBA chain are summarized in Table II. By utilizing the methodology introduced in section II, the SFDR of 58.1 dB is achieved.

V. CONCLUSION

In this paper, the design methodology of the baseband analog chain to maximize SFDR for ATSC terrestrial and cable digital TV tuner ICs is presented. By optimizing the allocation of the gain of each block in the baseband analog chain, a fully integrated tunable CMOS baseband analog chain with excellent SFDR performance is implemented in the 0.18-μm CMOS process. It provides a minimum input referred noise density of 15.5 nV/$\sqrt{\text{Hz}}$ with 62 dB gain and out-of-channel OIP3 of 33 dBm at the power consumption of 294 mW. This design methodology can be applied to the baseband analog chain in other applications.

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Kuduck Kwon was born in Daegu, Korea, in 1981. He received the B.S. degree in Electrical Engineering and Computer Science (EECS) from Korea Advanced Institute of Science and Technology (KAIST), in Daejeon, Korea, in 2004. He is currently pursuing the Ph.D degree in EECS from KAIST.

His current research activities include RF circuits and baseband analog circuits for CMOS Digital TV Tuner IC design.

Hong-Teuk Kim received the M.S degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, in 1993, and the Ph.D. degree from the Seoul National University, Seoul, Korea, in 2004, where his works were MMIC designs for 6-18GHz power amplifier, Ka/Q-band phase shifter, 60GHz active antenna transmitter, and many pioneering designs for mm-wave low-loss MEMS circuits such as new transmission line, tunable filter, and phase shifter for 60 GHz beam forming system.

In 2002, he joined LG Electronics Institute of Technology, and designed high efficient and linear power amplifier MMIC for CDMA mobile phone, RF sensor system for Volatile Organic Compound (VOC) detection, and compact wideband mobile internal antenna up to 2004. Currently he works as a team leader for DTV CMOS RFIC development and a technical consultant for PDP EMI, and also serves as a member of LG Technical Expert Council in RF area.

Kwyro Lee (M'80-SM'90) received the B.S. degree in electronics engineering from Seoul National University, Seoul, Korea, in 1976 and the M.S. and Ph.D. degrees from the University of Minnesota, Minneapolis, in 1981 and 1983, respectively, where he did many pioneering works for characterization and modeling of AlGaAs/GaAs hetero-junction field effect transistor.

From 1983 to 1986, he worked as an Engineering General Manager with GoldStar Semiconductor Inc., Korea, responsible for the development of the first polysilicon CMOS products in Korea. In 1987, he joined the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1987 as an Assistant Professor in the department of electrical engineering. He is currently a Professor with KAIST. From 1998 to 2000, he served as the KAIST Dean of Research Affairs and the Dean of Institute Development and Cooperation. Since 1997, he has been the Director of the Micro Information and Communication Remote-object Oriented Systems (MICROS) Research Center, an Engineering Center of Excellence supported by the Korea Science and Engineering Foundation. In March 2005, he joined LG Electronics Institute of Technology, Seoul, as Executive Vice President. He has authored or coauthored over 150 publications in major international journals and conferences. He authored *Semiconductor Device Modeling for VLSI* (Englewood Cliffs, NJ: Prentice Hall, 1993) and was one of the co-developers of AIM-Spice, the world's first SPICE run under Windows.

Dr. Lee is a Life Member of the Korean Institute of Electrical and Communications Engineers. From 1990 to 1996, he served as the Conference Co-Chair of the International Semiconductor Device Research Symposium, Charlottesville, VA. From1998 to 2000, he served as the Chairman of the IEEE Korea Electron Device Chapter and currently serves as an Elected Member of the Administrative Committee (AdCom) of the Electron Devices Society (EDS).